

## High-Speed CMOS Logic 9-Bit Odd/Even Parity Generator/Checker

### Features

- Typical Propagation Delay = 17ns at  $V_{CC} = 5V$ ,  $C_L = 15pF$ ,  $T_A = 25^\circ C$
- Replaces LS180 Types
- Easily Cascadable
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . .  $-55^\circ C$  to  $125^\circ C$
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5V$
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility,  $V_{IL} = 0.8V$  (Max),  $V_{IH} = 2V$  (Min)
  - CMOS Input Compatibility,  $I_I \leq 1\mu A$  at  $V_{OL}$ ,  $V_{OH}$

### Description

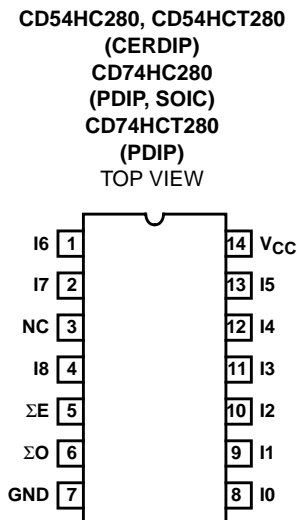
The 'HC280 and 'HCT280 are 9-bit odd/even parity, generator checker devices. Both even and odd parity outputs are available for checking or generating parity for words up to nine bits long. Even parity is indicated ( $\Sigma E$  output is high) when an even number of data inputs is high. Odd parity is indicated ( $\Sigma O$  output is high) when an odd number of data inputs is high. Parity checking for words larger than 9 bits can be accomplished by tying the  $\Sigma E$  output to any input of an additional HC/HCT280 parity checker.

### Ordering Information

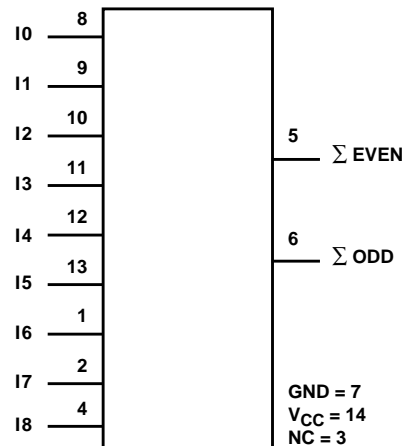
| PART NUMBER   | TEMP. RANGE (°C) | PACKAGE      |
|---------------|------------------|--------------|
| CD54HC280F3A  | -55 to 125       | 14 Ld Cerdip |
| CD54HCT280F3A | -55 to 125       | 14 Ld Cerdip |
| CD74HC280E    | -55 to 125       | 14 Ld PDIP   |
| CD74HC280MT   | -55 to 125       | 14 Ld SOIC   |
| CD74HC280M96  | -55 to 125       | 14 Ld SOIC   |
| CD74HCT280E   | -55 to 125       | 14 Ld PDIP   |

NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

### Pinout



### Functional Diagram



## CD54HC280, CD74HC280, CD54HCT280, CD74HCT280

### Absolute Maximum Ratings

|  |             |
|--|-------------|
| DC Supply Voltage, $V_{CC}$ .....                      | -0.5V to 7V |
| DC Input Diode Current, $I_{IK}$                       |             |
| For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ .....       | $\pm 20mA$  |
| DC Output Diode Current, $I_{OK}$                      |             |
| For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ .....       | $\pm 20mA$  |
| DC Drain Current, per Output, $I_O$                    |             |
| For $-0.5V < V_O < V_{CC} + 0.5V$ .....                | $\pm 25mA$  |
| DC Output Source or Sink Current per Output Pin, $I_O$ |             |
| For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ .....       | $\pm 25mA$  |
| DC $V_{CC}$ or Ground Current, $I_{CC}$ .....          | $\pm 50mA$  |

### Thermal Information

|  |   |
|--|---|
| Thermal Resistance (Typical, Note1)            | $\theta_{JA}$ ( $^{\circ}C/W$ )           |
| E (PDIP) Package .....                         | 80  |
| M (SOIC) Package .....                         | 86  |
| Maximum Junction Temperature .....             | $150^{\circ}C$                            |
| Maximum Storage Temperature Range .....        | $-65^{\circ}C$ to $150^{\circ}C$          |
| Maximum Lead Temperature (Soldering 10s) ..... | $300^{\circ}C$<br>(SOIC - Lead Tips Only) |

### Operating Conditions

|  |                                  |
|--|----------------------------------|
| Temperature Range, $T_A$ .....               | $-55^{\circ}C$ to $125^{\circ}C$ |
| Supply Voltage Range, $V_{CC}$               |                                  |
| HC Types .....                               | 2V to 6V                         |
| HCT Types .....                              | 4.5V to 5.5V                     |
| DC Input or Output Voltage, $V_I, V_O$ ..... | 0V to $V_{CC}$                   |
| Input Rise and Fall Time                     |                                  |
| 2V .....                                     | 1000ns (Max)                     |
| 4.5V .....                                   | 500ns (Max)                      |
| 6V .....                                     | 400ns (Max)                      |

**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

#### NOTE:

- The package thermal impedance is calculated in accordance with JEDEC 51-7.

### DC Electrical Specifications

| PARAMETER                               | SYMBOL   | TEST CONDITIONS         |            |              | 25°C |     |           | -40°C TO 85°C |         | -55°C TO 125°C |         | UNITS   |
|---|----------|-------------------------|------------|--------------|------|-----|-----------|---------------|---------|----------------|---------|---------|
|   |          | $V_I$ (V)               | $I_O$ (mA) | $V_{CC}$ (V) | MIN  | TYP | MAX       | MIN           | MAX     | MIN            | MAX     |         |
| <b>HC TYPES</b>                         |          |                         |            |              |      |     |           |               |         |                |         |         |
| High Level Input Voltage                | $V_{IH}$ | -                       | -          | 2            | 1.5  | -   | -         | 1.5           | -       | 1.5            | -       | V       |
|   |          |                         |            | 4.5          | 3.15 | -   | -         | 3.15          | -       | 3.15           | -       | V       |
|   |          |                         |            | 6            | 4.2  | -   | -         | 4.2           | -       | 4.2            | -       | V       |
| Low Level Input Voltage                 | $V_{IL}$ | -                       | -          | 2            | -    | -   | 0.5       | -             | 0.5     | -              | 0.5     | V       |
|   |          |                         |            | 4.5          | -    | -   | 1.35      | -             | 1.35    | -              | 1.35    | V       |
|   |          |                         |            | 6            | -    | -   | 1.8       | -             | 1.8     | -              | 1.8     | V       |
| High Level Output Voltage<br>CMOS Loads | $V_{OH}$ | $V_{IH}$ or<br>$V_{IL}$ | -0.02      | 2            | 1.9  | -   | -         | 1.9           | -       | 1.9            | -       | V       |
|   |          |                         | -0.02      | 4.5          | 4.4  | -   | -         | 4.4           | -       | 4.4            | -       | V       |
|   |          |                         | -0.02      | 6            | 5.9  | -   | -         | 5.9           | -       | 5.9            | -       | V       |
| High Level Output Voltage<br>TTL Loads  | $V_{OH}$ | $V_{IH}$ or<br>$V_{IL}$ | -4         | 4.5          | 3.98 | -   | -         | 3.84          | -       | 3.7            | -       | V       |
|   |          |                         | -5.2       | 6            | 5.48 | -   | -         | 5.34          | -       | 5.2            | -       | V       |
| Low Level Output Voltage<br>CMOS Loads  | $V_{OL}$ | $V_{IH}$ or<br>$V_{IL}$ | 0.02       | 2            | -    | -   | 0.1       | -             | 0.1     | -              | 0.1     | V       |
|   |          |                         | 0.02       | 4.5          | -    | -   | 0.1       | -             | 0.1     | -              | 0.1     | V       |
|   |          |                         | 0.02       | 6            | -    | -   | 0.1       | -             | 0.1     | -              | 0.1     | V       |
| Low Level Output Voltage<br>TTL Loads   | $V_{OL}$ | $V_{IH}$ or<br>$V_{IL}$ | 4          | 4.5          | -    | -   | 0.26      | -             | 0.33    | -              | 0.4     | V       |
|   |          |                         | 5.2        | 6            | -    | -   | 0.26      | -             | 0.33    | -              | 0.4     | V       |
| Input Leakage Current                   | $I_I$    | $V_{CC}$ or<br>GND      | -          | 6            | -    | -   | $\pm 0.1$ | -             | $\pm 1$ | -              | $\pm 1$ | $\mu A$ |
| Quiescent Device Current                | $I_{CC}$ | $V_{CC}$ or<br>GND      | 0          | 6            | -    | -   | 8         | -             | 80      | -              | 160     | $\mu A$ |

**CD54HC280, CD74HC280, CD54HCT280, CD74HCT280**

**DC Electrical Specifications (Continued)**

| PARAMETER  | SYMBOL                    | TEST CONDITIONS                    |                     | V <sub>CC</sub> (V) | 25°C |     |      | -40°C TO 85°C |      | -55°C TO 125°C |     | UNITS |
|--|---------------------------|------------------------------------|---------------------|---------------------|------|-----|------|---------------|------|----------------|-----|-------|
|  |                           | V <sub>I</sub> (V)                 | I <sub>O</sub> (mA) |                     | MIN  | TYP | MAX  | MIN           | MAX  | MIN            | MAX |       |
| <b>HCT TYPES</b>   |                           |                                    |                     |                     |      |     |      |               |      |                |     |       |
| High Level Input Voltage                                       | V <sub>IH</sub>           | -                                  | -                   | 4.5 to 5.5          | 2    | -   | -    | 2             | -    | 2              | -   | V     |
| Low Level Input Voltage  | V <sub>IL</sub>           | -                                  | -                   | 4.5 to 5.5          | -    | -   | 0.8  | -             | 0.8  | -              | 0.8 | V     |
| High Level Output Voltage<br>CMOS Loads                        | V <sub>OH</sub>           | V <sub>IH</sub> or V <sub>IL</sub> | -0.02               | 4.5                 | 4.4  | -   | -    | 4.4           | -    | 4.4            | -   | V     |
| High Level Output Voltage<br>TTL Loads                         |                           |                                    | -4                  | 4.5                 | 3.98 | -   | -    | 3.84          | -    | 3.7            | -   | V     |
| Low Level Output Voltage<br>CMOS Loads                         | V <sub>OL</sub>           | V <sub>IH</sub> or V <sub>IL</sub> | 0.02                | 4.5                 | -    | -   | 0.1  | -             | 0.1  | -              | 0.1 | V     |
| Low Level Output Voltage<br>TTL Loads                          |                           |                                    | 4                   | 4.5                 | -    | -   | 0.26 | -             | 0.33 | -              | 0.4 | V     |
| Input Leakage Current  | I <sub>I</sub>            | V <sub>CC</sub> to GND             | 0                   | 5.5                 | -    | -   | ±0.1 | -             | ±1   | -              | ±1  | μA    |
| Quiescent Device Current                                       | I <sub>CC</sub>           | V <sub>CC</sub> or GND             | 0                   | 5.5                 | -    | -   | 8    | -             | 80   | -              | 160 | μA    |
| Additional Quiescent Device Current Per Input Pin: 1 Unit Load | ΔI <sub>CC</sub> (Note 2) | V <sub>CC</sub> -2.1               | -                   | 4.5 to 5.5          | -    | 100 | 360  | -             | 450  | -              | 490 | μA    |

NOTE:

2. For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4V, V<sub>CC</sub> = 5.5V) specification is 1.8mA.

**HCT Input Loading Table**

| INPUT | UNIT LOADS |
|-------|------------|
| All   | 1          |

NOTE: Unit Load is ΔI<sub>CC</sub> limit specified in DC Electrical Specifications table, e.g., 360μA max at 25°C.

**Switching Specifications** Input t<sub>r</sub>, t<sub>f</sub> = 6ns

| PARAMETER                          | SYMBOL                              | TEST CONDITIONS       | V <sub>CC</sub> (V) | 25°C |     | -40°C TO 85°C | -55°C TO 125°C | UNITS |
|------------------------------------|-------------------------------------|-----------------------|---------------------|------|-----|---------------|----------------|-------|
|                                    |                                     |                       |                     | TYP  | MAX | MAX           | MAX            |       |
| <b>HC TYPES</b>                    |                                     |                       |                     |      |     |               |                |       |
| Propagation Delay, Any Input to ΣO | t <sub>PLH</sub> , t <sub>PHL</sub> | C <sub>L</sub> = 50pF | 2                   | -    | 200 | 250           | 300            | ns    |
|                                    |                                     |                       | 4.5                 | -    | 40  | 50            | 60             | ns    |
|                                    |                                     |                       | 6                   | -    | 34  | 43            | 51             | ns    |
|                                    |                                     | C <sub>L</sub> = 15pF | 5                   | 17   | -   | -             | -              | ns    |
| Propagation Delay, Any Input to ΣE | t <sub>PLH</sub> , t <sub>PHL</sub> | C <sub>L</sub> = 50pF | 2                   | -    | 200 | 250           | 300            | ns    |
|                                    |                                     |                       | 4.5                 | -    | 40  | 50            | 60             | ns    |
|                                    |                                     |                       | 6                   | -    | 34  | 43            | 51             | ns    |
|                                    |                                     | C <sub>L</sub> = 15pF | 5                   | 17   | -   | -             | -              | ns    |

## CD54HC280, CD74HC280, CD54HCT280, CD74HCT280

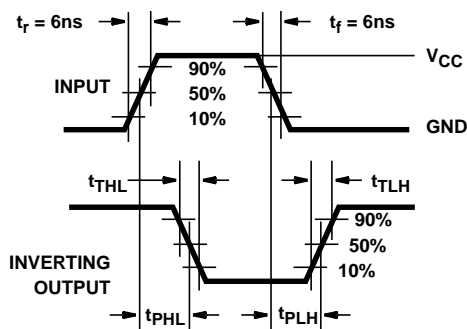
### Switching Specifications Input $t_r, t_f = 6\text{ns}$ (Continued)

| PARAMETER                                  | SYMBOL             | TEST CONDITIONS     | $V_{CC}$ (V) | 25°C |     | -40°C TO 85°C | -55°C TO 125°C | UNITS |
|--|--------------------|---------------------|--------------|------|-----|---------------|----------------|-------|
|  |                    |                     |              | TYP  | MAX | MAX           | MAX            |       |
| Output Transition Time                     | $t_{TLH}, t_{THL}$ | $C_L = 50\text{pF}$ | 2            | -    | 75  | 95            | 110            | ns    |
|  |                    |                     | 4.5          | -    | 15  | 19            | 22             | ns    |
|  |                    |                     | 6            | -    | 13  | 16            | 19             | ns    |
| Input Capacitance                          | $C_I$              | -                   | -            | -    | 10  | 10            | 10             | pF    |
| Power Dissipation Capacitance (Notes 3, 4) | $C_{PD}$           | -                   | 5            | 58   | -   | -             | -              | pF    |
| <b>HCT TYPES</b>                           |                    |                     |              |      |     |               |                |       |
| Propagation Delay, Any Input to $\Sigma O$ | $t_{PLH}, t_{PHL}$ | $C_L = 50\text{pF}$ | 4.5          | -    | 45  | 56            | 68             | ns    |
|  |                    | $C_L = 15\text{pF}$ | 5            | 19   | -   | -             | -              | ns    |
| Propagation Delay, Any Input to $\Sigma E$ | $t_{PLH}, t_{PHL}$ | $C_L = 50\text{pF}$ | 4.5          | -    | 42  | 53            | 63             | ns    |
|  |                    | $C_L = 15\text{pF}$ | 5            | 18   | -   | -             | -              | ns    |
| Output Transition Time                     | $t_{TLH}, t_{THL}$ | $C_L = 50\text{pF}$ | 4.5          | -    | 15  | 19            | 22             | ns    |
| Input Capacitance                          | $C_{IN}$           | -                   | -            | -    | 10  | 10            | 10             | pF    |
| Power Dissipation Capacitance (Notes 3, 4) | $C_{PD}$           | -                   | 5            | 58   | -   | -             | -              | pF    |

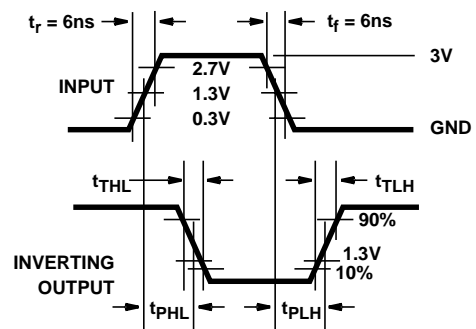
**NOTES:**

3.  $C_{PD}$  is used to determine the dynamic power consumption, per package.
4.  $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$  where  $f_i$  = Input Frequency,  $f_o$  = Output Frequency,  $C_L$  = Output Load Capacitance,  $V_{CC}$  = Supply Voltage.

### Test Circuits and Waveforms



**FIGURE 1. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC**



**FIGURE 2. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC**

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| Wireless         |  | Video & Imaging     | <a href="http://www.ti.com/video">www.ti.com/video</a>                   |
|                  |  | Wireless            | <a href="http://www.ti.com/wireless">www.ti.com/wireless</a>             |

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**PACKAGING INFORMATION**

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| 8607701CA        | ACTIVE                | CDIP         | J               | 14   | 1           | TBD                     | A42 SNPB         | N / A for Pkg Type           |
| CD54HC280F3A     | ACTIVE                | CDIP         | J               | 14   | 1           | TBD                     | A42 SNPB         | N / A for Pkg Type           |
| CD54HCT280F3A    | ACTIVE                | CDIP         | J               | 14   | 1           | TBD                     | A42 SNPB         | N / A for Pkg Type           |
| CD74HC280E       | ACTIVE                | PDIP         | N               | 14   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| CD74HC280EE4     | ACTIVE                | PDIP         | N               | 14   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| CD74HC280M96     | ACTIVE                | SOIC         | D               | 14   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HC280M96E4   | ACTIVE                | SOIC         | D               | 14   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HC280M96G4   | ACTIVE                | SOIC         | D               | 14   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HC280MT      | ACTIVE                | SOIC         | D               | 14   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HC280MTE4    | ACTIVE                | SOIC         | D               | 14   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HC280MTG4    | ACTIVE                | SOIC         | D               | 14   | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| CD74HCT280E      | ACTIVE                | PDIP         | N               | 14   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |
| CD74HCT280EE4    | ACTIVE                | PDIP         | N               | 14   | 25          | Pb-Free (RoHS)          | CU NIPDAU        | N / A for Pkg Type           |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

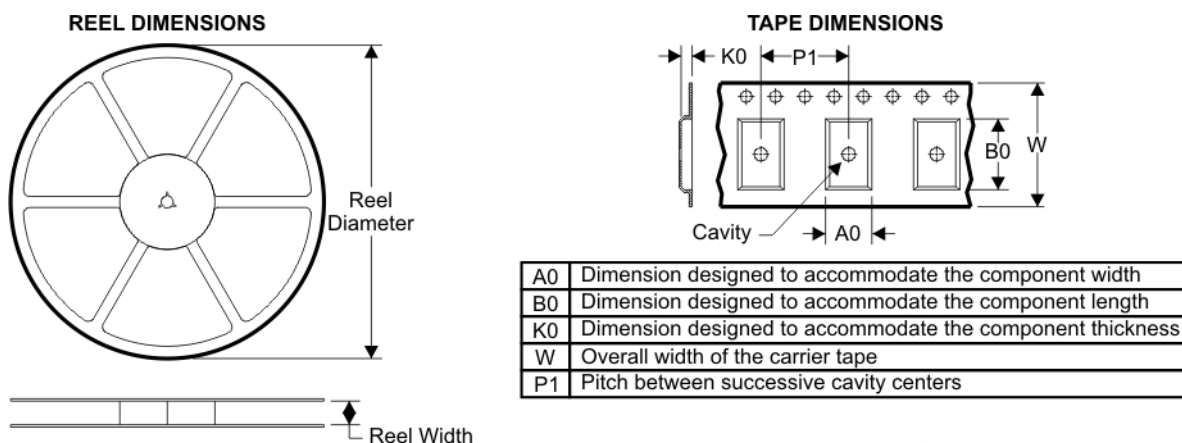
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

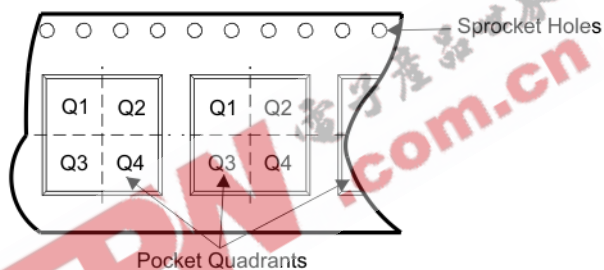
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

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**TAPE AND REEL BOX INFORMATION**



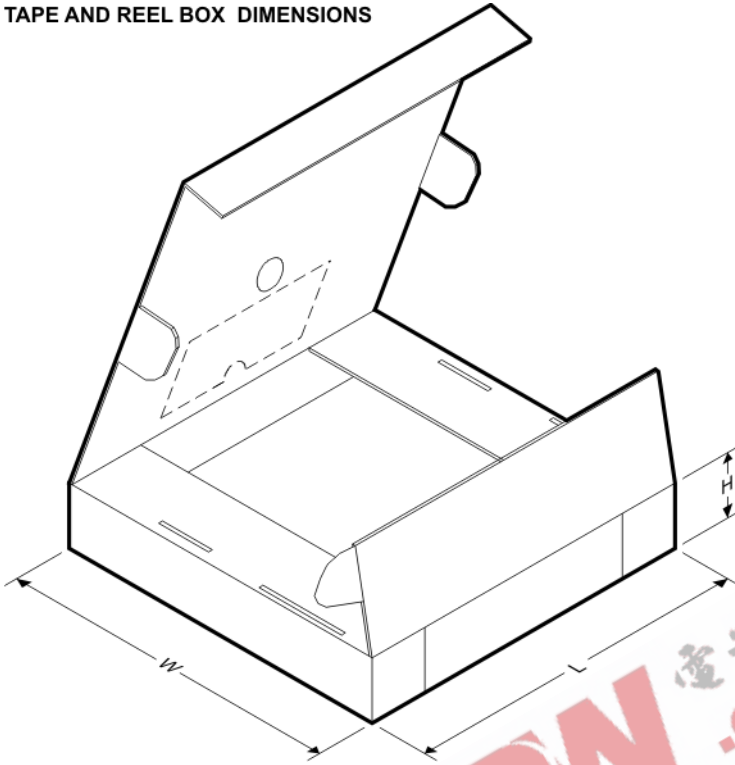
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



| Device       | Package | Pins | Site    | Reel Diameter (mm) | Reel Width (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|---------|------|---------|--------------------|-----------------|---------|---------|---------|---------|--------|---------------|
| CD74HC280M96 | D       | 14   | SITE 41 | 330                | 16              | 6.5     | 9.0     | 2.1     | 8       | 16     | Q1            |



**TAPE AND REEL BOX DIMENSIONS**



| Device       | Package | Pins | Site    | Length (mm) | Width (mm) | Height (mm) |
|--------------|---------|------|---------|-------------|------------|-------------|
| CD74HC280M96 | D       | 14   | SITE 41 | 346.0       | 346.0      | 33.0        |

J (R-GDIP-T\*\*)   
 14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14                     | 16                     | 18                     | 20                     |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A             | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX         | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN         | —                      | —                      | —                      | —                      |
| C MAX         | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN         | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



4040083/F 03/03

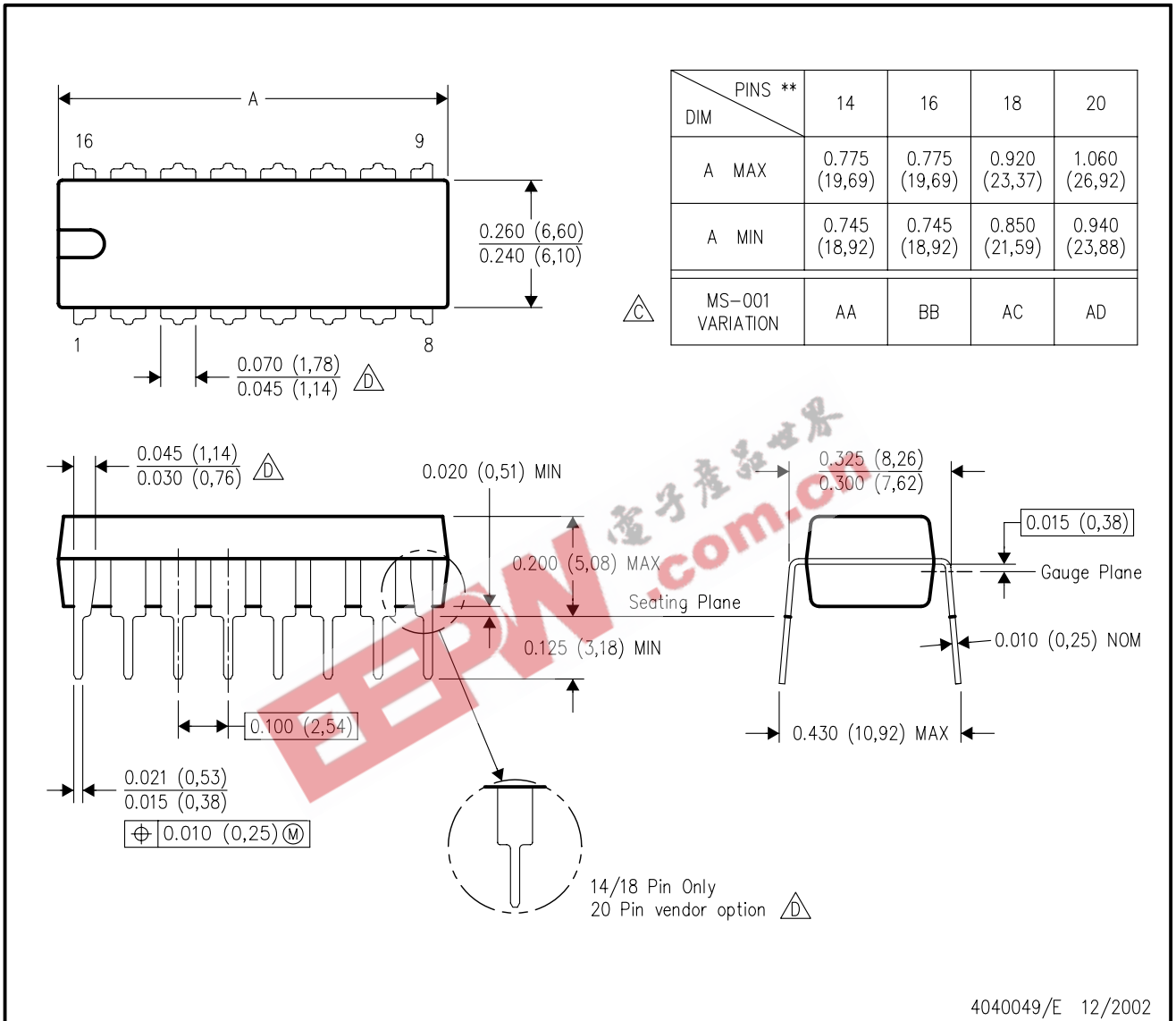
- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

# MECHANICAL DATA

## N (R-PDIP-T\*\*)

## PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



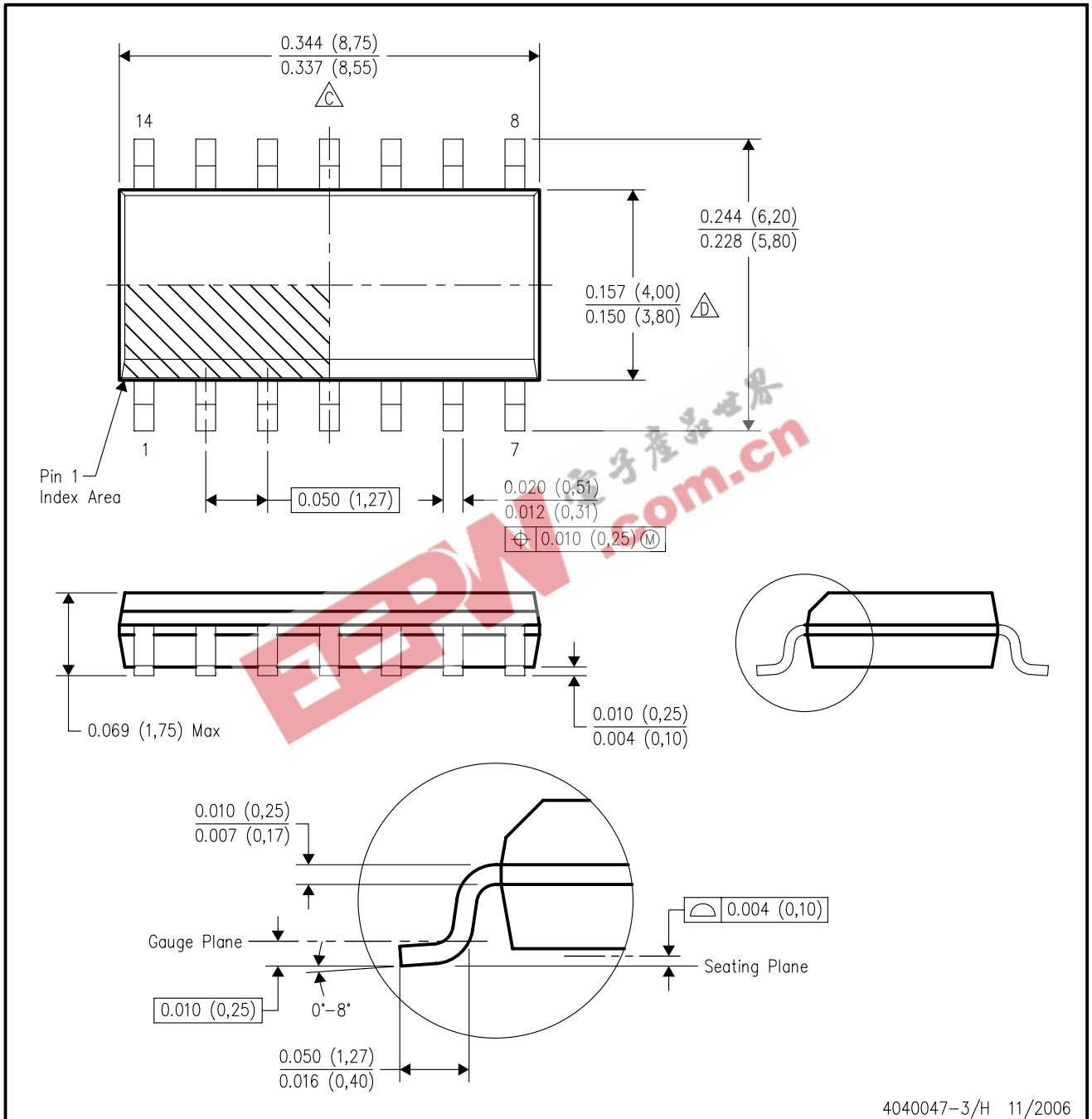
- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.

- △ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 △ The 20 pin end lead shoulder width is a vendor option, either half or full width.

# MECHANICAL DATA

## D (R-PDSO-G14)

## PLASTIC SMALL-OUTLINE PACKAGE



4040047-3/H 11/2006

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
  - Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
  - Reference JEDEC MS-012 variation AB.