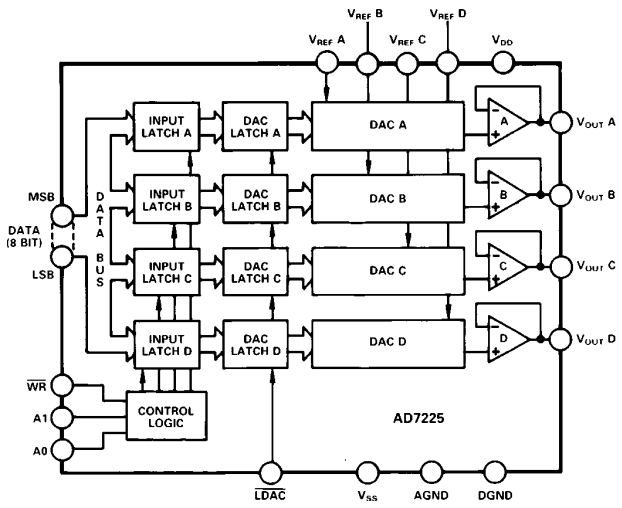
LC²MOS Quad 8-Bit DAC with Separate Reference Inputs

AD7225

FEATURES

Four 8-Bit DACs with Output Amplifiers
Separate Reference Input for Each DAC
µP Compatible with Double-Buffered Inputs
Simultaneous Update of All Four Outputs
Operates with Single or Dual Supplies
Extended Temperature Range Operation
No User Trims Required
Skinny 24-Pin DIP, SOIC and 28-Terminal Surface Mount Packages

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7225 contains four 8-bit voltage output digital-to-analog converters, with output buffer amplifiers and interface logic on a single monolithic chip. Each D/A converter has a separate reference input terminal. No external trims are required to achieve full specified performance for the part.

The double-buffered interface logic consists of two 8-bit registers per channel–an input register and a DAC register. Control inputs A0 and A1 determine which input register is loaded when $\overline{WR}$ goes low. Only the data held in the DAC registers determines the analog outputs of the converters. The double-buffering allows simultaneous update of all four outputs under control of $\overline{LDAC}$. All logic inputs are TTL and CMOS (5 V) level compatible and the control logic is speed compatible with most 8-bit microprocessors.

Specified performance is guaranteed for input reference voltages from +2 V to +12.5 V when using dual supplies. The part is also specified for single supply operation using a reference of +10 V. Each output buffer amplifier is capable of developing +10 V across a 2 kΩ load.

The AD7225 is fabricated on an all ion-implanted high-speed Linear Compatible CMOS (LC²MOS) process which has been specifically developed to integrate high speed digital logic circuits and precision analog circuitry on the same chip.

PRODUCT HIGHLIGHTS

1. DACs and Amplifiers on CMOS Chip
   The single-chip design of four 8-bit DACs and amplifiers allows a dramatic reduction in board space requirements and offers increased reliability in systems using multiple converters. Its pinout is aimed at optimizing board layout with all analog inputs and outputs at one end of the package and all digital inputs at the other.
2. Single or Dual Supply Operation
   The voltage-mode configuration of the AD7225 allows single supply operation. The part can also be operated with dual supplies giving enhanced performance for some parameters.
3. Versatile Interface Logic
   The AD7225 has a common 8-bit data bus with individual DAC latches, providing a versatile control architecture for simple interface to microprocessors. The double-buffered interface allows simultaneous update of the four outputs.
4. Separate Reference Input for Each DAC
   The AD7225 offers great flexibility in dealing with input signals with a separate reference input provided for each DAC and each reference having variable input voltage capability.

REV. B

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 **Fax: 617/326-8703**

AD7225–SPECIFICATIONS

DUAL SUPPLY

(V_{DD} = 11.4 V to 16.5 V, V_{SS} = –5 V ± 10%; AGND = DGND = 0 V; V_{REF} = +2 V to (V_{DD} – 4 V)[1] unless otherwise noted. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	K, B Versions[2]	L, C Versions[2]	T Version	U Version	Units	Conditions/Comments
STATIC PERFORMANCE						
Resolution	8	8	8	8	Bits	
Total Unadjusted Error	±2	±1	±2	±1	LSB max	V_{DD} = +15 V ± 5%, V_{REF} = +10 V
Relative Accuracy	±1	±1/2	±1	±1/2	LSB max	
Differential Nonlinearity	±1	±1	±1	±1	LSB max	Guaranteed Monotonic
Full-Scale Error	±1	±1/2	±1	±1/2	LSB max	
Full-Scale Temp. Coeff.	±5	±5	±5	±5	ppm/°C typ	V_{DD} = 14 V to 16.5 V, V_{REF} = +10 V
Zero Code Error @ 25°C	±25	±15	±25	±15	mV max	
T_{MIN} to T_{MAX}	±30	±20	±30	±20	mV max	
Zero Code Error Temp Coeff.	±30	±30	±30	±30	µV/°C typ	
REFERENCE INPUT						
Voltage Range	2 to (V_{DD} – 4)	2 to (V_{DD} – 4)	2 to (V_{DD} – 4)	2 to (V_{DD} – 4)	V min to V max	
Input Resistance	11	11	11	11	kΩ min	
Input Capacitance[3]	100	100	100	100	pF max	Occurs when each DAC is loaded with all 1s.
Channel-to-Channel Isolation[3]	60	60	60	60	dB min	V_{REF} = 10 V p-p Sine Wave @ 10 kHz
AC Feedthrough[3]	–70	–70	–70	–70	dB max	V_{REF} = 10 V p-p Sine Wave @ 10 kHz
DIGITAL INPUTS						
Input High Voltage, V_{INH}	2.4	2.4	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	0.8	0.8	V max	
Input Leakage Current	±1	±1	±1	±1	µA max	V_{IN} = 0 V or V_{DD}
Input Capacitance[3]	8	8	8	8	pF max	
Input Coding	Binary	Binary	Binary	Binary		
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate[3]	2.5	2.5	2.5	2.5	V/µs min	
Voltage Output Settling Time[3]						
Positive Full-Scale Change	5	5	5	5	µs max	V_{REF} = +10 V; Settling Time to ±1/2 LSB
Negative Full-Scale Change	5	5	5	5	µs max	V_{REF} = +10 V; Settling Time to ±1/2 LSB
Digital Feedthrough[3]	50	50	50	50	nV secs typ	Code transition all 0s to all 1s.
Digital Crosstalk[3]	50	50	50	50	nV secs typ	Code transition all 0s to all 1s.
Minimum Load Resistance	2	2	2	2	kΩ min	V_{OUT} = +10 V
POWER SUPPLIES						
V_{DD} Range	11.4/16.5	11.4/16.5	11.4/16.5	11.4/16.5	V min to V max	For Specified Performance
I_{DD}	10	10	12	12	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
I_{SS}	9	9	10	10	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
SWITCHING CHARACTERISTICS[3, 4]						
t_1						
@ 25°C	95	95	95	95	ns min	Write Pulse Width
T_{MIN} to T_{MAX}	120	120	150	150	ns min	
t_2						
@ 25°C	0	0	0	0	ns min	Address to Write Setup Time
T_{MIN} to T_{MAX}	0	0	0	0	ns min	
t_3						
@ 25°C	0	0	0	0	ns min	Address to Write Hold Time
T_{MIN} to T_{MAX}	0	0	0	0	ns min	
t_4						
@ 25°C	70	70	70	70	ns min	Data Valid to Write Setup Time
T_{MIN} to T_{MAX}	90	90	90	90	ns min	
t_5						
@ 25°C	10	10	10	10	ns min	Data Valid to Write Hold Time
T_{MIN} to T_{MAX}	10	10	10	10	ns min	
t_6						
@ 25°C	95	95	95	95	ns min	Load DAC Pulse Width
T_{MIN} to T_{MAX}	120	120	150	150	ns min	

NOTES
[1]Maximum possible reference voltage.
[2]Temperature ranges are as follows:
K, L Versions: –40°C to +85°C
B, C Versions: –40°C to +85°C
T, U Versions: –55°C to +125°C
[3]Sample Tested at 25°C to ensure compliance.
[4]Switching characteristics apply for single and dual supply operation.

Specifications subject to change without notice.

SINGLE SUPPLY

(V_{DD} = +15 V ± 5%; V_{SS} = AGND = DGND = 0 V; V_{REF} = +10 V[1] unless otherwise noted. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	K, B Versions[2]	L, C Versions[2]	T Version	U Version	Units	Conditions/Comments
STATIC PERFORMANCE						
Resolution	8	8	8	8	Bits	
Total Unadjusted Error[3]	±2	±1	±2	±1	LSB max	
Differential Nonlinearity[3]	±1	±1	±1	±1	LSB max	Guaranteed Monotonic
REFERENCE INPUT						
Input Resistance	11	11	11	11	kΩ min	
Input Capacitance[4]	100	100	100	100	pF max	Occurs when each DAC is loaded with all 1s.
Channel-to-Channel Isolation[3, 4]	60	60	60	60	dB min	V_{REF} = 10 V p-p Sine Wave @ 10 kHz
AC Feedthrough[3, 4, 5]	–70	–70	–70	–70	dB max	V_{REF} = 10 V p-p Sine Wave @ 10 kHz
DIGITAL INPUTS						
Input High Voltage, V_{INH}	2.4	2.4	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	0.8	0.8	V max	
Input Leakage Current	±1	±1	±1	±1	µA max	V_{IN} = 0 V or V_{DD}
Input Capacitance[4]	8	8	8	8	pF max	
Input Coding	Binary	Binary	Binary	Binary		
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate[4]	2	2	2	2	V/µs min	
Voltage Output Settling Time[4]						
Positive Full-Scale Change	5	5	5	5	µs max	Settling Time to ±1/2 LSB
Negative Full-Scale Change	7	7	7	7	µs max	Settling Time to ±1/2 LSB
Digital Feedthrough[3, 4]	50	50	50	50	nV secs typ	Code transition all 0s to all 1s.
Digital Crosstalk[3, 4]	50	50	50	50	nV secs typ	Code transition all 0s to all 1s.
Minimum Load Resistance	2	2	2	2	kΩ min	V_{OUT} = +10 V
POWER SUPPLIES						
V_{DD} Range	14.25/15.75	14.25/15.75	14.25/15.75	14.25/15.75	V min to V max	For Specified Performance
I_{DD}	10	10	12	12	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
SWITCHING CHARACTERISTICS[4]						
t_1						
@ 25°C	95	95	95	95	ns min	Write Pulse Width
T_{MIN} to T_{MAX}	120	120	150	150	ns min	
t_2						
@ 25°C	0	0	0	0	ns min	Address to Write Setup Time
T_{MIN} to T_{MAX}	0	0	0	0	ns min	
t_3						
@ 25°C	0	0	0	0	ns min	Address to Write Hold Time
T_{MIN} to T_{MAX}	0	0	0	0	ns min	
t_4						
@ 25°C	70	70	70	70	ns min	Data Valid to Write Setup Time
T_{MIN} to T_{MAX}	90	90	90	90	ns min	
t_5						
@ 25°C	10	10	10	10	ns min	Data Valid to Write Hold Time
T_{MIN} to T_{MAX}	10	10	10	10	ns min	
t_6						
@ 25°C	95	95	95	95	ns min	Load DAC Pulse Width
T_{MIN} to T_{MAX}	120	120	150	150	ns min	

NOTES
[1]Maximum possible reference voltage.
[2]Temperature ranges are as follows:
K, L Versions: –40°C to +85°C
B, C Versions: –40°C to +85°C
T, U Versions: –55°C to +125°C
[3]Sample Tested at 25°C to ensure compliance.
[4]Switching characteristics apply for single and dual supply operation.
Specifications subject to change without notice.

ORDERING GUIDE

Model[1]	Temperature Range	Total Unadjusted Error	Package Option[2]
AD7225KN	–40°C to +85°C	±2 LSB	N-24
AD7225LN	–40°C to +85°C	±1 LSB	N-24
AD7225KP	–40°C to +85°C	±2 LSB	P-28A
AD7225LP	–40°C to +85°C	±1 LSB	P-28A
AD7225KR	–40°C to +85°C	±2 LSB	R-24
AD7225LR	–40°C to +85°C	±1 LSB	R-24
AD7225BQ	–40°C to +85°C	±2 LSB	Q-24
AD7225CQ	–40°C to +85°C	±1 LSB	Q-24
AD7225TQ	–55°C to +125°C	±2 LSB	Q-24
AD7225UQ	–55°C to +125°C	±1 LSB	Q-24
AD7225TE	–55°C to +125°C	±2 LSB	E-28A
AD7225UE	–55°C to +125°C	±1 LSB	E-28A

NOTES
[1]To order MIL-STD-883 processed parts, add /883B to part number. Contact your local sales office for military data sheet.
[2]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC.

ABSOLUTE MAXIMUM RATINGS[1]

V_{DD} to AGND ..... –0.3 V, +17 V
V_{DD} to DGND ..... –0.3 V, +17 V
V_{DD} to V_{SS} ..... –0.3 V, +24 V
AGND to DGND ..... –0.3 V, V_{DD}
Digital Input Voltage to DGND ..... –0.3 V, V_{DD} + 0.3 V
V_{REF} to AGND ..... –0.3 V, V_{DD} + 0.3 V
V_{OUT} to AGND[2] ..... V_{SS}, V_{DD}
Power Dissipation (Any Package) to +75°C ..... 500 mW
Derates above 75°C by ..... 2.0 mW/°C
Operating Temperature
Commercial (K, L Versions) ..... –40°C to +85°C
Industrial (B, C Versions) ..... –40°C to +85°C
Extended (T, U Versions) ..... –55°C to +125°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 secs) ..... +300°C

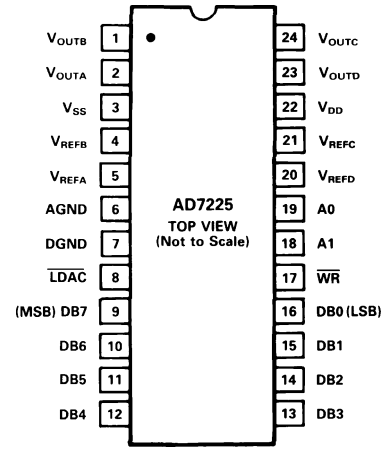
NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Outputs may be shorted to any voltage in the range V_{SS} to V_{DD} provided that the power dissipation of the package is not exceeded. Typical short circuit current for a short to AGND or V_{SS} is 50 mA.

CAUTION

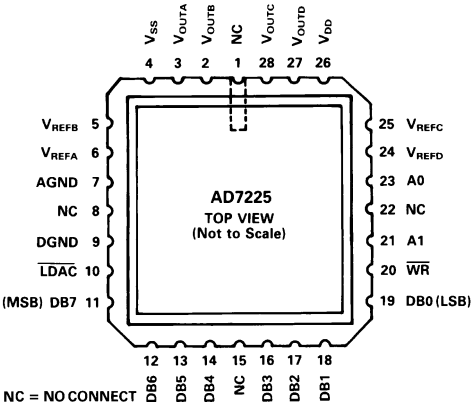
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7225 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS

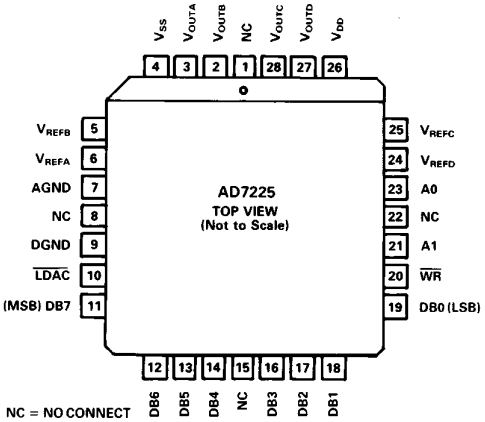
DIP and SOIC



LCCC



PLCC



TERMINOLOGY

TOTAL UNADJUSTED ERROR

Total Unadjusted Error is a comprehensive specification which includes full-scale error, relative accuracy, and zero code error. Maximum output voltage is V_{REF} – 1 LSB (ideal), where 1 LSB (ideal) is $V_{REF}/256$. The LSB size will vary over the V_{REF} range. Hence the zero code error will, relative to the LSB size, increase as V_{REF} decreases. Accordingly, the total unadjusted error, which includes the zero code error, will also vary in terms of LSBs over the V_{REF} range. As a result, total unadjusted error is specified for a fixed reference voltage of +10 V.

RELATIVE ACCURACY

Relative Accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after allowing for zero code error and full-scale error and is normally expressed in LSBs or as a percentage of full-scale reading.

DIFFERENTIAL NONLINEARITY

Differential Nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB max over the operating temperature range ensures monotonicity.

DIGITAL FEEDTHROUGH

Digital Feedthrough is the glitch impulse transferred to the output of the DAC due to a change in its digital input code. It is specified in nV secs and is measured at V_{REF} = 0 V.

DIGITAL CROSSTALK

Digital Crosstalk is the glitch impulse transferred to the output of one converter (not addressed) due to a change in the digital input code to another addressed converter. It is specified in nV secs and is measured at V_{REF} = 0 V.

AC FEEDTHROUGH

AC Feedthrough is the proportion of reference input signal which appears at the output of a converter when that DAC is loaded with all 0s.

CHANNEL-TO-CHANNEL ISOLATION

Channel-to-channel isolation is the proportion of input signal from the reference of one DAC (loaded with all 1s) which appears at the output of one of the other three DACs (loaded with all 0s) The figure given is the worst case for the three other outputs and is expressed as a ratio in dBs.

FULL-SCALE ERROR

Full-Scale Error is defined as:

Measured Value – Zero Code Error – Ideal Value

T_A = 25°C, V_{DD} = +15 V, V_{SS} = –5 V unless otherwise noted.

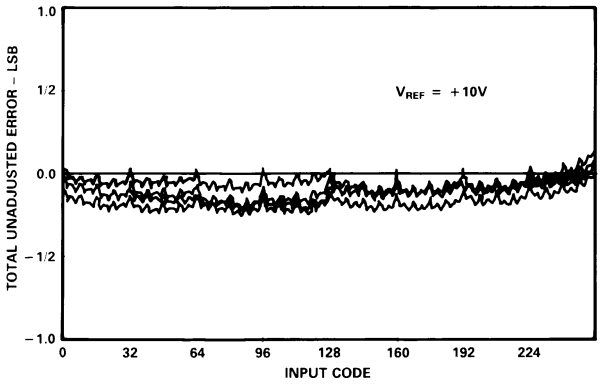


Figure 1. Channel-to-Channel Matching

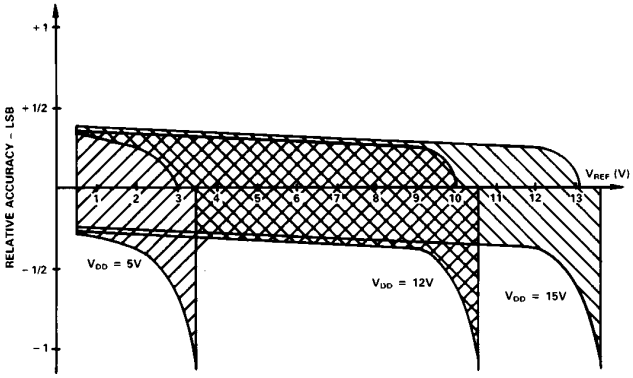


Figure 2. Relative Accuracy vs. V_{REF}

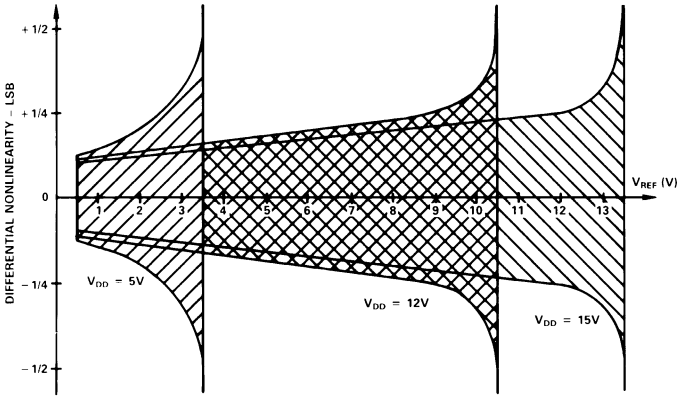


Figure 3. Differential Nonlinearity vs. V_{REF}

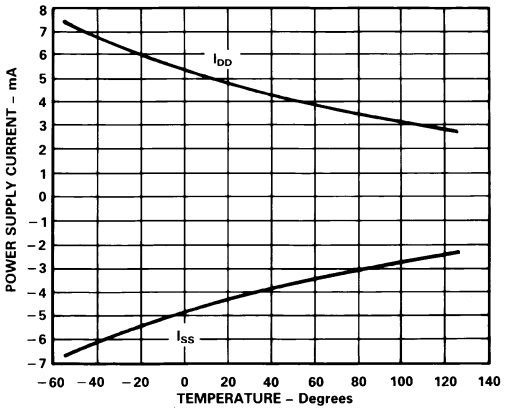


Figure 4. Power Supply Current vs. Temperature

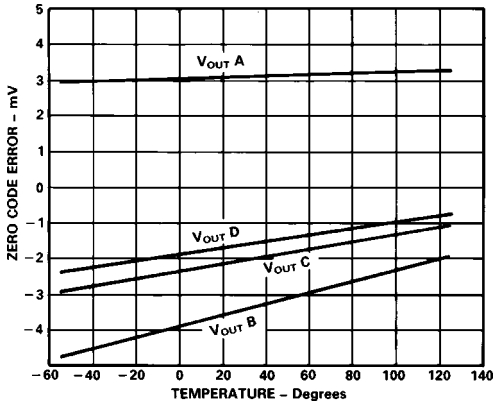


Figure 5. Zero Code Error vs. Temperature

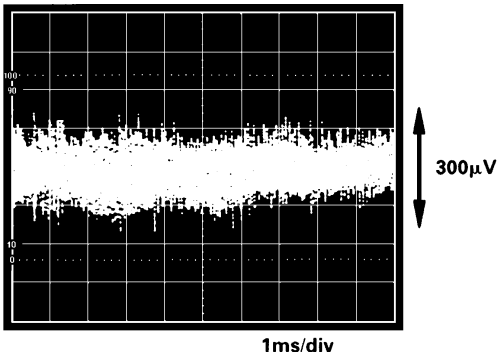


Figure 6. Broadband Noise

CIRCUIT INFORMATION

D/A SECTION

The AD7225 contains four, identical, 8-bit voltage mode digital-to-analog converters. Each D/A converter has a separate reference input. The output voltages from the converters have the same polarity as the reference voltages, allowing single supply operation. A novel DAC switch pair arrangement on the AD7225 allows a reference voltage range from +2 V to +12.5 V on each reference input.

Each DAC consists of a highly stable, thin-film, R-2R ladder and eight high speed NMOS, single-pole, double-throw switches. The simplified circuit diagram for channel A is shown in Figure 7. Note that AGND (Pin 6) is common to all four DACs.

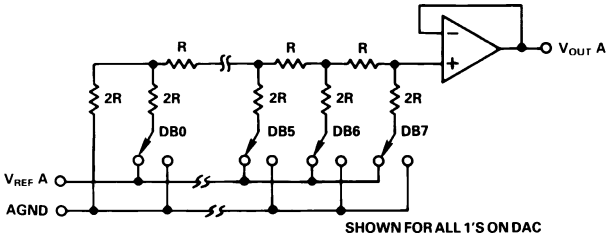


Figure 7. D/A Simplified Circuit Diagram

The input impedance at any of the reference inputs is code dependent and can vary from 11 kΩ minimum to infinity. The lowest input impedance at any reference input occurs when that DAC is loaded with the digital code 01010101. Therefore, it is important that the reference presents a low output impedance under changing load conditions. The nodal capacitance at the reference terminals is also code dependent and typically varies from 15 pF to 35 pF.

Each V_{OUT} pin can be considered as a digitally programmable voltage source with an output voltage of:

$$V_{OUTX} = D_X \bullet V_{REFX}$$

where D_X is fractional representation of the digital input code and can vary from 0 to 255/256.

The output impedance is that of the output buffer amplifier.

OP-AMP SECTION

Each voltage mode D/A converter output is buffered by a unity gain noninverting CMOS amplifier. This buffer amplifier is capable of developing +10 V across a 2 kΩ load and can drive capacitive loads of 3300 pF.

The AD7225 can be operated single or dual supply; operating with dual supplies results in enhanced performance in some parameters which cannot be achieved with single supply operation. In single supply operation (V_{SS} = 0 V = AGND) the sink capability of the amplifier, which is normally 400 μA, is reduced as the output voltage nears AGND. The full sink capability of 400 μA is maintained over the full output voltage range by tying V_{SS} to –5 V. This is indicated in Figure 8.

Settling-time for negative-going output signals approaching AGND is similarly affected by V_{SS}. Negative-going settling-time for single supply operation is longer than for dual supply operation. Positive-going settling-time is not affected by V_{SS}.

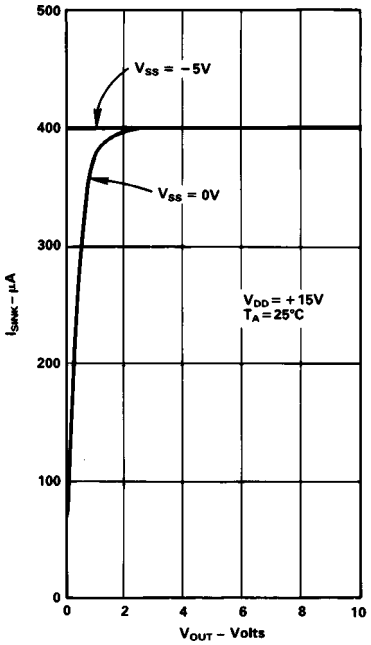


Figure 8. Variation of I_{SINK} with V_{OUT}

Additionally, the negative V_{SS} gives more headroom to the output amplifiers which results in better zero code performance and improved slew rate at the output, than can be obtained in the single supply mode.

DIGITAL SECTION

The AD7225 digital inputs are compatible with either TTL or 5 V CMOS levels. All logic inputs are static protected MOS gates with typical input currents of less than 1 nA. Internal input protection is achieved by an on-chip distributed diode between DGND and each MOS gate. To minimize power supply currents, it is recommended that the digital input voltages be driven as close to the supply rails (V_{DD} and DGND) as practically possible.

INTERFACE LOGIC INFORMATION

The AD7225 contains two registers per DAC, an input register and a DAC register. Address lines A0 and A1 select which input register will accept data from the input port. When the $\overline{WR}$ signal is LOW, the input latches of the selected DAC are transparent. The data is latched into the addressed input register on the rising edge of $\overline{WR}$. Table I shows the addressing for the input registers on the AD7225.

Table I. AD7225 Addressing

A1	A0	Selected Input Register
L	L	DAC A Input Register
L	H	DAC B Input Register
H	L	DAC C Input Register
H	H	DAC D Input Register

Only the data held in the DAC register determines the analog output of the converter. The $\overline{LDAC}$ signal is common to all four DACs and controls the transfer of information from the input registers to the DAC registers. Data is latched into all four DAC registers simultaneously on the rising edge of $\overline{LDAC}$. The $\overline{LDAC}$ signal is level triggered and therefore the DAC registers may be made transparent by tying $\overline{LDAC}$ LOW (in this case the outputs of the converters will respond to the data held in their respective input latches). $\overline{LDAC}$ is an asynchronous signal and is independent of $\overline{WR}$. This is useful in many applications. However, in systems where the asynchronous $\overline{LDAC}$ can occur during a write cycle (or vice versa) care must be taken to ensure that incorrect data is not latched through to the output. In other words, if $\overline{LDAC}$ is activated prior to the rising edge of $\overline{WR}$ (or $\overline{WR}$ occurs during $\overline{LDAC}$), then $\overline{LDAC}$ must stay LOW for t_6 or longer after $\overline{WR}$ goes HIGH to ensure correct data is latched through to the output. Table II shows the truth table for AD7225 operation. Figure 9 shows the input control logic for the part and the write cycle timing diagram is given in Figure 10.

Table II. AD7225 Truth Table

$\overline{WR}$	$\overline{LDAC}$	Function
H	H	No Operation. Device not selected
L	H	Input Register of Selected DAC Transparent
↓	H	Input Register of Selected DAC Latched
H	L	All Four DAC Registers Transparent (i.e. Outputs respond to data held in respective input registers)
		Input Registers are Latched
H	↓	All Four DAC Registers Latched
L	L	DAC Registers and Selected Input Register Transparent Output follows Input Data for Selected Channel.

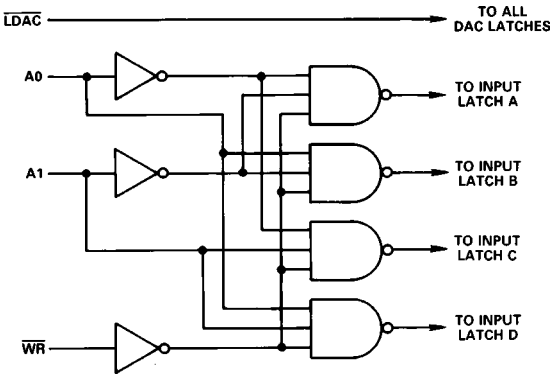


Figure 9. Input Control Logic

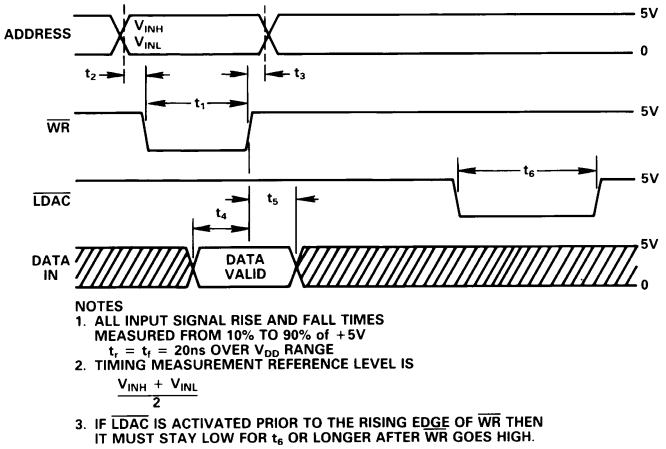


Figure 10. Write Cycle Timing Diagram

GROUND MANAGEMENT AND LAYOUT

Since the AD7225 contains four reference inputs which can be driven from ac sources (see AC REFERENCE SIGNAL section) careful layout and grounding is important to minimize analog crosstalk between the four channels. The dynamic performance of the four DACs depends upon the optimum choice of board layout. Figure 11 shows the relationship between input

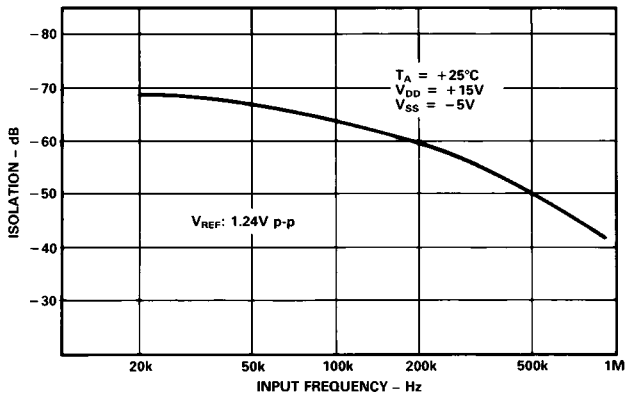


Figure 11. Channel-to-Channel Isolation

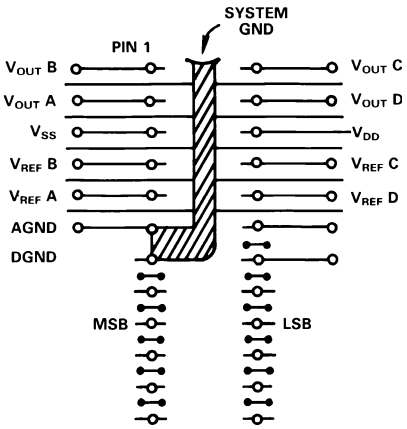


Figure 12. Suggested PCB Layout for AD7225. Layout Shows Component Side (Top View)

frequency and channel-to-channel isolation. Figure 12 shows a printed circuit board layout which is aimed at minimizing crosstalk and feedthrough. The four input signals are screened by AGND. V_{REF} was limited to between 2 V and 3.24 V to avoid slew rate limiting effects from the output amplifier during measurements.

SPECIFICATION RANGES

For the AD7225 to operate to rated specifications, its input reference voltage must be at least 4 V below the V_{DD} power supply voltage. This voltage differential is the overhead voltage required by the output amplifiers.

The AD7225 is specified to operate over a V_{DD} range from +12 V ± 5% to +15 V ±10% (i.e., from +11.4 V to +16.5 V) with a V_{SS} of –5 V ±10%. Operation is also specified for a single +15 V ± 5% V_{DD} supply. Applying a V_{SS} of –5 V results in improved zero code error, improved output sink capability with outputs near AGND and improved negative going settling time.

Performance is specified over a wide range of reference voltages from 2 V to (V_{DD} – 4 V) with dual supplies. This allows a range of standard reference generators to be used such as the AD580, a +2.5 V bandgap reference and the AD584, a precision +10 V reference. Note that an output voltage range of 0 V to +10 V requires a nominal +15 V ± 5% power supply voltage.

UNIPOLAR OUTPUT OPERATION

This is the basic mode of operation for each channel of the AD7225, with the output voltage having the same positive polarity as V_{REF}. The AD7225 can be operated single supply (V_{SS} = AGND) or with positive/negative supplies (see op-amp section which outlines the advantages of having negative V_{SS}). Connections for the unipolar output operation are shown in Figure 13. The voltage at any of the reference inputs must never be negative with respect to DGND. Failure to observe this precaution may cause parasitic transistor action and possible device destruction. The code table for unipolar output operation is shown in Table III.

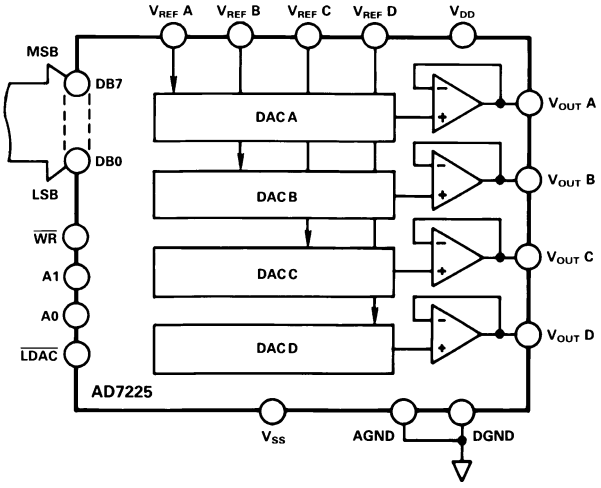


Figure 13. Unipolar Output Circuit

Table III. Unipolar Code Table

DAC Latch Contents MSB LSB	Analog Output
1 1 1 1 1 1 1 1	$+V_{REF}\left(\frac{255}{256}\right)$
1 0 0 0 0 0 0 1	$+V_{REF}\left(\frac{129}{256}\right)$
1 0 0 0 0 0 0 0	$+V_{REF}\left(\frac{128}{256}\right)=+\frac{V_{REF}}{2}$
0 1 1 1 1 1 1 1	$+V_{REF}\left(\frac{127}{256}\right)$
0 0 0 0 0 0 0 1	$+V_{REF}\left(\frac{1}{256}\right)$
0 0 0 0 0 0 0 0	*0 V*

Note: $1\ LSB = (V_{REF})(2^{-8}) = V_{REF}\left(\frac{1}{256}\right)$

BIPOLAR OUTPUT OPERATION

Each of the DACs of the AD7225 can be individually configured to provide bipolar output operation. This is possible using one external amplifier and two resistors per channel. Figure 14 shows a circuit used to implement offset binary coding (bipolar operation) with DAC A of the AD7225. In this case

$$V_{OUT} = \left(1+\frac{R2}{R1}\right)\cdot(D_A V_{REF}) - \left(\frac{R2}{R1}\right)\cdot(V_{REF})$$

With $R1 = R2$

$$V_{OUT} = (2\ D_A - 1) \bullet V_{REF}$$

where D_A is a fractional representation of the digital word in latch A. ($0 \le D_A \le 255/256$)

Mismatch between R1 and R2 causes gain and offset errors and, therefore, these resistors must match and track over temperature. Once again the AD7225 can be operated in single supply or from positive/negative supplies. Table IV shows the digital code versus output voltage relationship for the circuit of Figure 14 with R1 = R2.

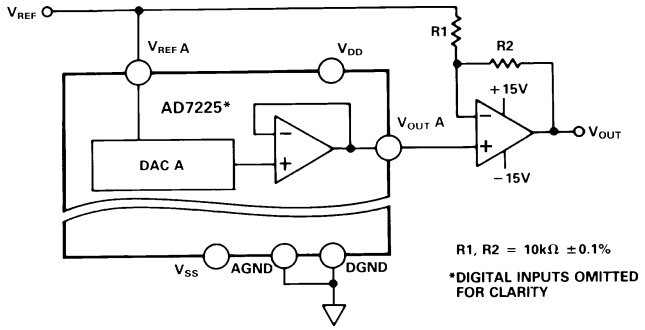


Figure 14. AD7225 Bipolar Output Circuit

Table IV. Bipolar (Offset Binary) Code Table

DAC Latch Contents MSB	LSB	Analog Output
1 1 1 1	1 1 1 1	$+V_{REF}\left(\frac{127}{128}\right)$
1 0 0 0	0 0 0 1	$+V_{REF}\left(\frac{1}{128}\right)$
1 0 0 0	0 0 0 0	*0 V*
0 1 1 1	1 1 1 1	$-V_{REF}\left(\frac{1}{128}\right)$
0 0 0 0	0 0 0 1	$-V_{REF}\left(\frac{127}{128}\right)$
0 0 0 0	0 0 0 0	$-V_{REF}\left(\frac{128}{128}\right)=-V_{REF}$

AGND BIAS

The AD7225 AGND pin can be biased above system GND (AD7225 DGND) to provide an offset "zero" analog output voltage level. Figure 15 shows a circuit configuration to achieve this for channel A of the AD7225. The output voltage, V_{OUT} A, can be expressed as:

$$V_{OUT}\,A = V_{BIAS} + D_A\,(V_{IN})$$

where D_A is a fractional representation of the digital word in DAC latch A. ($0 \le D_A \le 255/256$).

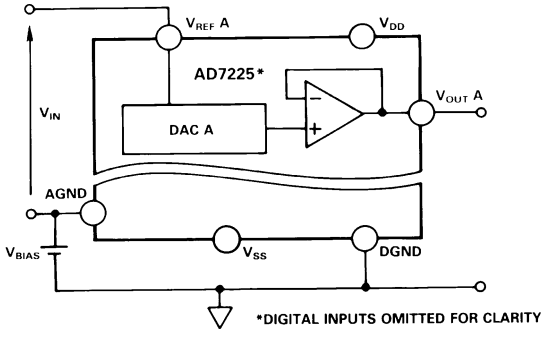


Figure 15. AGND Bias Circuit

For a given V_{IN}, increasing AGND above system GND will reduce the effective V_{DD}–V_{REF} which must be at least 4 V to ensure specified operation. Note that because the AGND pin is common to all four DACs, this method biases up the output voltages of all the DACs in the AD7225. Note that V_{DD} and V_{SS} of the AD7225 should be referenced to DGND.

AC REFERENCE SIGNAL

In some applications it may be desirable to have ac reference signals. The AD7225 has multiplying capability within the upper (V_{DD} – 4 V) and lower (2 V) limits of reference voltage when operated with dual supplies. Therefore ac signals need to be ac coupled and biased up before being applied to the reference inputs. Figure 16 shows a sine wave signal applied to V_{REF} A. For input signal frequencies up to 50 kHz the output distortion typically remains less than 0.1%. The typical 3 dB bandwidth figure for small signal inputs is 800 kHz.

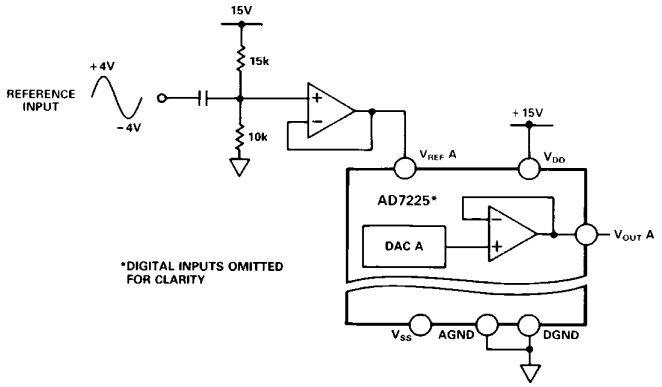


Figure 16. Applying an AC Signal to the AD7225

APPLICATIONS

PROGRAMMABLE TRANSVERSAL FILTER

A discrete-time filter may be described by either multiplication in the frequency domain or convolution in the time domain i.e.

$$Y(\omega) = H(\omega)X(\omega) \quad or \quad y_n = \sum_{k=1}^{N} h_{kXn-k+1}$$

The convolution sum may be implemented using the special structure known as the transversal filter (Figure 17). Basically, it consists of an N-stage delay line with N taps weighted by N coefficients, the resulting products being accumulated to form the output. The tap weights or coefficients h_k are actually the nonzero elements of the impulse response and therefore determine the filter transfer function. A particular filter frequency response is realized by setting the coefficients to the appropriate values. This property leads to the implementation of transversal filters whose frequency response is programmable.

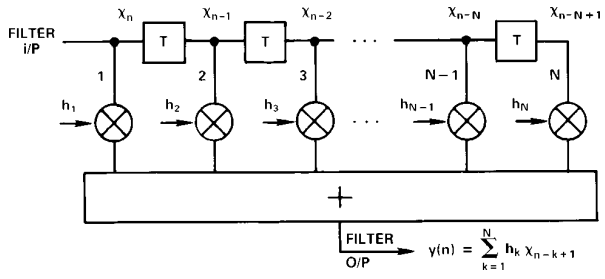


Figure 17. Transversal Filter

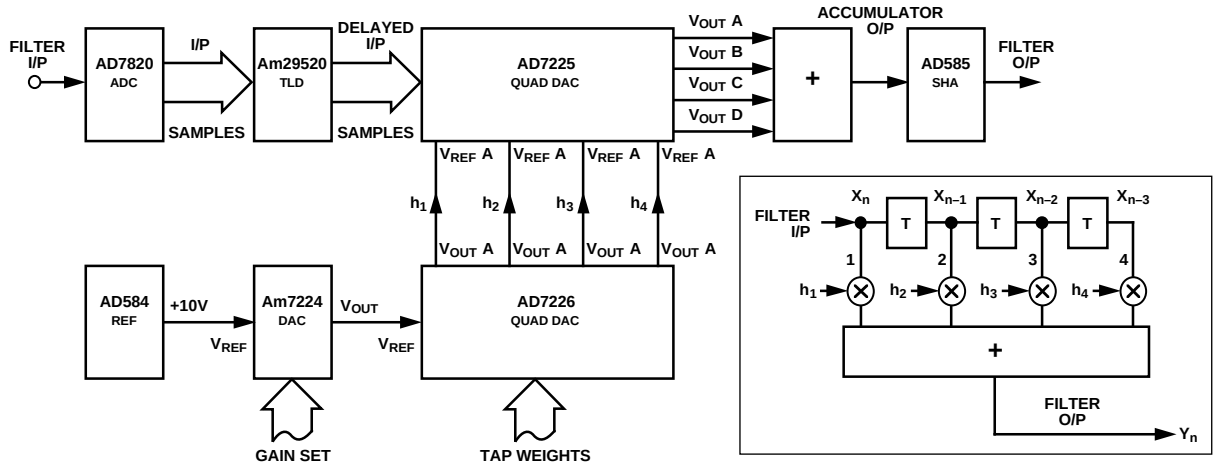


Figure 18. Programmable Transversal Filter

A 4-tap programmable transversal filter may be implemented using the AD7225 (Figure 18). The input signal is first sampled and converted to allow the tapped delay line function to be provided by the Am29520. The multiplication of delayed input samples by fixed, programmable up weights is accomplished by the AD7225, the four coefficients or reference inputs being set by the digital codes stored in the AD7226. The resultant products are accumulated to yield the convolution sum output sample which is held by the AD585.

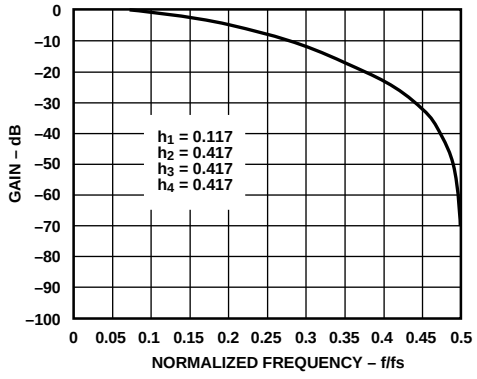


Figure 19. Predicted (Theoretical) Response

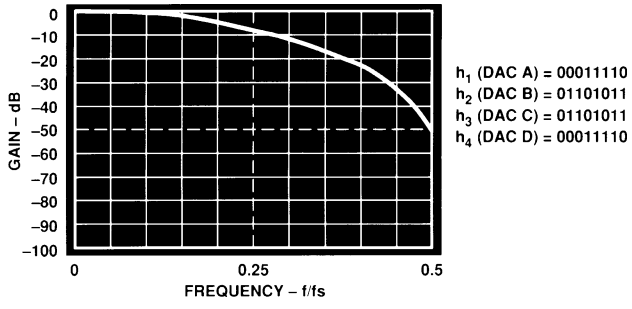


Figure 20. Actual Response

Low pass, bandpass and high pass filters may be synthesized using this arrangement. The particular up weights needed for any desired transfer function may be obtained using the standard Remez Exchange Algorithm. Figure 19 shows the theoretical low pass frequency response produced by a 4-tap transversal filter with the coefficients indicated. Although the theoretical prediction does not take into account the quantization of the input samples and the truncation of the coefficients, nevertheless, there exists a good correlation with the actual performance of the transversal filter (Figure 20).

DIGITAL WORD MULTIPLICATION

Since each DAC of the AD7225 has a separate reference input, the output of one DAC can be used as the reference input for another. This means that multiplication of digital words can be performed (with the result given in analog form). For example, if the output from DACA is applied to V_{REF} B then the output from DACB, V_{OUT} B, can be expressed as:

$$V_{OUT}\ B = D_A \bullet D_B \bullet V_{REF}\ A$$

where D_A and D_B are the fractional representations of the digital words in DAC latches A and B respectively.

If $D_A = D_B = D$ then the result is $D^2 \bullet V_{REF}$ A

In this manner, the four DACs can be used on their own or in conjunction with an external summing amplifier to generate complex waveforms. Figure 21 shows one such application. In this case the output waveform, Y, is represented by:

$$Y = -(x^4 + 2x^3 + 3x^2 + 2x + 4) \bullet V_{IN}$$

where x is the digital code which is applied to all four DAC latches.

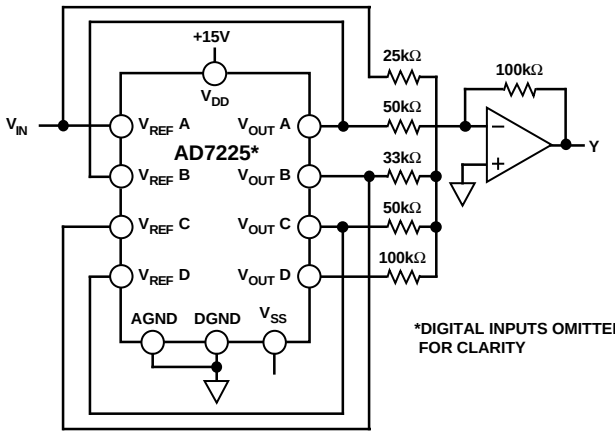


Figure 21. Complex Waveform Generation

MICROPROCESSOR INTERFACE

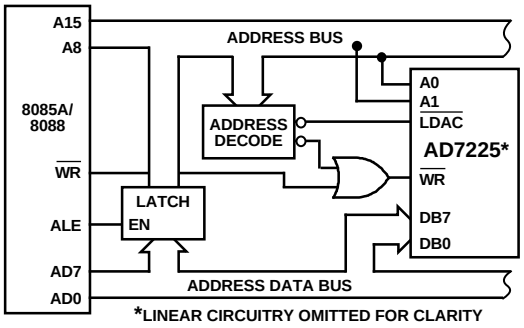


Figure 22. AD7225 to 8085A/8088 Interface, Double-Buffered Mode

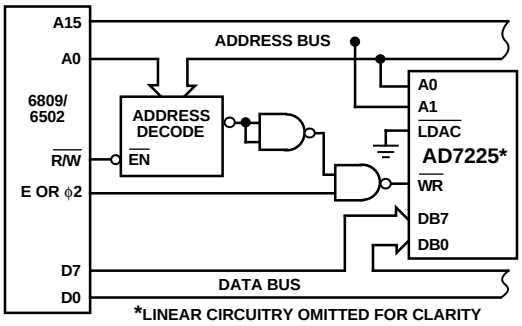


Figure 23. AD7225 to 6809/6502 Interface, Single-Buffered Mode

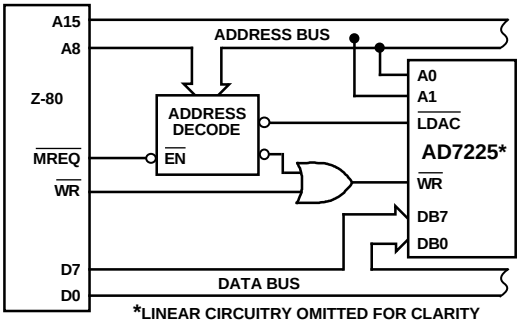


Figure 24. AD7225 to Z-80 Interface, Double-Buffered Mode

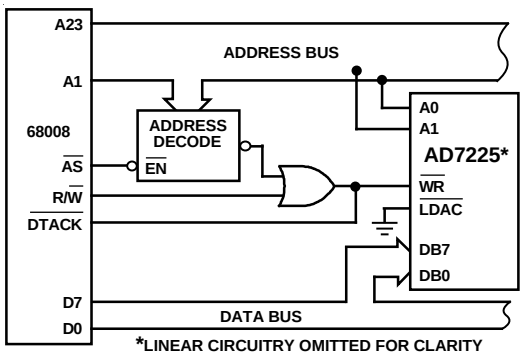


Figure 25. AD7225 to 68008 Interface, Single-Buffered Mode

V_{SS} GENERATION

Operating the AD7225 from dual supplies results in enhanced performance over single supply operation on a number of parameters as previously outlined. Some applications may require this enhanced performance, but may only have a single power supply rail available. The circuit of Figure 26 shows a method of generating a negative voltage using one CD4049, operated from a V_{DD} of +15 V. Two inverters of the hex inverter chip are used as an oscillator. The other four inverters are in parallel and used as buffers for higher output current. The square-wave output is level translated to a negative-going signal, then rectified and filtered. The circuit configuration shown will provide an output voltage of –5.1 V for current loadings in the range 0.5 mA to 9 mA. This will satisfy the AD7225 I_{SS} requirement over the commercial operating temperature range.

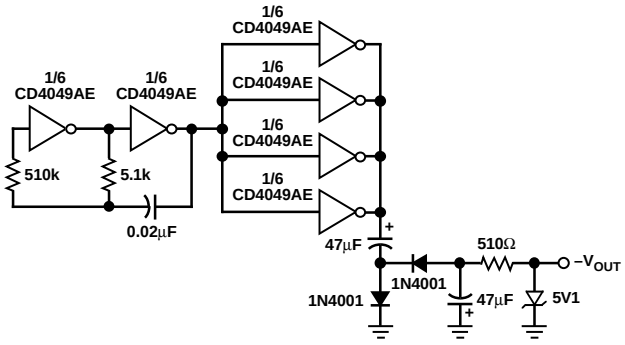
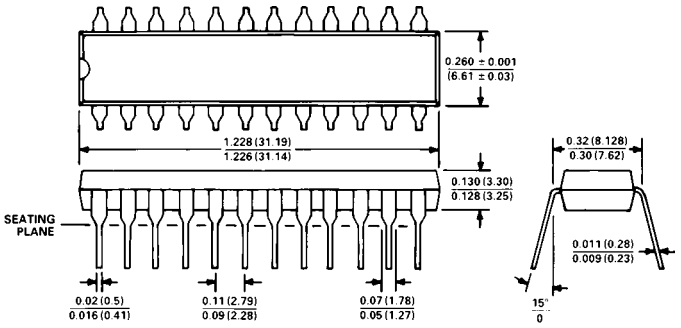


Figure 26. V_{SS} Generation Circuit

OUTLINE DIMENSIONS

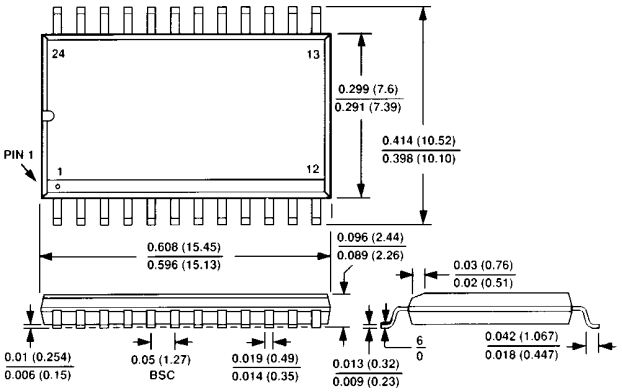
Dimensions shown in inches and (mm).

24-Pin Plastic (N-24)



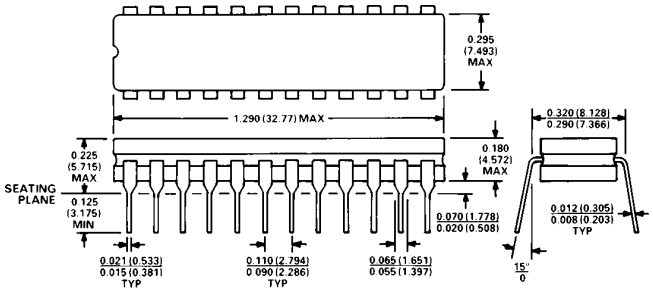
NOTES
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
2. PLASTIC LEADS WILL BE EITHER SOLDER DIPPED OR TIN LEAD PLATED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

24-Lead SOIC (R-24)



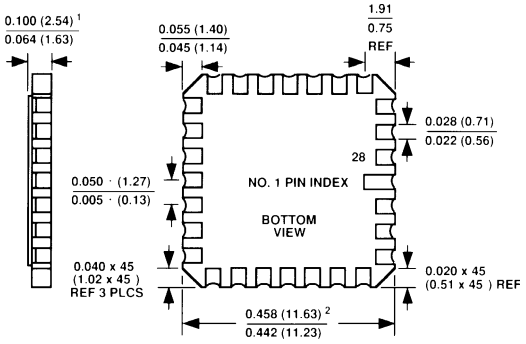
1. LEAD NO. 1 IDENTIFIED BY A DOT.
2. SOIC LEADS WILL BE EITHER TIN PLATED OR SOLDER DIPPED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS

24-Pin Cerdip (Q-24)



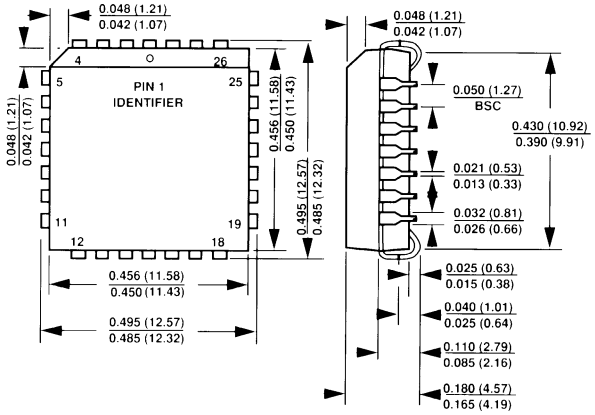
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
2. CERDIP LEADS WILL BE EITHER TIN PLATED OR SOLDER DIPPED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

28-Terminal Leadless Ceramic Chip Carrier (E-28A)



NOTES
1. THIS DIMENSION CONTROLS THE OVERALL PACKAGE THICKNESS.
2. APPLIES TO ALL FOUR SIDES.
3. ALL TERMINALS ARE GOLD PLATED.

28-Lead PLCC (P-28A)



C927a–5–5/86

PRINTED IN U.S.A.