Low Power, High Speed Rail-to-Rail Input/Output Amplifier

AD8029/AD8030/AD8040

FEATURES

Low power
- **1.3 mA supply current/amplifier**

High speed
- **125 MHz, –3 dB bandwidth (G = +1)**
- **60 V/µs slew rate**
- **80 ns settling time to 0.1%**

Rail-to-rail input and output
- **No phase reversal, inputs 200 mV beyond rails**

Wide supply range: 2.7 V to 12 V
Offset voltage: 6 mV max
Low input bias current
- **+0.7 µA to –1.5 µA**

Small packaging
- **SOIC-8, SC70-6, SOT23-8, SOIC-14, TSSOP-14**

APPLICATIONS

Battery-powered instrumentation
Filters
A-to-D drivers
Buffering

CONNECTION DIAGRAMS

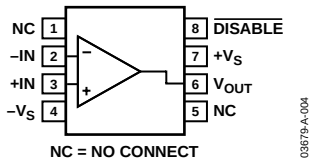

Figure 1. SOIC-8 (R)

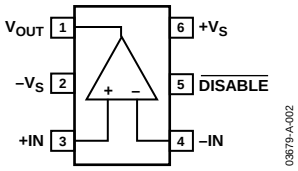

Figure 2. SC70-6 (KS)

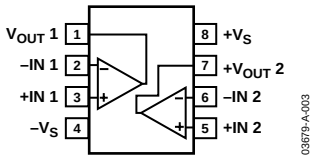

Figure 3. SOIC-8(R) and SOT23-8 (RJ)

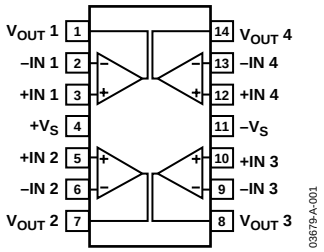

Figure 4. SOIC-14 (R) and TSSOP-14 (RU)

GENERAL DESCRIPTION

The AD8029 (single), AD8030 (dual), and AD8040 (quad) are rail-to-rail input and output high speed amplifiers with a quiescent current of only 1.3 mA per amplifier. Despite their low power consumption, the amplifiers provide excellent performance with 125 MHz small signal bandwidth and 60 V/µs slew rate. ADI's proprietary XFCB process enables high speed and high performance on low power.

This family of amplifiers exhibits true single-supply operation with rail-to-rail input and output performance for supply voltages ranging from 2.7 V to 12 V. The input voltage range extends 200 mV beyond each rail without phase reversal. The dynamic range of the output extends to within 40 mV of each rail.

The AD8029/AD8030/AD8040 provide excellent signal quality with minimal power dissipation. At G = +1, SFDR is –72 dBc at 1 MHz and settling time to 0.1% is only 80 ns. Low distortion and fast settling performance make these amplifiers suitable drivers for single-supply A/D converters.

The versatility of the AD8029/AD8030/AD8040 allows the user to operate the amplifiers on a wide range of supplies while consuming less than 6.5 mW of power. These features extend the operation time in applications ranging from battery-powered systems with large bandwidth requirements to high speed systems where component density requires lower power dissipation.

The AD8029/AD8030 are the only low power, rail-to-rail input and output high speed amplifiers available in SOT23 and SC70 micro packages. The amplifiers are rated over the extended industrial temperature range, –40°C to +125°C.

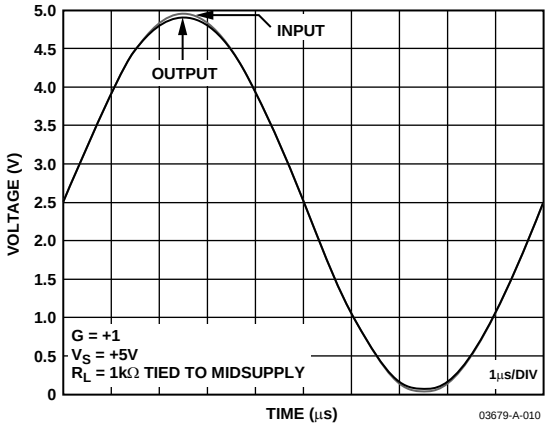

Figure 5. Rail-to-Rail Response

Rev. A

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TABLE OF CONTENTS

REVISION HISTORY

Revision A
11/03—Data Sheet Changed from Rev. 0 to Rev. A

Change	Page
Added AD8040 part	Universal
Change to Figure 5	1
Changes to Specifications	3
Changes to Figures 10–12	7
Change to Figure 14	8
Changes to Figures 20 and 21	9
Inserted new Figure 36	11
Change to Figure 40	12
Inserted new Figure 41	12
Added Output Loading Sensitivity section	16
Changes to Table 5	17
Changes to Power Supply Bypassing section	18
Changes to Ordering Guide	20

SPECIFICATIONS

SPECIFICATIONS WITH ±5 V SUPPLY

Table 1. V_S = ±5 V @ T_A = 25°C, G = +1, R_L = 1 kΩ to ground, unless otherwise noted. All specifications are per amplifier.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Bandwidth	G = +1, V_O = 0.1 V p-p	80	125		MHz
	G = +1, V_O = 2 V p-p	14	19		MHz
Bandwidth for 0.1 dB Flatness	G = +2, V_O = 0.1 V p-p		6		MHz
Slew Rate	G = +1, V_O = 2 V Step		62		V/µs
	G = –1, V_O = 2 V Step		63		V/µs
Settling Time to 0.1%	G = +2, V_O = 2 V Step		80		ns
NOISE/DISTORTION PERFORMANCE					
Spurious Free Dynamic Range (SFDR)	f_C = 1 MHz, V_O = 2 V p-p		–74		dBc
	f_C = 5 MHz, V_O = 2 V p-p		–56		dBc
Input Voltage Noise	f = 100 kHz		16.5		nV/√Hz
Input Current Noise	f = 100 kHz		1.1		pA/√Hz
Crosstalk (AD8030/AD8040)	f = 5 MHz, V_{IN} = 2 V p-p		–79		dB
DC PERFORMANCE					
Input Offset Voltage	PNP Active, V_{CM} = 0 V		1.6	5	mV
	NPN Active, V_{CM} = 4.5 V		2	6	mV
Input Offset Voltage Drift	T_{MIN} to T_{MAX}		30		µV/°C
Input Bias Current[1]	NPN Active, V_{CM} = 4.5 V		0.7	1.3	µA
	T_{MIN} to T_{MAX}		1		µA
	PNP Active, V_{CM} = 0 V		–1.7	–2.8	µA
	T_{MIN} to T_{MAX}		2		µA
Input Offset Current			±0.1	±0.9	µA
Open-Loop Gain	V_o = ±4.0 V	65	74		dB
INPUT CHARACTERISTICS					
Input Resistance			6		MΩ
Input Capacitance			2		pF
Input Common-Mode Voltage Range			–5.2 to +5.2		V
Common-Mode Rejection Ratio	V_{CM} = –4.5 V to +3 V, R_L = 10 kΩ	80	90		dB
$\overline{\text{DISABLE}}$ PIN (AD8029)					
$\overline{\text{DISABLE}}$ Low Voltage			$–V_S$ + 0.8		V
$\overline{\text{DISABLE}}$ Low Current			–6.5		µA
$\overline{\text{DISABLE}}$ High Voltage			$–V_S$ + 1.2		V
$\overline{\text{DISABLE}}$ High Current			0.2		µA
Turn-Off Time	50% of $\overline{\text{DISABLE}}$ to <10% of Final V_O, V_{IN} = –1 V, G = –1		150		ns
Turn-On Time	50% of $\overline{\text{DISABLE}}$ to <10% of Final V_O, V_{IN} = –1 V, G = –1		85		ns
OUTPUT CHARACTERISTICS					
Output Overdrive Recovery Time (Rising/Falling Edge)	V_{IN} = +6 V to –6 V, G = –1		55/45		ns
Output Voltage Swing	R_L = 1 kΩ	$–V_S$ + 0.22		$+V_S$ – 0.22	V
	R_L = 10 kΩ	$–V_S$ + 0.05		$+V_S$ – 0.05	V
Short-Circuit Current	Sinking and Sourcing		170/160		mA
Off Isolation (AD8029)	V_{IN} = 0.1 V p-p, f = 1 MHz, $\overline{\text{DISABLE}}$ = Low		–55		dB
Capacitive Load Drive	30% Overshoot		20		pF
POWER SUPPLY					
Operating Range		2.7		12	V
Quiescent Current/Amplifier			1.4	1.5	mA
Quiescent Current (Disabled)	$\overline{\text{DISABLE}}$ = Low		150	200	µA
Power Supply Rejection Ratio	V_s ± 1 V	73	80		dB

[1] Plus, +, (or no sign) indicates current into pin; minus (–) indicates current out of pin.

SPECIFICATIONS WITH +5 V SUPPLY

Table 2. V_S = 5 V @ T_A = 25°C, G = +1, R_L = 1 kΩ to midsupply, unless otherwise noted. All specifications are per amplifier.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = +1, V_O = 0.1 V p-p	80	120		MHz
	G = +1, V_O = 2 V p-p	13	18		MHz
Bandwidth for 0.1 dB Flatness	G = +2, V_O = 0.1 V p-p		6		MHz
Slew Rate	G = +1, V_O = 2 V Step		55		V/µs
	G = −1, V_O = 2 V Step		60		V/µs
Settling Time to 0.1%	G = +2, V_O = 2 V Step		82		ns
NOISE/DISTORTION PERFORMANCE					
Spurious Free Dynamic Range (SFDR)	f_C = 1 MHz, V_O = 2 V p-p		−73		dBc
	f_C = 5 MHz, V_O = 2 V p-p		−55		dBc
Input Voltage Noise	f = 100 kHz		16.5		nV/√Hz
Input Current Noise	f = 100 kHz		1.1		pA/√Hz
Crosstalk (AD8030/AD8040)	f = 5 MHz, V_{IN} = 2 V p-p		-79		dB
DC PERFORMANCE					
Input Offset Voltage	PNP Active, V_{CM} = 2.5 V		1.4	5	mV
	NPN Active, V_{CM} = 4.5 V		1.8	6	mV
Input Offset Voltage Drift	T_{MIN} to T_{MAX}		25		µV/°C
Input Bias Current[1]	NPN Active, V_{CM} = 4.5 V		0.8	1.2	µA
	T_{MIN} to T_{MAX}		1		µA
	PNP Active, V_{CM} = 2.5 V		−1.8	−2.8	µA
	T_{MIN} to T_{MAX}		2		µA
Input Offset Current			±0.1	±0.9	µA
Open-Loop Gain	V_o = 1 V to 4 V	65	74		dB
INPUT CHARACTERISTICS					
Input Resistance			6		MΩ
Input Capacitance			2		pF
Input Common-Mode Voltage Range			−0.2 to +5.2		V
Common-Mode Rejection Ratio	V_{CM} = 0.25 V to 2 V, R_L = 10 kΩ	80	90		dB
$\overline{\text{DISABLE}}$ PIN (AD8029)					
$\overline{\text{DISABLE}}$ Low Voltage			$-V_S$ + 0.8		V
$\overline{\text{DISABLE}}$ Low Current			−6.5		µA
$\overline{\text{DISABLE}}$ High Voltage			$-V_S$ + 1.2		V
$\overline{\text{DISABLE}}$ High Current			0.2		µA
Turn-Off Time	50% of $\overline{\text{DISABLE}}$ to <10% of Final V_O, V_{IN} = −1 V, G = −1		155		ns
Turn-On Time	50% of $\overline{\text{DISABLE}}$ to <10% of Final V_O, V_{IN} = −1 V, G = −1		90		ns
OUTPUT CHARACTERISTICS					
Overdrive Recovery Time (Rising/Falling Edge)	V_{IN} = −1 V to +6 V, G = −1		45/50		ns
Output Voltage Swing	R_L = 1 kΩ	$-V_S$ + 0.17		$+V_S$ − 0.17	V
	R_L = 10 kΩ	$-V_S$ + 0.04		$+V_S$ − 0.04	V
Short-Circuit Current	Sinking and Sourcing		95/60		mA
Off Isolation (AD8029)	V_{in} = 0.1 V p-p, f = 1 MHz, $\overline{\text{DISABLE}}$ = Low		−55		dB
Capacitive Load Drive	30% Overshoot		15		pF
POWER SUPPLY					
Operating Range		2.7		12	V
Quiescent Current/Amplifier			1.3	1.5	mA
Quiescent Current (Disabled)	$\overline{\text{DISABLE}}$ = Low		140	200	µA
Power Supply Rejection Ratio	V_S ± 1 V	73	80		dB

[1] Plus, +, (or no sign) indicates current into pin; minus (−) indicates current out of pin.

SPECIFICATIONS WITH +3 V SUPPLY

Table 3. V_S = +3 V @ T_A = 25°C, G = +1, R_L = 1 kΩ to midsupply, unless otherwise noted. All specifications are per amplifier.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = +1, V_O = 0.1 V p-p	80	112		MHz
	G = +1, V_O = 2 V p-p	13	18		MHz
Bandwidth for 0.1 dB Flatness	G = +2, V_O = 0.1 V p-p		6		MHz
Slew Rate	G = +1, V_O = 2 V Step		55		V/µs
	G = −1, V_O = 2 V Step		57		V/µs
Settling Time to 0.1%	G = +2, V_O = 2 V Step		110		ns
NOISE/DISTORTION PERFORMANCE					
Spurious Free Dynamic Range (SFDR)	f_C = 1 MHz, V_O = 2 V p-p		−72		dBc
	f_C = 5 MHz, V_O = 2 V p-p		−60		dBc
Input Voltage Noise	f = 100 kHz		16.5		nV/√Hz
Input Current Noise	f = 100 kHz		1.1		pA/√Hz
Crosstalk (AD8030/AD8040)	f = 5 MHz, V_{IN} = 2 V p-p		-80		dB
DC PERFORMANCE					
Input Offset Voltage	PNP Active, V_{CM} = 1.5 V		1.1	5	mV
	NPN Active, V_{CM} = 2.5 V		1.6	6	mV
Input Offset Voltage Drift	T_{MIN} to T_{MAX}		24		µV/°C
Input Bias Current[1]	NPN Active, V_{CM} = 2.5 V		0.7	1.2	µA
	T_{MIN} to T_{MAX}		1		µA
Input Bias Current[1]	PNP Active, V_{CM} = 1.5 V		−1.5	−2.5	µA
	T_{MIN} to T_{MAX}		1.6		µA
Input Offset Current			±0.1	±0.9	µA
Open-Loop Gain	V_o = 0.5 V to 2.5 V	64	73		dB
INPUT CHARACTERISTICS					
Input Resistance			6		MΩ
Input Capacitance			2		pF
Input Common-Mode Voltage Range			−0.2 to +3.2		V
Common-Mode Rejection Ratio	V_{CM} = 0.25 V to 1.25 V, R_L = 10 kΩ	78	88		dB
$\overline{\text{DISABLE}}$ PIN (AD8029)					
$\overline{\text{DISABLE}}$ Low Voltage			$-V_S$ + 0.8		V
$\overline{\text{DISABLE}}$ Low Current			−6.5		µA
$\overline{\text{DISABLE}}$ High Voltage			$-V_S$ + 1.2		V
$\overline{\text{DISABLE}}$ High Current			0.2		µA
Turn-Off Time	50% of $\overline{\text{DISABLE}}$ to <10% of Final V_O, V_{IN} = −1 V, G = −1		165		ns
Turn-On Time	50% of $\overline{\text{DISABLE}}$ to <10% of Final V_O, V_{IN} = −1 V, G = −1		95		ns
OUTPUT CHARACTERISTICS					
Output Overdrive Recovery Time (Rising/Falling Edge)	V_{IN} = −1 V to +4 V, G = −1		75/100		ns
Output Voltage Swing	R_L = 1 kΩ	$-V_S$ + 0.09		$+V_S$ − 0.09	V
	R_L = 10 kΩ	$-V_S$ + 0.04		$+V_S$ − 0.04	V
Short-Circuit Current	Sinking and Sourcing		80/40		mA
Off Isolation (AD8029)	V_{IN} = 0.1 V p-p, f = 1 MHz, $\overline{\text{DISABLE}}$ = Low		−55		dB
Capacitive Load Drive	30% Overshoot		10		pF
POWER SUPPLY					
Operating Range		2.7		12	V
Quiescent Current/Amplifier			1.3	1.4	mA
Quiescent Current (Disabled)	$\overline{\text{DISABLE}}$ = Low		145	200	µA
Power Supply Rejection Ratio	V_S ± 1 V	70	76		dB

[1] Plus, +, (or no sign) indicates current into pin; minus (–) indicates current out of pin.

ABSOLUTE MAXIMUM RATINGS

Table 4. AD8029/AD8030/AD8040 Stress Ratings

Parameter	Rating
Supply Voltage	12.6 V
Power Dissipation	See Figure 6
Common-Mode Input Voltage	$\pm V_S \pm 0.5$ V
Differential Input Voltage	±1.8 V
Storage Temperature	–65°C to +125°C
Operating Temperature Range	–40°C to +125°C
Lead Temperature Range (Soldering 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation in the AD8029/AD8030/AD8040 package is limited by the associated rise in junction temperature (T_J) on the die. The plastic encapsulating the die locally reaches the junction temperature. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the AD8029/AD8030/AD8040. Exceeding a junction temperature of 175°C for an extended period can result in changes in silicon devices, potentially causing failure.

The still-air thermal properties of the package and PCB (θ_{JA}), ambient temperature (T_A), and the total power dissipated in the package (P_D) determine the junction temperature of the die. The junction temperature can be calculated as

$$T_J = T_A + (P_D \times \theta_{JA})$$

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). Assuming the load (R_L) is referenced to midsupply, the total drive power is $V_S/2 \times I_{OUT}$, some of which is dissipated in the package and some in the load ($V_{OUT} \times I_{OUT}$). The difference between the total drive power and the load power is the drive power dissipated in the package.

$$P_D = \textit{Quiescent Power} + (\textit{Total Drive Power} - \textit{Load Power})$$

$$P_D = (V_S \times I_S) + \left(\frac{V_S}{2} \times \frac{V_{OUT}}{R_L}\right) - \frac{{V_{OUT}}^2}{R_L}$$

RMS output voltages should be considered. If R_L is referenced to V_S–, as in single-supply operation, then the total drive power is $V_S \times I_{OUT}$.

If the rms signal levels are indeterminate, consider the worst case, when $V_{OUT} = V_S/4$ for R_L to midsupply:

$$P_D = (V_S \times I_S) + \frac{(V_S/4)^2}{R_L}$$

In single-supply operation with R_L referenced to V_S–, worst case is $V_{OUT} = V_S/2$.

Airflow will increase heat dissipation, effectively reducing θ_{JA}. Also, more metal directly in contact with the package leads from metal traces, through holes, ground, and power planes will reduce the θ_{JA}. Care must be taken to minimize parasitic capacitances at the input leads of high speed op amps, as discussed in the PCB Layout section.

Figure 6 shows the maximum safe power dissipation in the package versus the ambient temperature for the SOIC-8 (125°C/W), SOT23-8 (160°C/W), SOIC-14 (90°C/W), TSSOP-14 (120°C/W), and SC70-6 (208°C/W) packages on a JEDEC standard 4-layer board. θ_{JA} values are approximations.

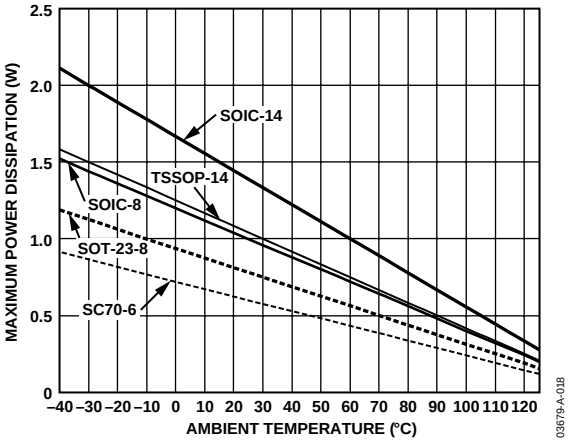


Figure 6. Maximum Power Dissipation

Output Short Circuit

Shorting the output to ground or drawing excessive current from the AD8029/AD8030/AD8040 could cause catastrophic failure.

TYPICAL PERFORMANCE CHARACTERISTICS

Default Conditions: V_S = 5 V (T_A = 25°C, R_L = 1 kΩ tied to midsupply, unless otherwise noted.)

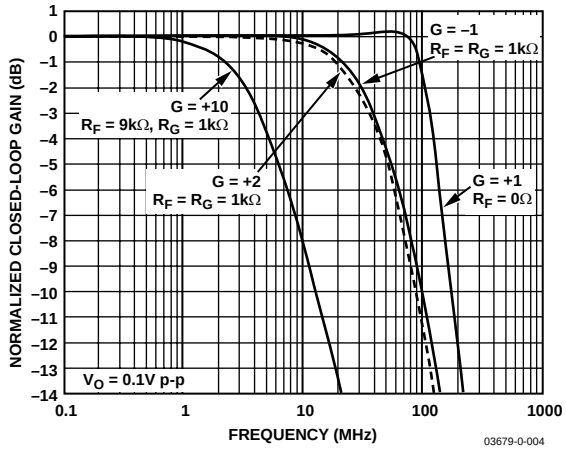


Figure 7. Small Signal Frequency Response for Various Gains

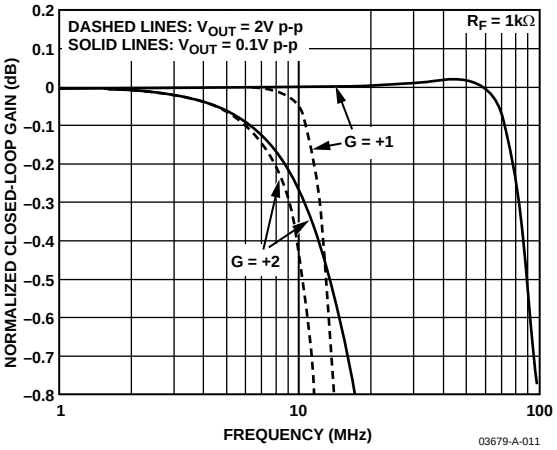


Figure 10. 0.1 dB Flatness Frequency Response

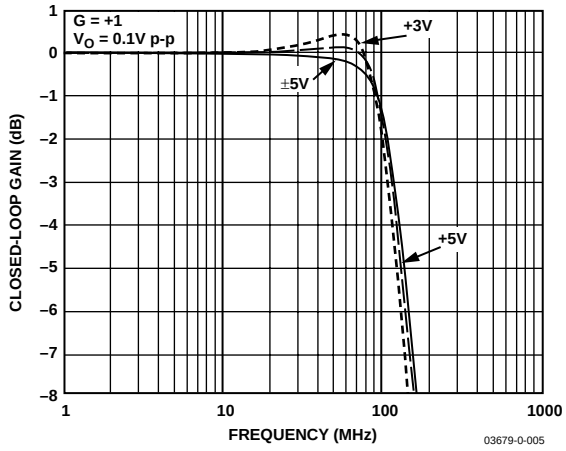


Figure 8. Small Signal Frequency Response for Various Supplies

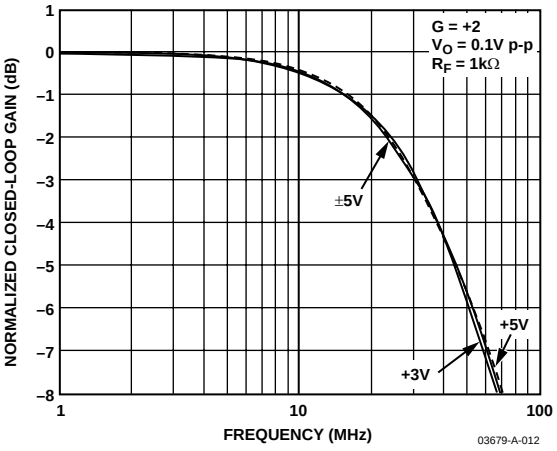


Figure 11. Small Signal Frequency Response for Various Supplies

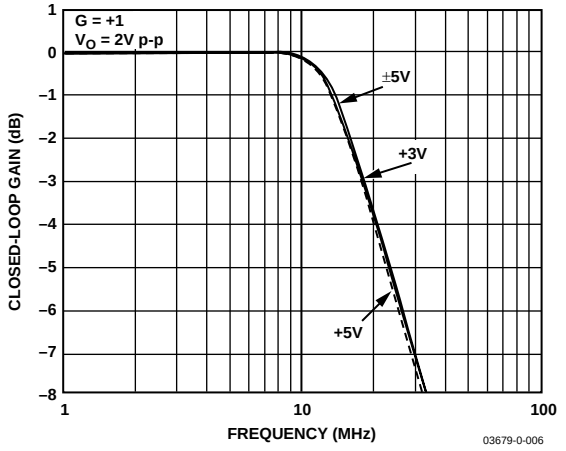


Figure 9. Large Signal Frequency Response for Various Supplies

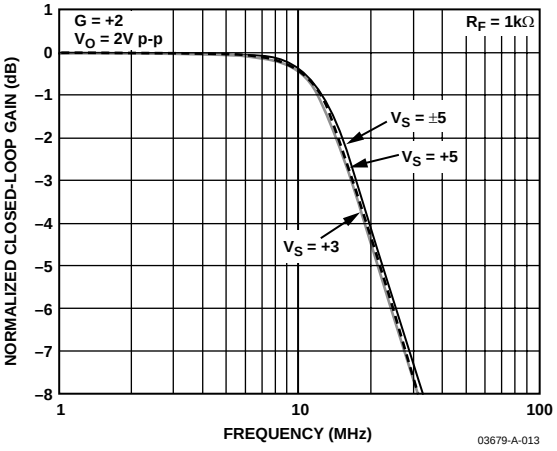


Figure 12. Large Signal Frequency Response for Various Supplies

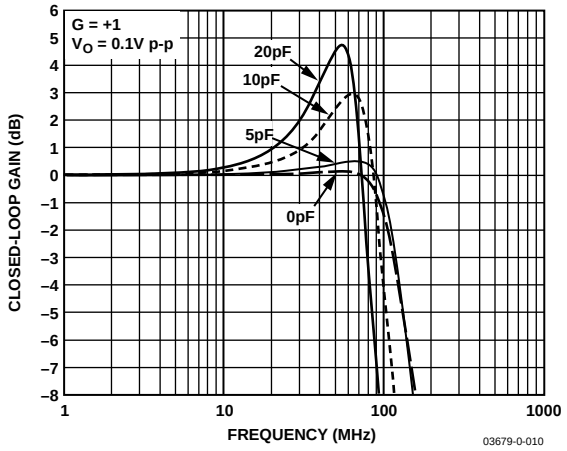


Figure 13. Small Signal Frequency Response for Various C_{LOAD}

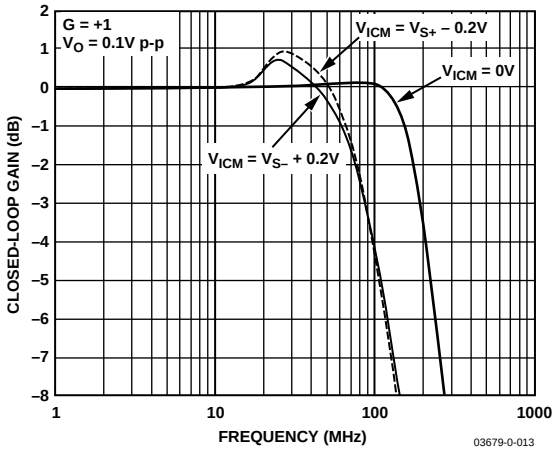


Figure 16. Small Signal Frequency Response for Various Input Common-Mode Voltages

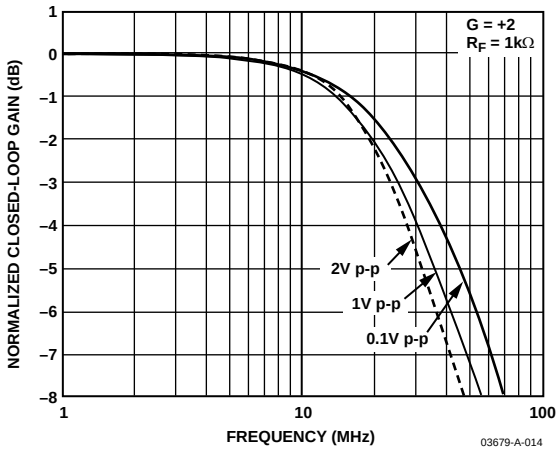


Figure 14. Frequency Response for Various Output Amplitudes

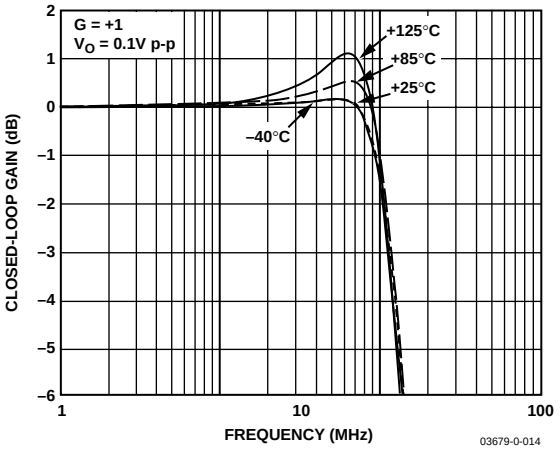


Figure 17. Small Signal Frequency Response vs. Temperature

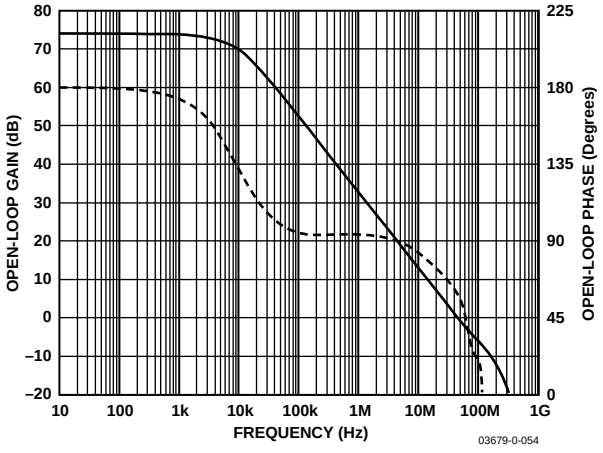


Figure 15. Open-Loop Gain and Phase vs. Frequency

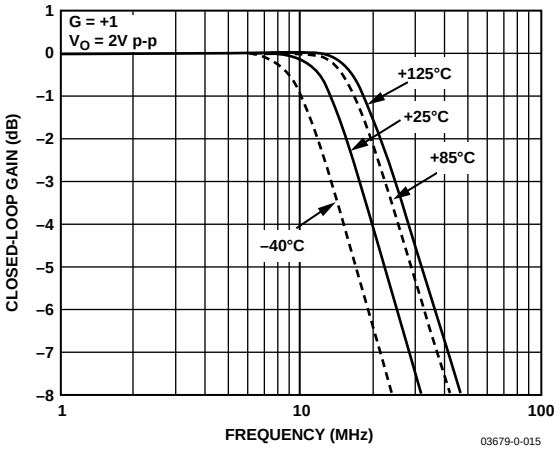


Figure 18. Large Signal Frequency Response vs. Temperature

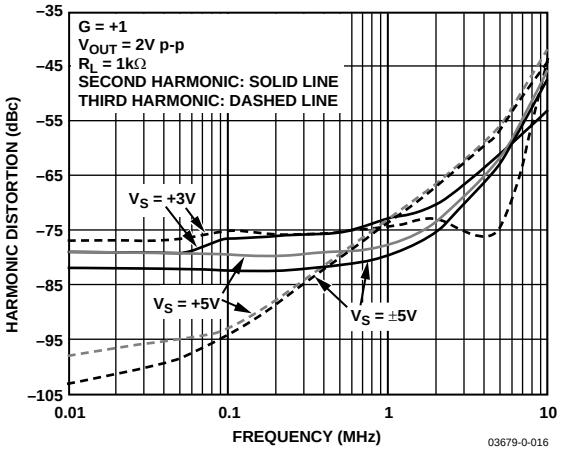


Figure 19. Harmonic Distortion vs. Frequency and Supply Voltage

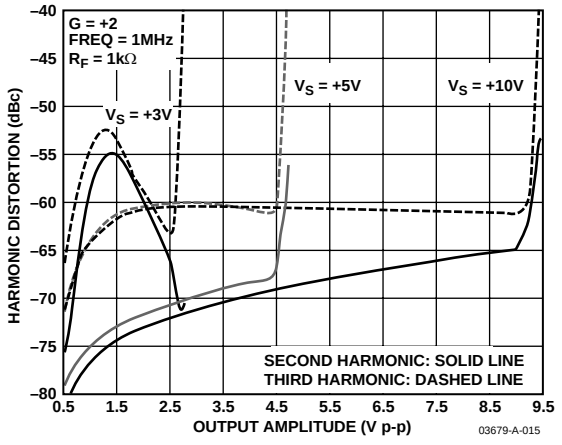


Figure 20. Harmonic Distortion vs. Output Amplitude

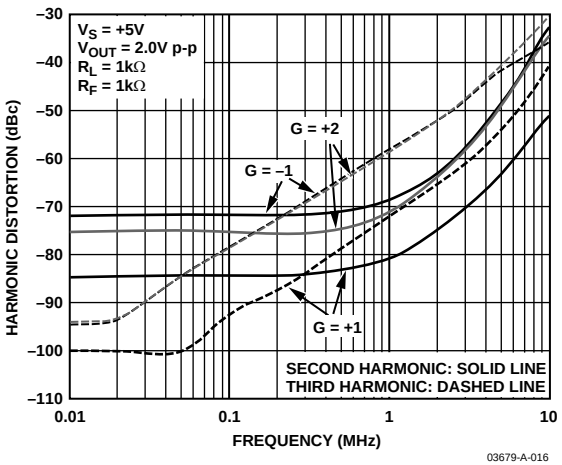


Figure 21. Harmonic Distortion vs. Frequency and Gain

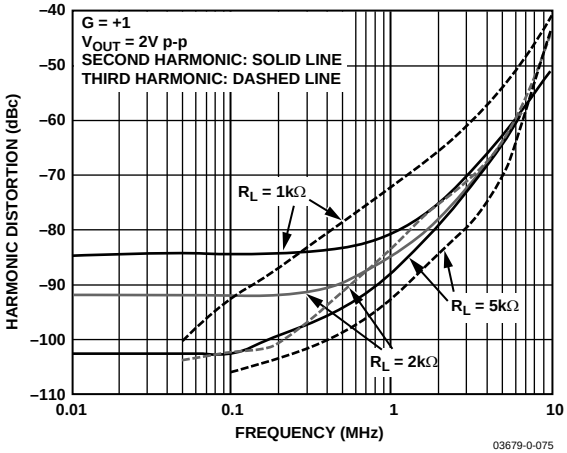


Figure 22. Harmonic Distortion vs. Frequency and Load

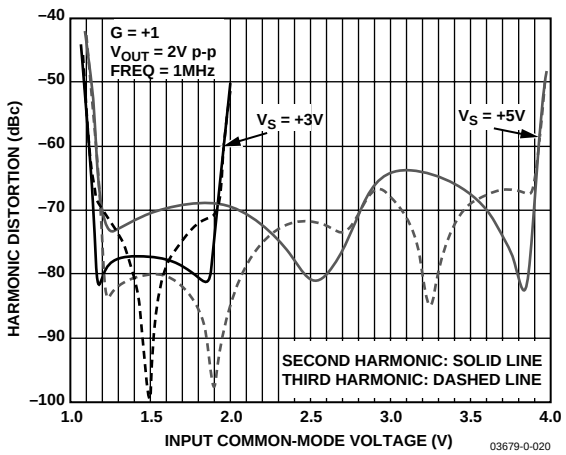


Figure 23. Harmonic Distortion vs. Input Common Mode Voltage

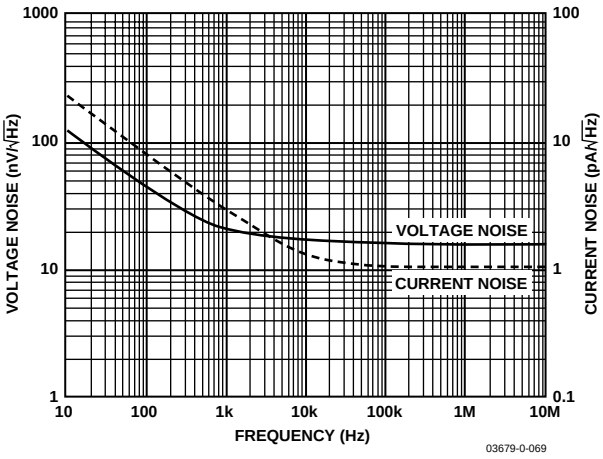


Figure 24. Voltage and Current Noise vs. Frequency

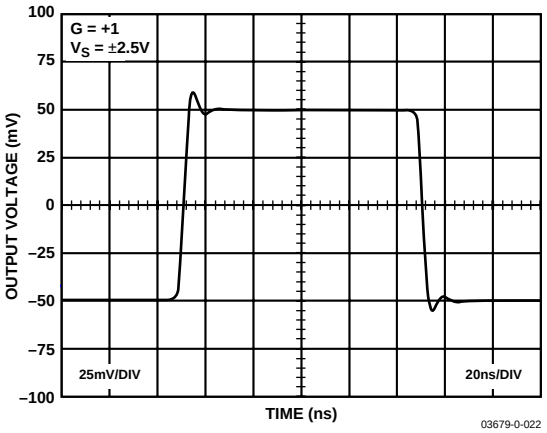


Figure 25. Small Signal Transient Response

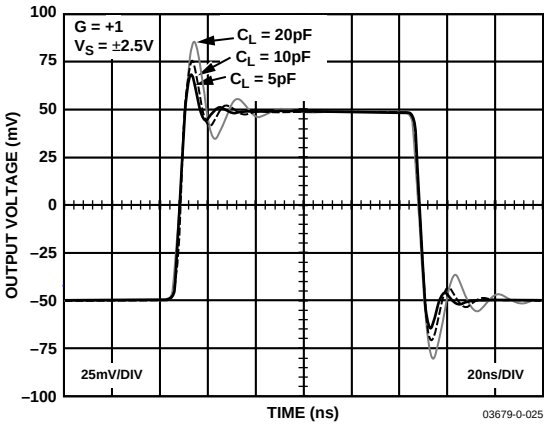


Figure 28. Small Signal Transient Response with Capacitive Load

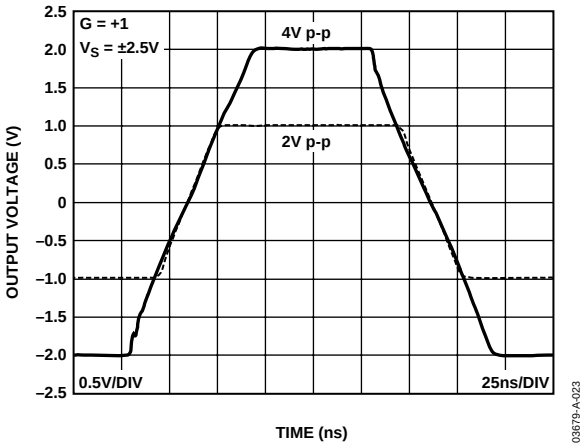


Figure 26. Large Signal Transient Response

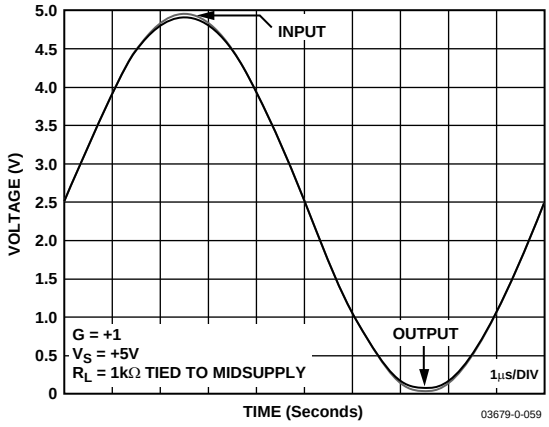


Figure 29. Rail-to-Rail Response, G = +1

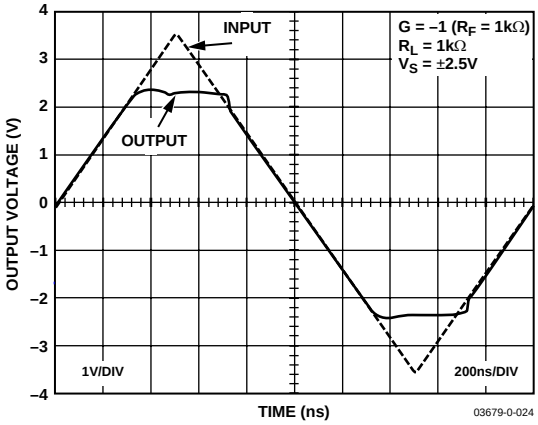


Figure 27. Output Overdrive Recovery

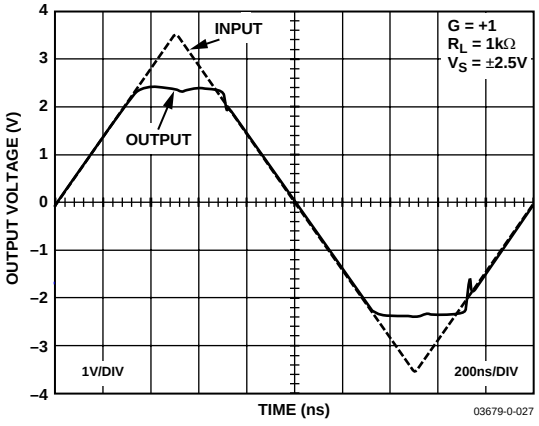


Figure 30. Input Overdrive Recovery

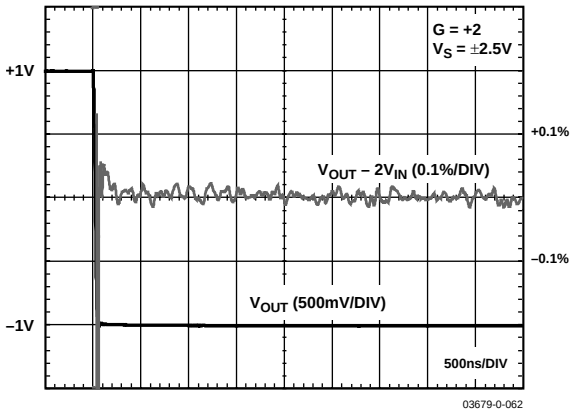


Figure 31. Long-Term Settling Time

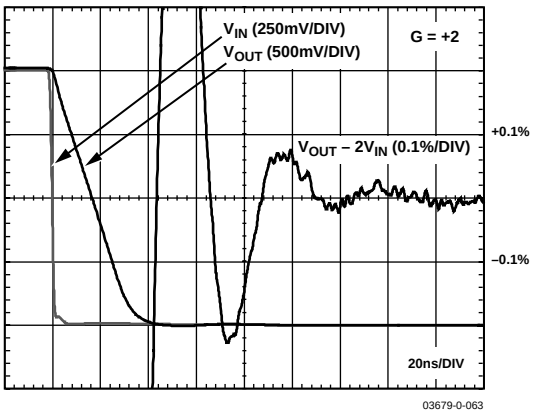


Figure 34.0.1% Short-Term Settling Time

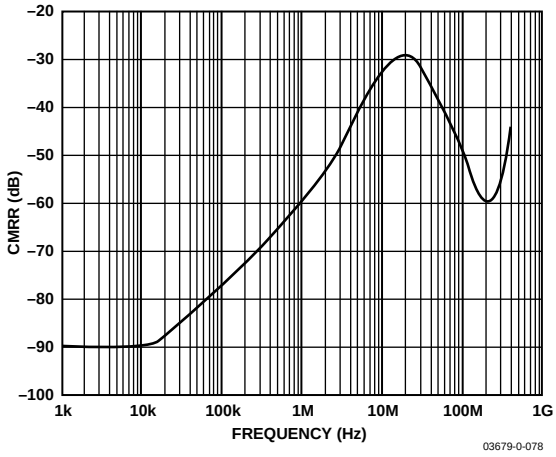


Figure 32. Common-Mode Rejection Ratio vs. Frequency

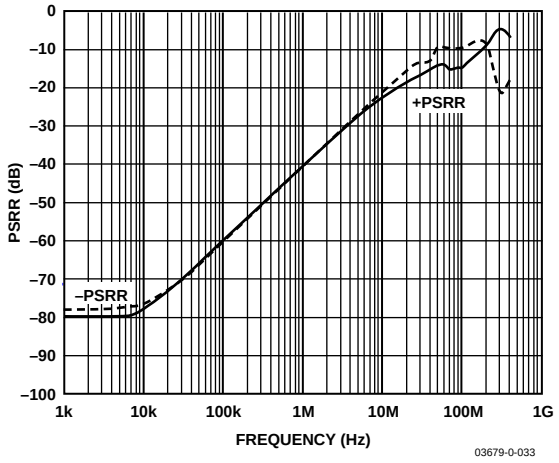


Figure 35. PSRR vs. Frequency

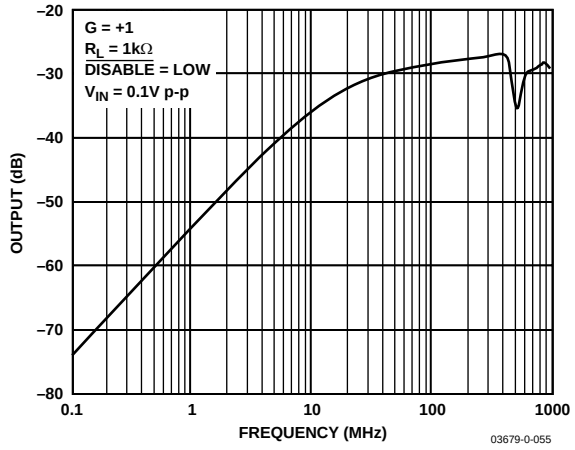


Figure 33. AD8029 Off-Isolation vs. Frequency

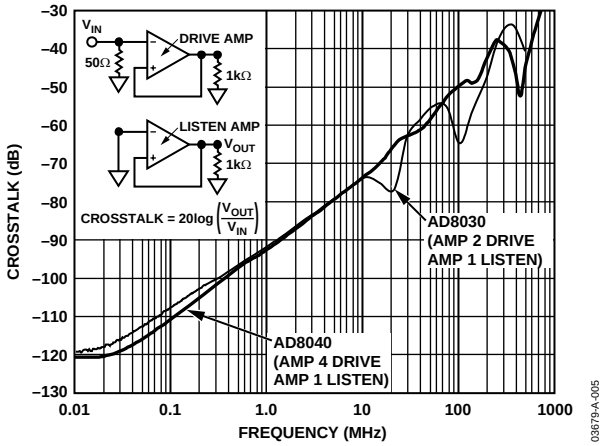


Figure 36. AD8030/AD8040 Crosstalk vs. Frequency

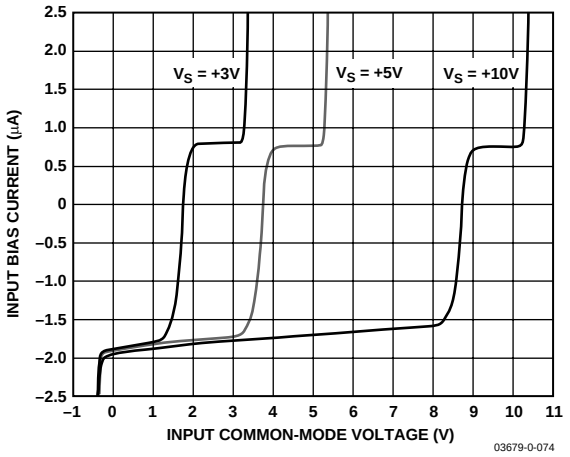


Figure 37. Input Bias Current vs. Input Common-Mode Voltage

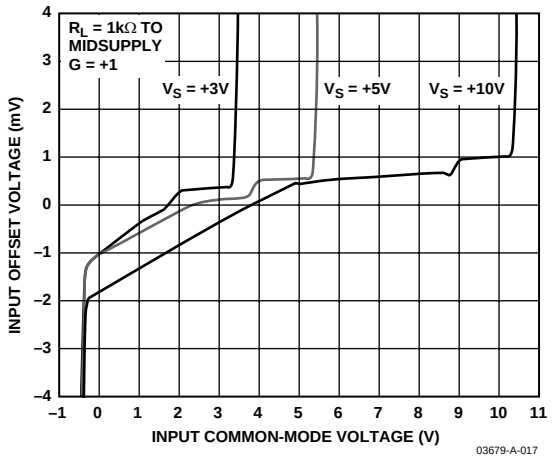


Figure 40. Input Offset Voltage vs. Input Common-Mode Voltage

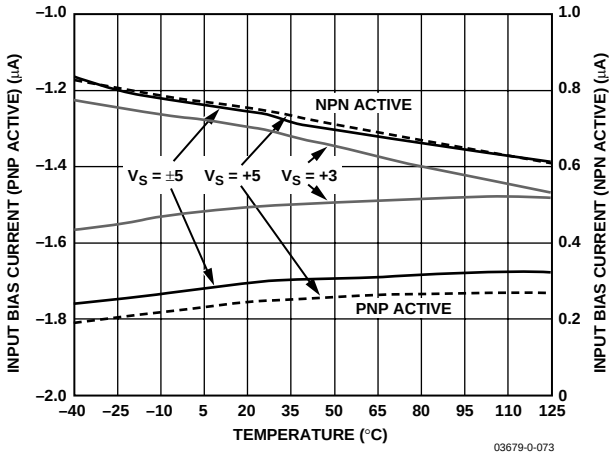


Figure 38. Input Bias Current vs. Temperature

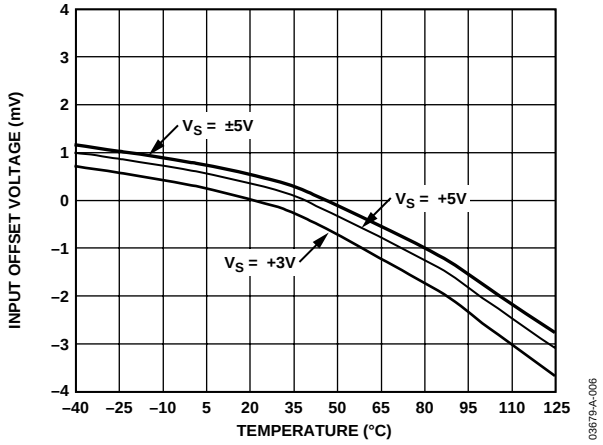


Figure 41. Input Offset Voltage vs. Temperature

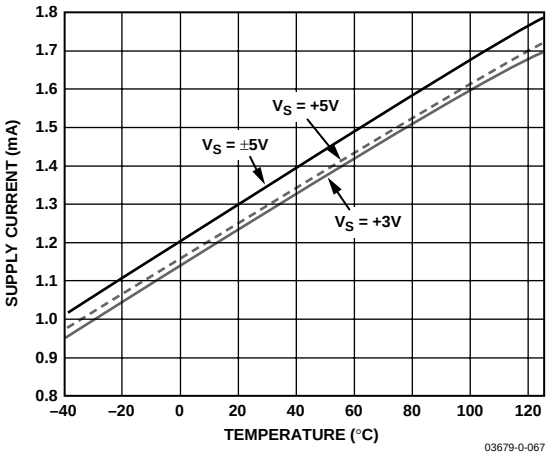


Figure 39 Quiescent Supply Current vs. Temperature

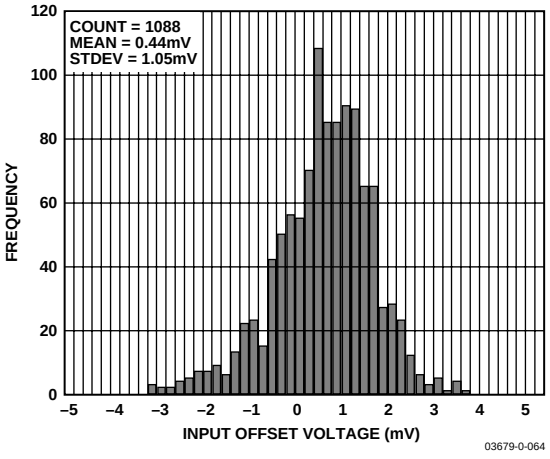


Figure 42. Input Offset Voltage Distribution

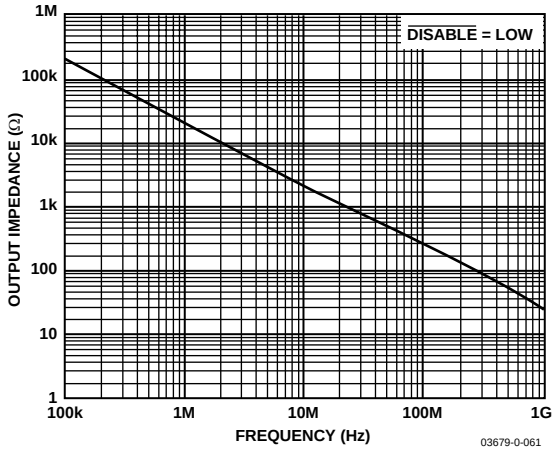


Figure 43. AD8029 Output Impedance vs. Frequency, Disabled

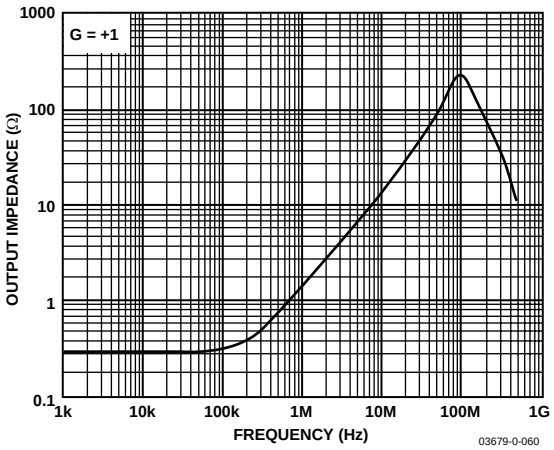


Figure 45. Output Impedance vs. Frequency, Enabled

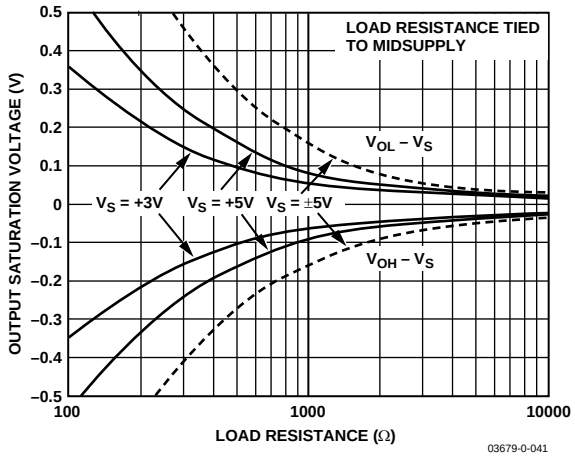


Figure 44. Output Saturation Voltage vs. Load Resistance

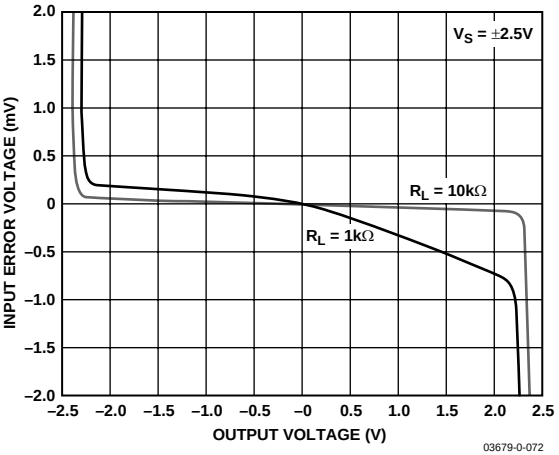


Figure 46. Input Error Voltage vs. Output Voltage

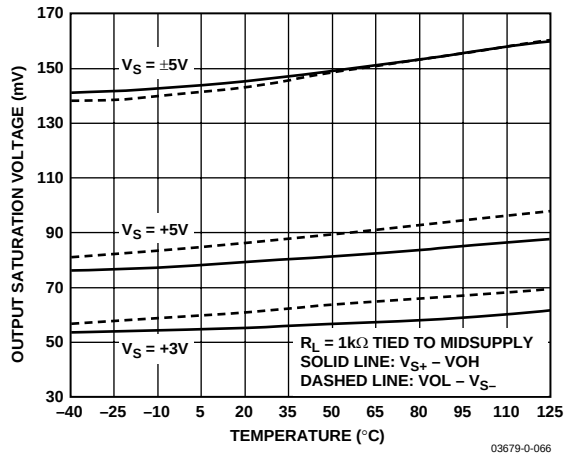


Figure 42. Output Saturation Voltage vs. Temperature

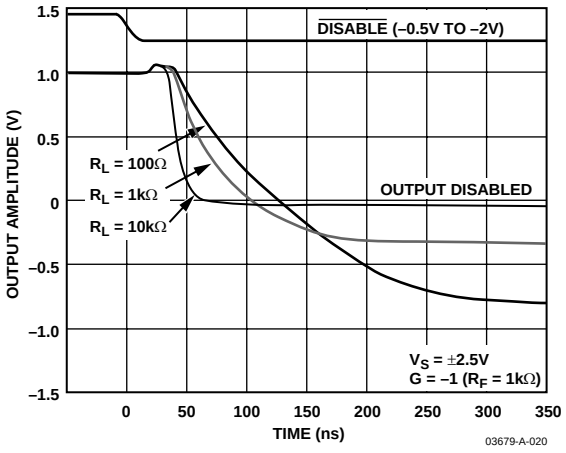


Figure 47. AD8029 $\overline{DISABLE}$ Turn-Off Timing

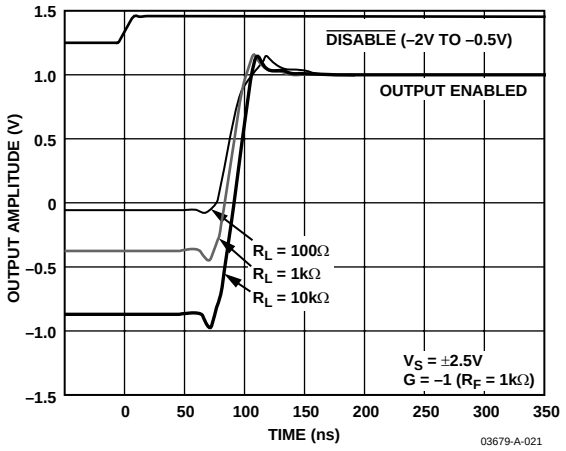


Figure 48. AD8029 $\overline{DISABLE}$ Turn-On Timing

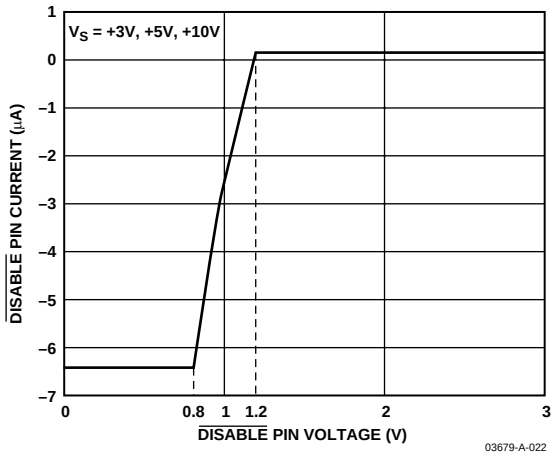


Figure 49. AD8029 $\overline{DISABLE}$ Pin Current vs. $\overline{DISABLE}$ Pin Voltage

THEORY OF OPERATION

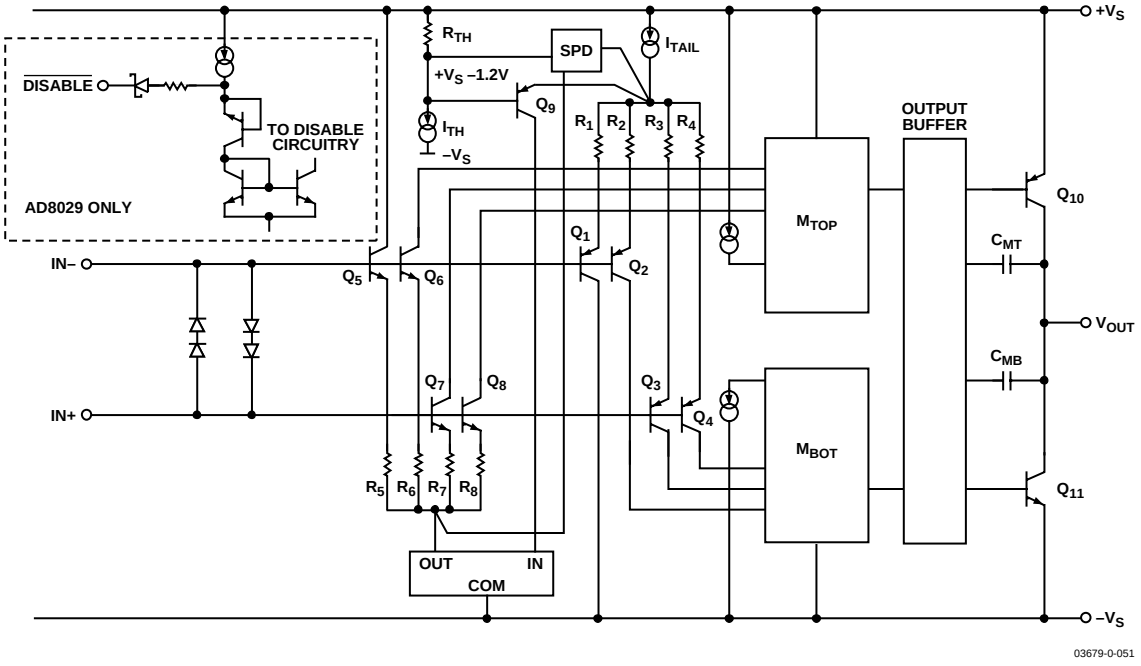


Figure 50. Simplified Schematic

The AD8029 (single), AD8030 (dual), and AD8040 (quad) are rail-to-rail input and output amplifiers fabricated using Analog Devices' XFCB process. The XFCB process enables the AD8029/AD8030/AD8040 to operate on 2.7 V to 12 V supplies with a 120 MHz bandwidth and a 60 V/µs slew rate. A simplified schematic of the AD8029/AD8030/AD8040 is shown in Figure 50.

INPUT STAGE

For input common-mode voltages less than a set threshold (1.2 V below V_{CC}), the resistor degenerated PNP differential pair (comprising Q_1 toQ_4) carries the entire I_{TAIL} current, allowing the input voltage to go 200 mV below $-V_S$. Conversely, input common-mode voltages exceeding the same threshold cause I_{TAIL} to be routed away from the PNP differential pair and into the NPN differential pair through transistor Q_9. Under this condition, the input common-mode voltage is allowed to rise 200 mV above $+V_S$ while still maintaining linear amplifier behavior. The transition between these two modes of operation leads to a sudden, temporary shift in input stage transconductance, g_m, and dc parameters (such as the input offset voltage V_{OS}), which in turn adversely affect the distortion performance. The SPD block shortens the duration of this transition, thus improving the distortion performance. As shown in Figure 50, the input differential pair is protected by a pair of two series diodes, connected in anti-parallel, which clamp the differential input voltage to approximately ±1.5 V.

OUTPUT STAGE

The currents derived from the PNP and NPN input differential pairs are injected into the current mirrors M_{BOT} and M_{TOP}, thus establishing a common-mode signal voltage at the input of the output buffer.

The output buffer performs three functions:

1. It buffers and applies the desired signal voltage to the output devices, Q_{10} and Q_{11}.
2. It senses the common-mode current level in the output devices.
3. It regulates the output common-mode current by establishing a common-mode feedback loop.

The output devices Q_{10} and Q_{11} work in a common-emitter configuration, and are Miller-compensated by internal capacitors, C_{MT} and C_{MB}.

The output voltage compliance is set by the output devices' collector resistance R_C (about 25 Ω), and by the required load current I_L. For instance, a light equivalent load (5 kΩ) allows the output voltage to swing to within 40 mV of either rail, while heavier loads cause this figure to deteriorate as $R_C \times I_L$.

APPLICATIONS

WIDEBAND OPERATION

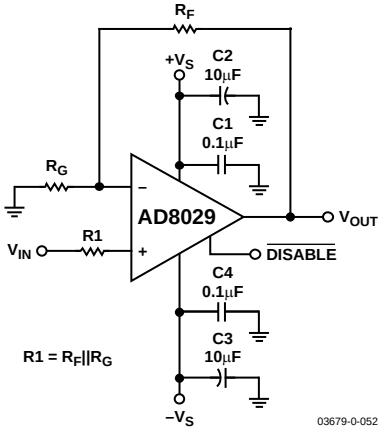


Figure 51. Wideband Non-inverting Gain Configuration

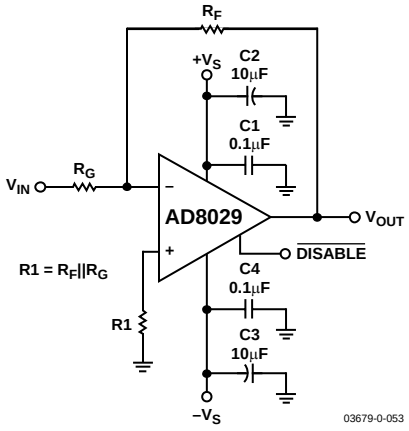


Figure 52. Wideband Inverting Gain Configuration

OUTPUT LOADING SENSITIVITY

To achieve maximum performance and low power dissipation, the designer needs to consider the loading at the output of AD8029/AD8030/AD8040. Table 5 shows the effects of output loading and performance.

When operating at unity gain, the effective load at the amplifier output is the resistance (R_L) being driven by the amplifier. For gains other than 1, in noninverting configurations, the feedback network represents an additional current load at the amplifier output. The feedback network ($R_F + R_G$) is in parallel with R_L, which lowers the effective resistance at the output of the amplifier. The lower effective resistance causes the amplifier to supply more current at the output. Lower values of feedback resistance increase the current draw, thus increasing the amplifier's power dissipation.

For example, if using the values shown in Table 5 for a gain of 2, with resistor values of 2.5 kΩ, the effective load at the output is 1.67 kΩ. For inverting configurations, only the feedback resistor R_F is in parallel with the output load. If the load is greater than that specified in the data sheet, the amplifier can introduce nonlinearities in its open-loop response, which increases distortion. Figure 53 and Figure 54 illustrate effective output loading and distortion performance. Increasing the resistance of the feedback network can reduce the current consumption, but has other implications.

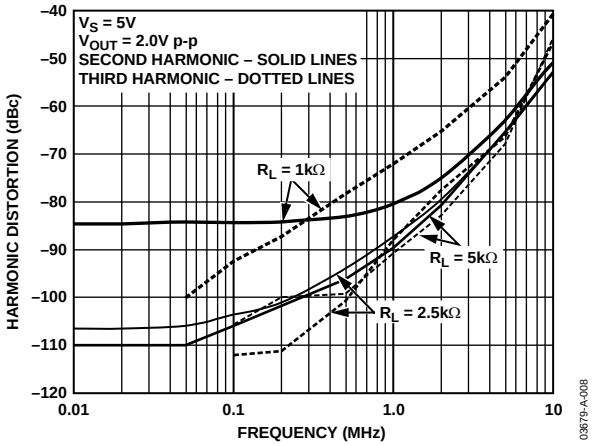


Figure 53. Gain of 1 Distortion

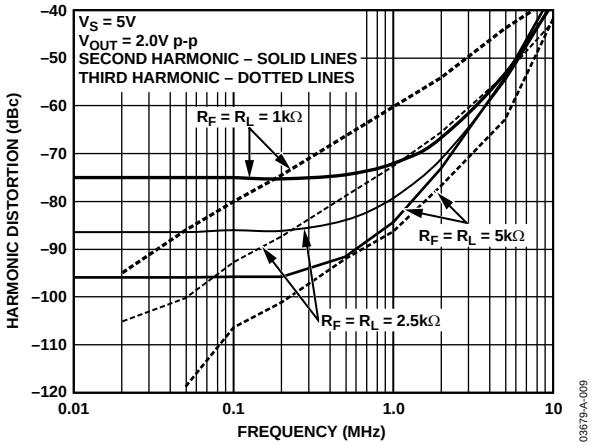


Figure 54. Gain of 2 Distortion

Table 5. Effect of Load on Performance

Noninverting Gain	R_F (kΩ)	R_G (kΩ)	R_{LOAD} (kΩ)	−3 dB SS BW (MHz)	Peaking (dB)	HD2 at 1 MHz, 2 V p-p (dB)	HD3 at 1 MHz, 2 V p-p (dB)	Output Noise (nV/√Hz)
1	0	N/A	1	120	0.02	−80	−72	16.5
1	0	N/A	2	130	0.6	−84	−83	16.5
1	0	N/A	5	139	1	−87.5	−92.5	16.5
2	1	1	1	36	0	−72	−60	33.5
2	2.5	2.5	2.5	44.5	0.2	−79	−72.5	34.4
2	5	5	5	43	2	−84	−86	36
−1	1	1	1	40	0.01	−68	−57	33.6
−1	2.5	2.5	2.5	40	0.05	−74	−68	34
−1	5	5	5	34	1	−78	−80	36

The feedback resistance (R_F || R_G) combines with the input capacitance to form a pole in the amplifier's loop response. This can cause peaking and ringing in the amplifier's response if the RC time constant is too low. Figure 55 illustrates this effect. Peaking can be reduced by adding a small capacitor (1 pF–4 pF) across the feedback resistor. The best way to find the optimal value of capacitor is to empirically try it in your circuit. Another factor of higher resistance values is the impact it has on noise performance. Higher resistor values generate more noise. Each application is unique and therefore a balance must be reached between distortion, peaking, and noise performance. Table 5 outlines the trade-offs that different loads have on distortion, peaking, and noise performance. In gains of 1, 2, and 10, equivalent loads of 1 kΩ, 2 kΩ, and 5 kΩ are shown.

With increasing load resistance, the distortion and –3 dB bandwidth improve, while the noise and peaking degrade slightly.

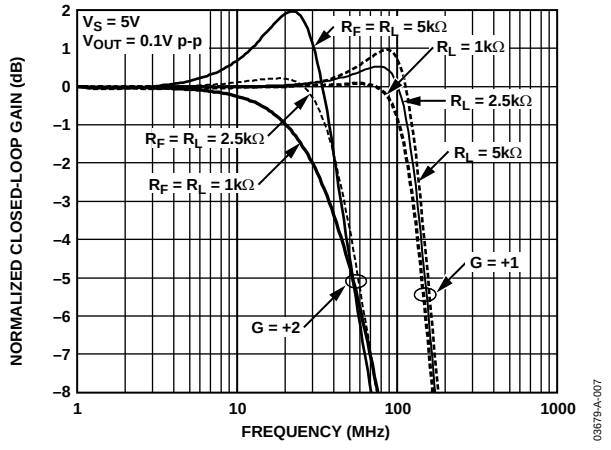


Figure 55. Frequency Response for Various Feedback/Load Resistances

DISABLE PIN

The AD8029 disable pin allows the amplifier to be shut down for power conservation or multiplexing applications. When in the disable mode, the amplifier draws only 150 μA of quiescent current. The disable pin control voltage is referenced to the negative supply. The amplifier enters power-down mode any time the disable pin is tied to the most negative supply or within 0.8 V of the negative supply. If left open, the amplifier will operate normally. For switching levels, refer to Table 6.

Table 6. Disable Pin Control Voltage

Disable Pin Voltage	Supply Voltage		
	+3 V	+5 V	±5 V
Low (Disabled)	0 V to <0.8 V	0 V to <0.8 V	−5 V to <−4 .2 V
High (Enabled)	1.2 V to 3 V	1.2 V to 5 V	−3.8 V to +5 V

CIRCUIT CONSIDERATIONS

PCB Layout

High speed op amps require careful attention to PCB layout to achieve optimum performance. Particular care must be exercised to minimize lead lengths of the bypass capacitors. Excess lead inductance can influence the frequency response and even cause high frequency oscillations. Using a multilayer board with an internal ground plane can help reduce ground noise and enable a more compact layout.

To achieve the shortest possible trace length at the inverting input, the feedback resistor, R_F, should be located the shortest distance from the output pin to the input pin. The return node of the resistor R_G should be situated as close as possible to the return node of the negative supply bypass capacitor.

On multilayer boards, all layers beneath the op amp should be cleared of metal to avoid creating parasitic capacitive elements. This is especially true at the summing junction, i.e., the inverting input, –IN. Extra capacitance at the summing junction can cause increased peaking in the frequency response and lower phase margin.

Grounding

To minimize parasitic inductances and ground loops in high speed, densely populated boards, a ground plane layer is critical. Understanding where the current flows in a circuit is critical in the implementation of high speed circuit design. The length of the current path is directly proportional to the magnitude of the parasitic inductances and thus the high frequency impedance of the path. Fast current changes in an inductive ground return will create unwanted noise and ringing.

The length of the high frequency bypass capacitor pads and traces is critical. A parasitic inductance in the bypass grounding works against the low impedance created by the bypass capacitor. Because load currents flow from supplies as well as from ground, the load should be placed at the same physical location as the bypass capacitor ground. For large values of capacitors, which are intended to be effective at lower frequencies, the current return path length is less critical.

Power Supply Bypassing

Power supply pins are actually inputs to the op amp. Care must be taken to provide the op amp with a clean, low noise dc voltage source.

Power supply bypassing is employed to provide a low impedance path to ground for noise and undesired signals at all frequencies. This cannot be achieved with a single capacitor type; but with a variety of capacitors in parallel the bandwidth of power supply bypassing can be greatly extended. The bypass capacitors have two functions:

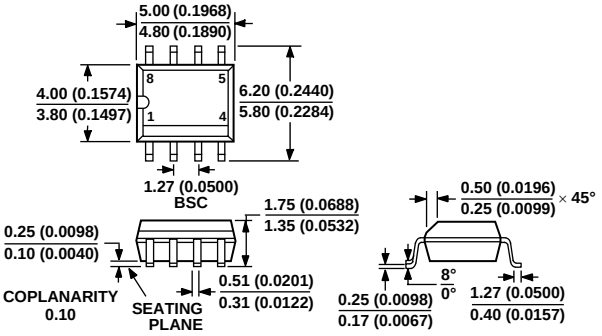
1. Provide a low impedance path for noise and undesired signals from the supply pins to ground.
2. Provide local stored charge for fast switching conditions and minimize the voltage drop at the supply pins during transients. This is typically achieved with large electrolytic capacitors.

Good quality ceramic chip capacitors should be used and always kept as close as possible to the amplifier package. A parallel combination of a 0.1 µF ceramic and a 10 µF electrolytic covers a wide range of rejection for unwanted noise. The 10 µF capacitor is less critical for high frequency bypassing and, in most cases, one per supply line is sufficient. The values of capacitors are circuit-dependant and should be determined by the system's requirements.

DESIGN TOOLS AND TECHNICAL SUPPORT

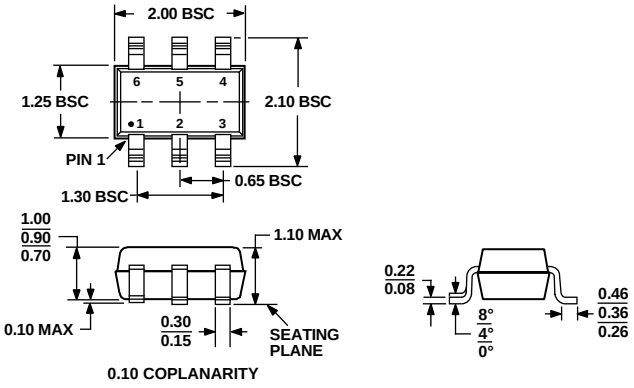
Analog Devices is committed to the design process by providing technical support and online design tools. ADI offers technical support via free evaluation boards, sample ICs, Spice models, interactive evaluation tools, application notes, phone and email support—all available at www.analog.com.

OUTLINE DIMENSIONS



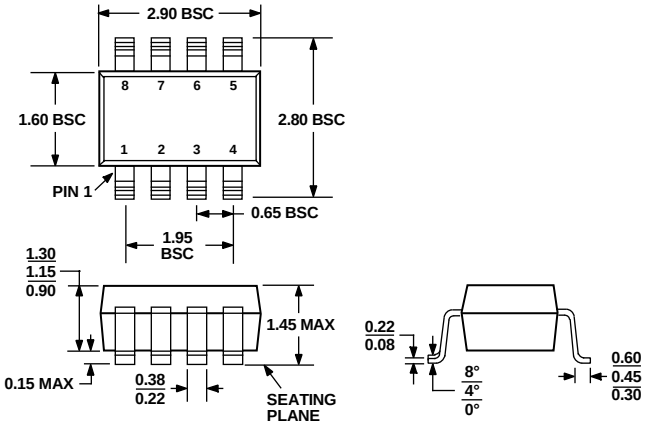
COMPLIANT TO JEDEC STANDARDS MS-012AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 56. 8-Lead Standard Small Outline Package, Narrow Body [SOIC] (R-8)
Dimensions shown in millimeters and (inches)



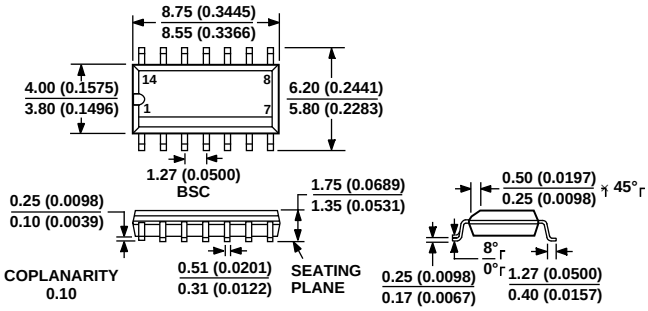
COMPLIANT TO JEDEC STANDARDS MO-203AB

Figure 57. 6-Lead Plastic Surface-Mount Package [SC70] (KS-6)
Dimensions shown in millimeters



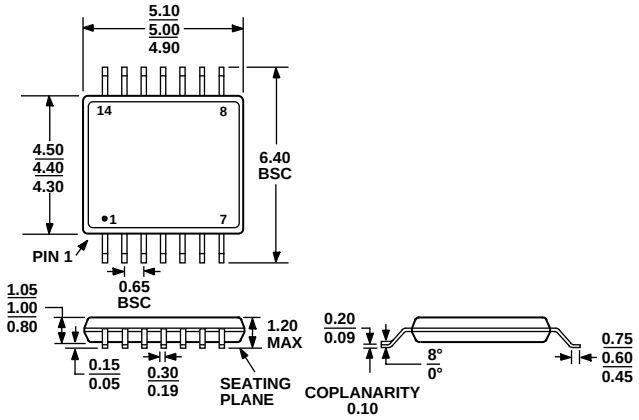
COMPLIANT TO JEDEC STANDARDS MO-178BA

Figure 58. 8-Lead Small Outline Transistor Package [SOT23] (RJ-8)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012AB
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Figure 59. 14-Lead Standard Small Outline Package [SOIC] (R-14)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-153AB-1

Figure 60. 14-Lead Thin Shrink Small Outline Package [TSSOP] (RU-14)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Minimum Ordering Quantity	Temperature Range	Package Description	Package Option	Branding
AD8029AR	1	–40°C to +125°C	8-Lead SOIC	R-8	
AD8029AR-REEL	2,500	–40°C to +125°C	8-Lead SOIC	R-8	
AD8029AR-REEL7	1,000	–40°C to +125°C	8-Lead SOIC	R-8	
AD8029AKS-R2	250	–40°C to +125°C	6-Lead SC70	KS-6	H6B
AD8029AKS-REEL	10,000	–40°C to +125°C	6-Lead SC70	KS-6	H6B
AD8029AKS-REEL7	3,000	–40°C to +125°C	6-Lead SC70	KS-6	H6B
AD8030AR	1	–40°C to +125°C	8-Lead SOIC	R-8	
AD8030AR-REEL	2,500	–40°C to +125°C	8-Lead SOIC	R-8	
AD8030AR-REEL7	1,000	–40°C to +125°C	8-Lead SOIC	R-8	
AD8030ARJ-R2	250	–40°C to +125°C	8-Lead SOT23-8	RJ-8	H7B
AD8030ARJ-REEL	10,000	–40°C to +125°C	8-Lead SOT23-8	RJ-8	H7B
AD8030ARJ-REEL7	3,000	–40°C to +125°C	8-Lead SOT23-8	RJ-8	H7B
AD8040AR	1	–40°C to +125°C	14-Lead SOIC	R-14	
AD8040AR-REEL	2500	–40°C to +125°C	14-Lead SOIC	R-14	
AD8040AR-REEL7	1000	–40°C to +125°C	14-Lead SOIC	R-14	
AD8040ARU	1	–40°C to +125°C	14-Lead TSSOP	RU-14	
AD8040ARU-REEL	2500	–40°C to +125°C	14-Lead TSSOP	RU-14	
AD8040ARU-REEL7	1000	–40°C to +125°C	14-Lead TSSOP	RU-14	

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

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