

FEATURES

- Programmable 12-Channel Gamma Reference Generator
- Mask Programmable Adjustable V_{COM} Buffer
- Upper/Lower Outputs Swing to V_{DD}/GND
- Continuous Output Current: 10 mA
- V_{COM} Peak Output Current: 250 mA
- Outputs with Fast Settling Time for Load Change
- Output Pins Are Compatible with ADD8701
- Single-Supply Operation: 7 V to 16 V
- Supply Current: 15 mA Max

APPLICATIONS

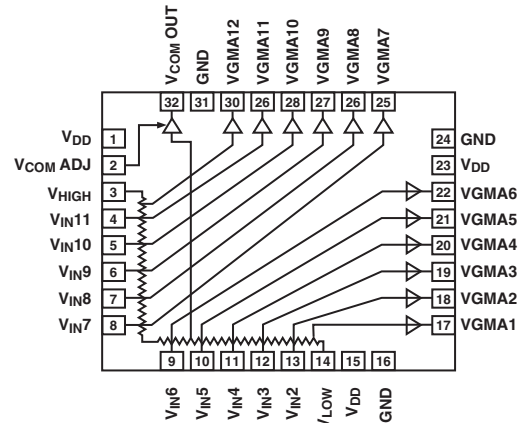
TFT LCD Panels

GENERAL DESCRIPTION

The ADD8702 is a low cost, mask programmable, 12-channel gamma reference generator, plus an adjustable V_{COM} driver. This part is designed to provide gamma correction for high resolution TFT LCD panels. The 12 gamma reference levels and V_{COM} are mask programmable to 0.3% resolution using the on-chip 500 chain resistor string. This reduces component and board costs.

The ADD8702 provides a complete programmed set of gamma voltage references for the LCD source drivers. These references settle quickly to load change. The V_{COM} output is stable with high capacitive loads and can source or sink 250 mA peak current. The V_{COM} output level can be adjusted using an external trim-potentiometer or discrete resistors.

FUNCTIONAL BLOCK DIAGRAM



The output pins are compatible with the ADD8701. This allows for single board design and fast turns for prototyping using the initial ADD8701 board design.

The ADD8702 is specified over the temperature range of -40°C to $+85^{\circ}\text{C}$ and comes in the 32-lead lead frame chip scale package (LFCSP) for compact board space.

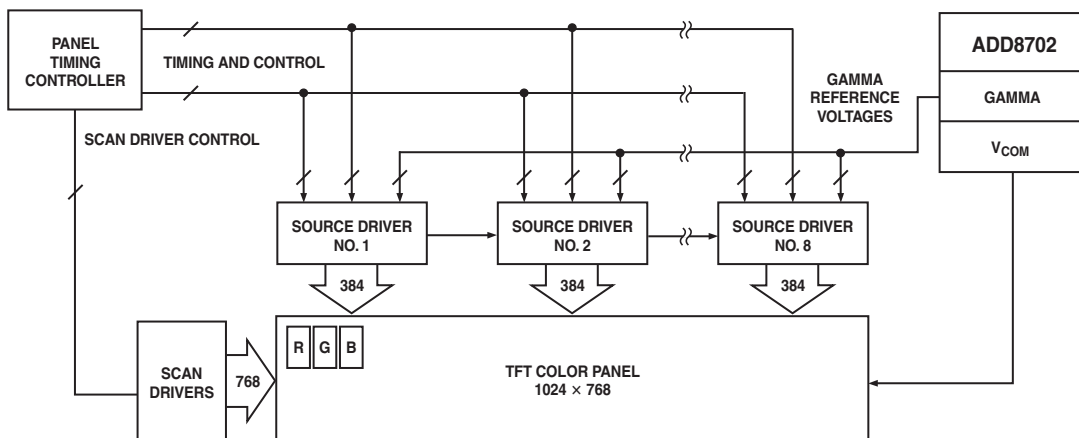


Figure 1. Typical SVGA TFT LCD Application

REV. 0

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ADD8702—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (V_{DD} = 16 V, T_A = 25°C, unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OUTPUT ACCURACY V _{SYSTEM ERROR}	V _{SY ERROR}			10	50	mV
MASK PROGRAMMABLE RESISTOR STRING						
Total Resistor String	R _{TOTAL}	500 Elements V _{LOW} to V _{HIGH}		22.5		kΩ
Resistor Matching	R _{MATCH}	Any Two Segments		1		%
OUTPUT CHARACTERISTICS						
Output Voltage High (VGMA11, VGMA12)	V _{OUT}	I _L = 100 μA I _L = 5 mA -40°C ≤ T _A ≤ +85°C	15.85 15.75	15.995 15.95		V V V
Output Voltage Mid (VGMA3 to VGMA10)	V _{OUT}	I _L = 5 mA		14.6		V
Output Voltage Low (VGMA1, VGMA2)	V _{OUT}	I _L = 100 μA I _L = 5 mA -40°C ≤ T _A ≤ +85°C		5 50	150	mV mV
Continuous Output Current	I _{OUT}			10		mA
Peak Output Current	I _{PK}			150		mA
Settling Time—Voltage	t _S	1 V Step 0.1%, R _L = 10 kΩ, C _L = 200 pF		1		μs
V _{COM} CHARACTERISTICS						
Continuous Output Current	I _{OUT}			35		mA
Peak Output Current	I _{PK}			250		mA
Settling Time—Voltage	t _S	1 V Step 0.1%, R _L = 10 kΩ, C _L = 200 pF		0.8		μs
SUPPLY CHARACTERISTICS						
Supply Voltage	V _{DD}		7		16	V
Power Supply Rejection Ratio	PSRR	V _S = 6 V to 17 V, -40°C ≤ T _A ≤ +85°C	68	75		dB
SUPPLY CURRENT	I _{SYS}	No Load -40°C ≤ T _A ≤ +85°C		11	15 16	mA mA

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (V_S)	18 V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-40°C to +85°C
Junction Temperature Range	-65°C to +150°C
Lead Temperature Range (Soldering, 60 sec.)	300°C
ESD Tolerance (HBM)	±1,000 V

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Type	θ_{JA}^1	Ψ_{JB}^2	Unit
32-Lead LFCSP (CP)	35	13	°C/W

NOTES

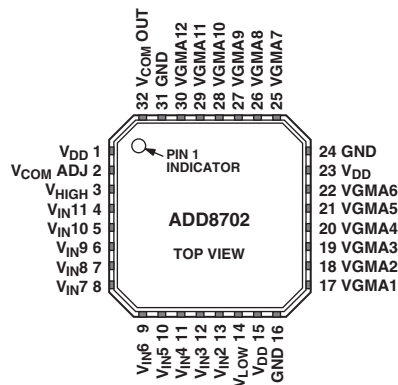
¹ θ_{JA} is specified for worst-case conditions, i.e., θ_{JA} is specified for device soldered in circuit board for surface-mount packages.

² Ψ_{JB} is applied for calculating the junction temperature by reference to the board temperature.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADD8702ACP-R2	-40°C to +85°C	32-Lead LFCSP	CP-32
ADD8702ACP-REEL	-40°C to +85°C	32-Lead LFCSP	CP-32
ADD8702ACP-REEL7	-40°C to +85°C	32-Lead LFCSP	CP-32

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

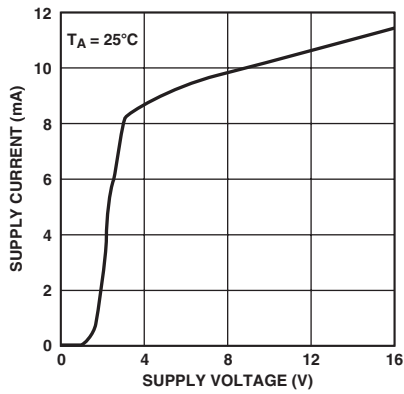
Pin No.	Mnemonic	Description
1, 15, 23	V_{DD}	Power (+)
2	$V_{COM} ADJ$	V_{COM} Adjust Input
3	V_{HIGH}	Highest Gamma Input Voltage
4-13	$V_{IN11}-V_{IN2}$	Gamma Buffer Inputs
14	V_{LOW}	Lowest Gamma Input Voltage
16, 24, 31	GND	Power (-)
17-22, 25-30	VGMA1-VGMA12	Gamma Buffer Outputs
32	$V_{COM} OUT$	V_{COM} Buffer Output

CAUTION

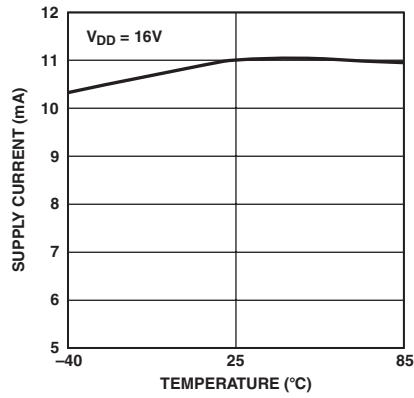
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADD8702 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



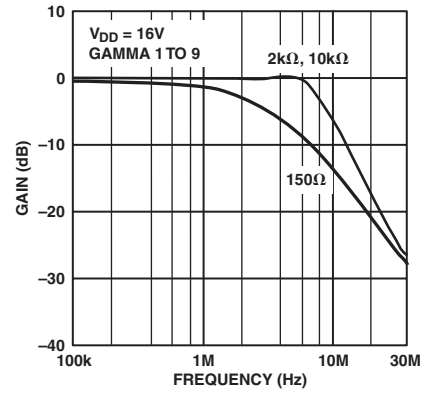
ADD8702—Typical Performance Characteristics



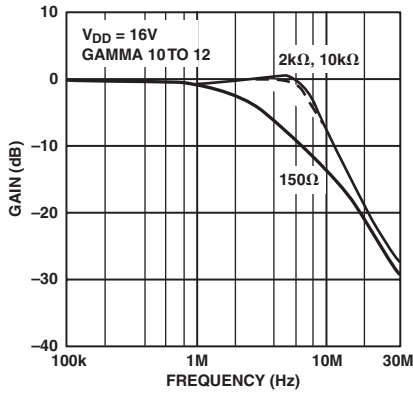
TPC 1. Supply Current vs. Supply Voltage



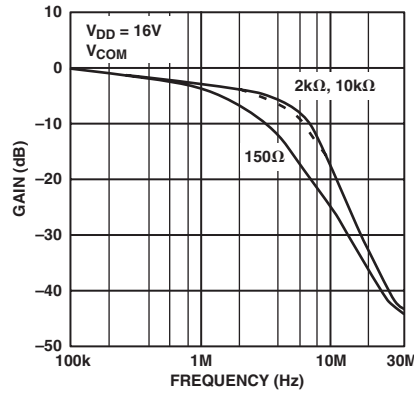
TPC 2. Supply Current vs. Temperature



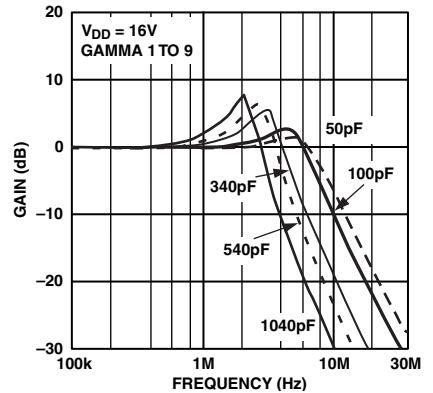
TPC 3. Frequency Response vs. Resistive Loading



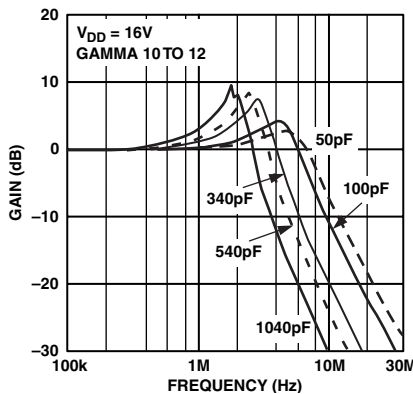
TPC 4. Frequency Response vs. Resistive Loading



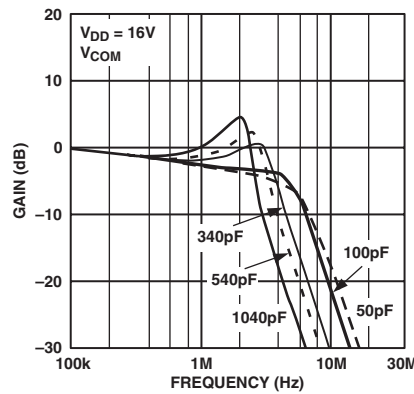
TPC 5. Frequency Response vs. Resistive Loading



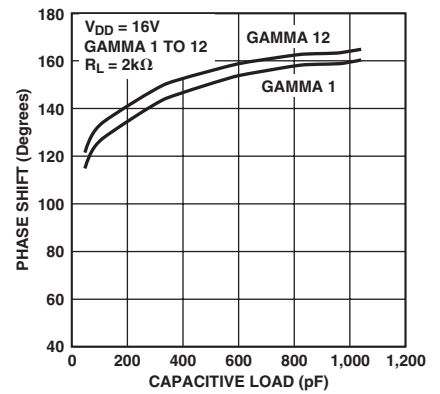
TPC 6. Frequency Response vs. Capacitive Loading



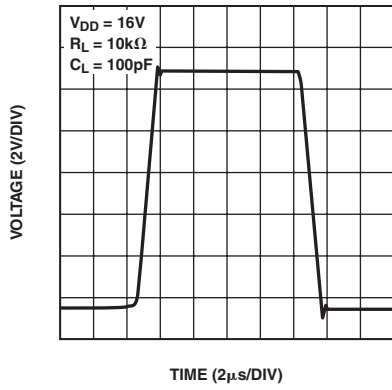
TPC 7. Frequency Response vs. Capacitive Loading



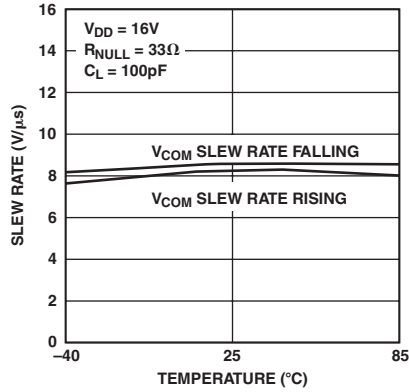
TPC 8. Frequency Response vs. Capacitive Loading



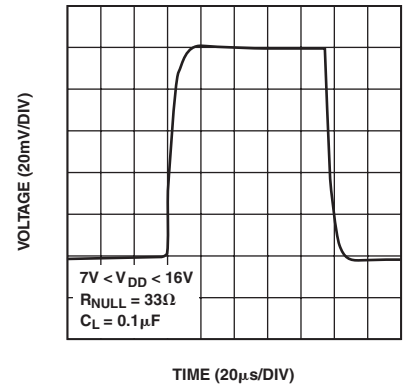
TPC 9. Input and Output Phase Shift vs. Capacitive Load



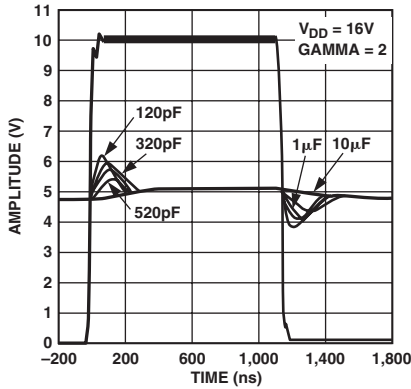
TPC 10. Large Signal Transient Response



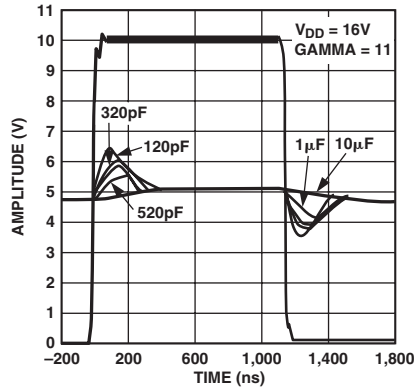
TPC 11. Slew Rate vs. Temperature



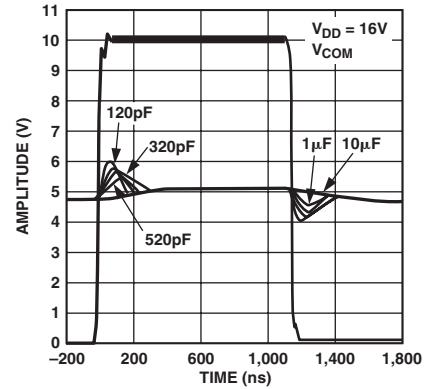
TPC 12. Small Signal Transient Response



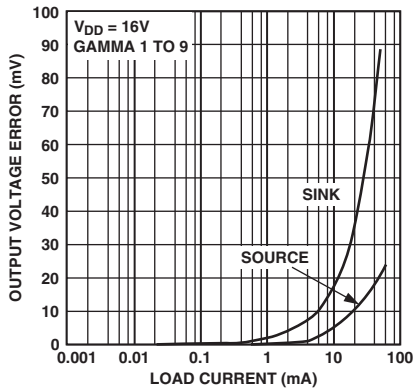
TPC 13. Transient Load Response vs. Capacitive Load



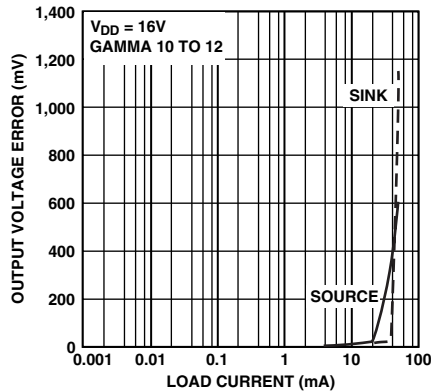
TPC 14. Transient Load Response vs. Capacitive Load



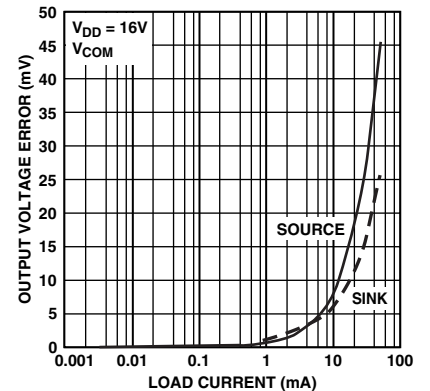
TPC 15. Transient Load Response vs. Capacitive Load



TPC 16. Output Voltage Error vs. Load Current

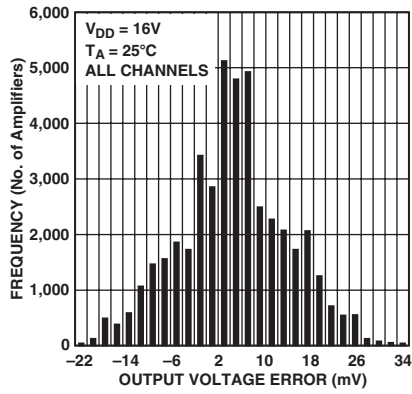


TPC 17. Output Voltage Error vs. Load Current

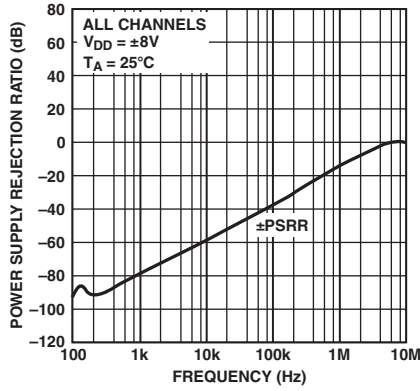


TPC 18. Output Voltage Error vs. Load Current

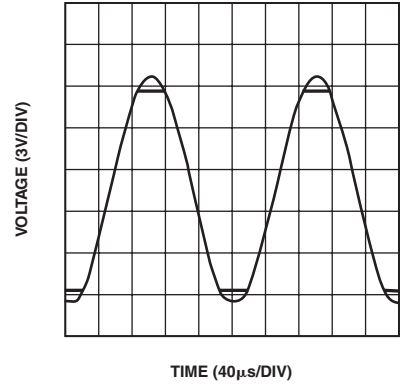
ADD8702



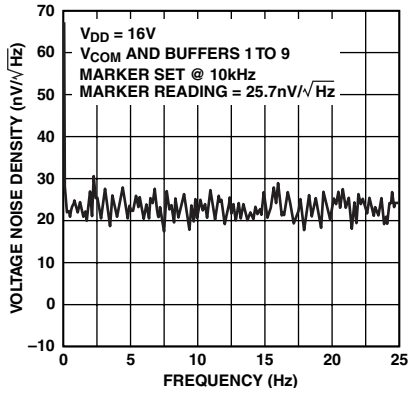
TPC 19. Output Voltage Error Distribution



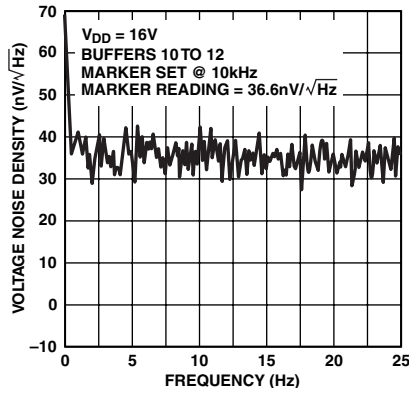
TPC 20. Power Supply Rejection Ratio vs. Frequency



TPC 21. No Phase Reversal



TPC 22. Voltage Noise Density vs. Frequency



TPC 23. Voltage Noise Density vs. Frequency

APPLICATIONS

Figure 1 is a block diagram of the configuration of an XGA-compatible (1024 × 768) TFT color panel with the ADD8702 providing gamma correction reference voltages to the source drivers and an integrated V_{COM} driver for LCD common node.

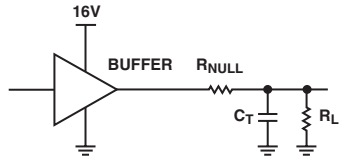


Figure 2. Bandwidth Measurement Information

Panel size and resolution determine the number of gamma reference voltages required. For a 256-grayscale level, 8-bit color scheme, 6×2 external reference nodes should be sufficient to match the characteristics of the LCD driver to the characteristics of the actual LCD panel for improved picture quality. External reference gamma correction voltages are often generated using a simple resistor ladder. Using the ADD8702, the resistor ladder is incorporated in the IC for reduced cost and number of components.

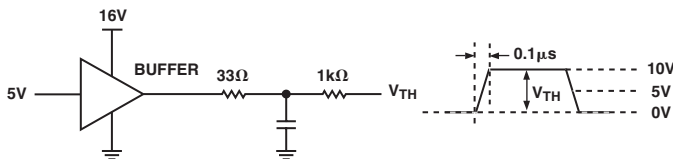


Figure 3. Transient Load Regulation Test Circuit

The ADD8702 is designed to meet the rail-to-rail capability needed by the application, yet offers the lowest cost per channel solution. The ADD8702 gamma buffers offer 10 mA continuous drive current capability. To be more competitive, the design maximizes the die area by allowing specific channels to swing to the positive rail and negative rail. So it is imperative that the channels swinging close to the supply rail be used for the positive gamma references and the channels swinging close to GND be used for the negative gamma references. The V_{COM} buffer can handle up to 35 mA continuous output current and can drive up to 1,000 pF pure capacitive load. Provision is available to adjust the V_{COM} voltage to a desired level. Refer to Figure 4 for an example of an application circuit for adjusting the output of the V_{COM} buffer.

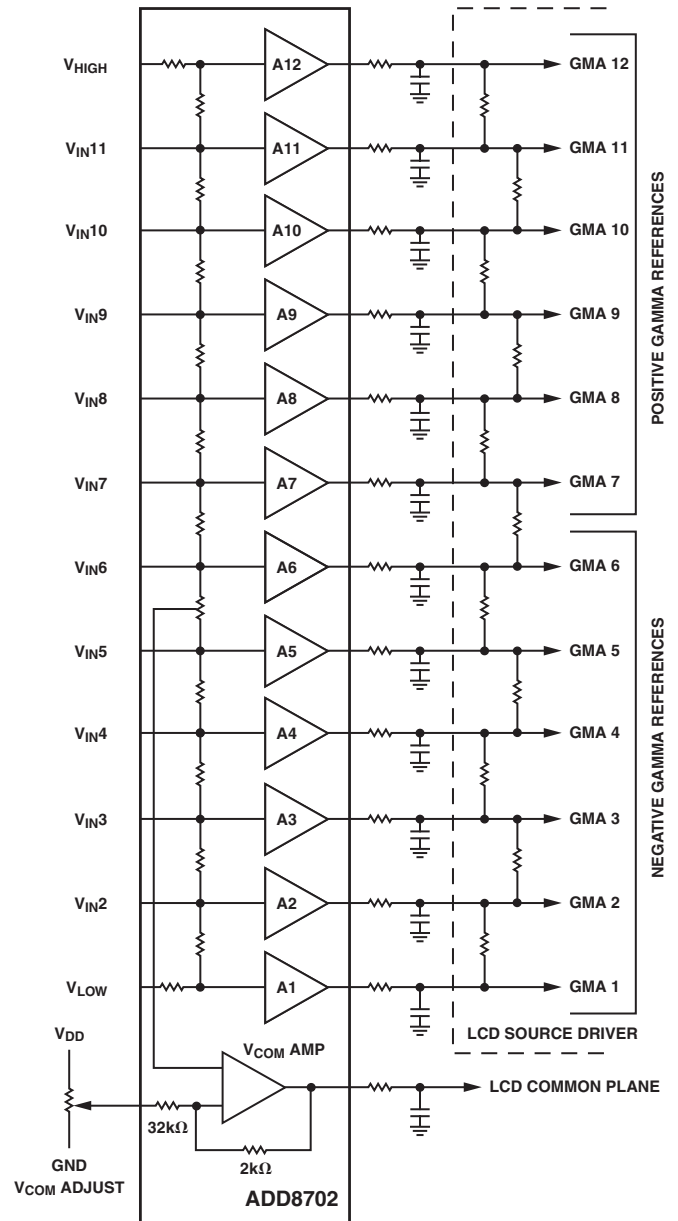


Figure 4. Application Circuit

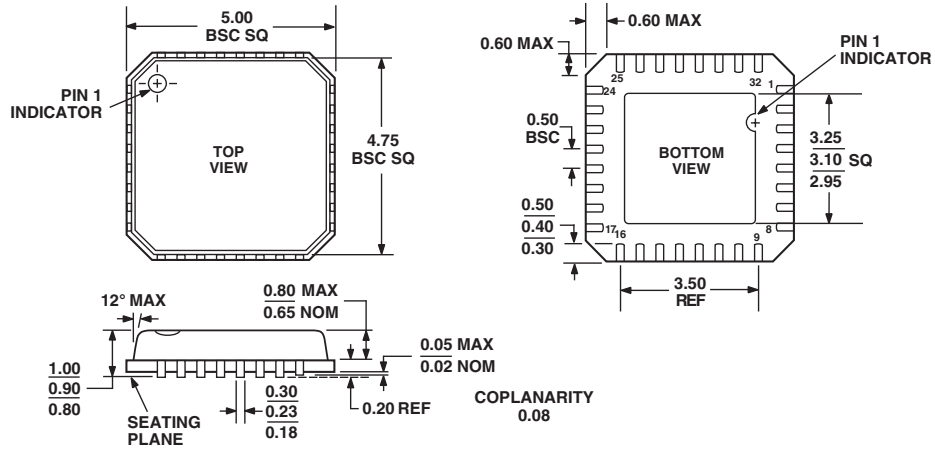
Table I. ADD8702 – 000 Mask Option, Resistor Tap Points ($0 \leq x \leq 500$) $V_{DD} = 12.5\text{ V}$, $V_{HIGH} = 12.5\text{ V}$, and $V_{LOW} = \text{GND}$

	Tap Point (x)	Voltage	Unit
VGMA1	8	0.2	V
VGMA2	57	1.43	V
VGMA3	84	2.11	V
VGMA4	115	2.89	V
VGMA5	139	3.48	V
VGMA6	194	4.86	V
VGMA7	218	5.45	V
VGMA8	298	7.45	V
VGMA9	371	9.29	V
VGMA10	418	10.45	V
VGMA11	442	11.04	V
VGMA12	488	12.2	V
V_{COM}	200	5	V

OUTLINE DIMENSIONS

32-Lead Lead Frame Chip Scale Package [LFCSP]
(CP-32)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VHHD-2