

### FEATURES

**AD5251: Dual 64-position resolution**  
**AD5252: Dual 256-position resolution**  
**1 kΩ, 10 kΩ, 50 kΩ, 100 kΩ**  
**Nonvolatile memory<sup>1</sup> stores wiper setting w/write protection**  
**Power-on refreshed with EEMEM settings in 300 μs typ**  
**EEMEM rewrite time = 540 μs typ**  
**Resistance tolerance stored in nonvolatile memory**  
**12 extra bytes in EEMEM for user-defined information**  
**I<sup>2</sup>C compatible serial interface**  
**Direct read/write access of RDAC<sup>2</sup> and EEMEM registers**  
**Predefined linear increment/decrement commands**  
**Predefined ±6 dB step change commands**  
**Synchronous or asynchronous dual channel update**  
**Wiper setting read back**  
**4 MHz bandwidth—1 kΩ version**  
**Single supply 2.7 V to 5.5 V**  
**Dual supply ±2.25 V to ±2.75 V**  
**2 slave address decoding bits allow operation of 4 devices**  
**100-year typical data retention T<sub>A</sub> = 55°C**  
**Operating temperature –40°C to +85°C**

### APPLICATIONS

**Mechanical potentiometer replacement**  
**General purpose DAC replacement**  
**LCD panel V<sub>COM</sub> adjustment**

### GENERAL DESCRIPTION

The AD5251/AD5252 are dual-channel, I<sup>2</sup>C, nonvolatile memory, digitally controlled potentiometers with 64/256 positions, respectively. These devices perform the same electronic adjustment functions as mechanical potentiometers, trimmers, and variable resistors. The parts' versatile programmability allows multiple modes of operation, including read/write access in the RDAC and EEMEM registers, increment/decrement of resistance, resistance changes in ±6 dB scales, wiper setting readback, and extra EEMEM for storing user-defined information such as memory data for other components, look-up table, or system identification information.

The AD5251/AD5252 allow the host I<sup>2</sup>C controllers to write any of the 64- or 256-step wiper settings in the RDAC registers and store them in the EEMEM. Once the settings are stored,

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**White LED brightness adjustment**  
**RF base station power amp bias control**  
**Programmable gain and offset control**  
**Programmable voltage-to-current conversion**  
**Programmable power supply**  
**Sensor calibrations**

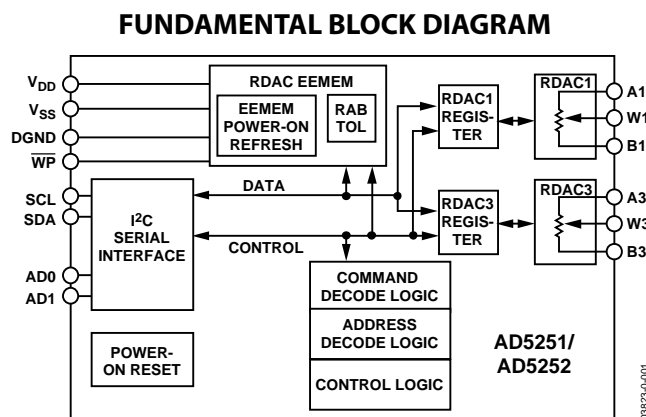


Figure 1.

<sup>1</sup>The terms nonvolatile memory and EEMEM are used interchangeably.

<sup>2</sup>The terms digital potentiometer and RDAC are used interchangeably.

they are restored automatically to the RDAC registers at system power-on; the settings can also be restored dynamically.

The AD5251/AD5252 provide additional increment, decrement, +6 dB step change, and –6 dB step change in synchronous or asynchronous channel update modes. The increment and decrement functions allow stepwise linear adjustments, while ±6 dB step changes are equivalent to doubling or halving the RDAC wiper setting. These functions are useful for steep-slope nonlinear adjustments such as white LED brightness and audio volume control. The parts have a patented resistance tolerance storing function which enable the user to access the EEMEM and obtain the absolute end-to-end resistance values of the RDACs for precision applications.

The AD5251/AD5252 are available in TSSOP-14 packages in 1 kΩ, 10 kΩ, 50 kΩ, and 100 kΩ options and all parts can operate over the –40°C to +85°C extended industrial temperature range.

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**REVISION HISTORY****6/04—Revision 0: Initial Version**

## ELECTRICAL CHARACTERISTICS

1 k $\Omega$  Version.  $V_{DD} = 3\text{ V} \pm 10\%$  or  $5\text{ V} \pm 10\%$ ;  $V_{SS} = 0\text{ V}$  or  $V_{DD}/V_{SS} = \pm 2.5\text{ V} \pm 10\%$ ;  $V_A = +V_{DD}$ ,  $V_B = 0\text{ V}$ ,  $-40^\circ\text{C} < T_A < +85^\circ\text{C}$ , unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ <sup>1</sup>	Max	Unit
<b>DC CHARACTERISTICS</b>						
<b>RHEOSTAT MODE</b>						
Resolution	N	AD5251/AD5252			6/8	Bits
Resistor Differential Nonlinearity <sup>2</sup>	R-DNL	$R_{WB}, R_{WA} = NC, V_{DD} = 5.5\text{ V}, \text{AD5251}$	-0.5	$\pm 0.2$	+0.5	LSB
		$R_{WB}, R_{WA} = NC, V_{DD} = 5.5\text{ V}, \text{AD5252}$	-1	$\pm 0.25$	+1	LSB
		$R_{WB}, R_{WA} = NC, V_{DD} = 2.7\text{ V}, \text{AD5251}$	-0.75	$\pm 0.3$	+0.75	LSB
		$R_{WB}, R_{WA} = NC, V_{DD} = 2.7\text{ V}, \text{AD5252}$	-1.5	$\pm 0.3$	+1.5	LSB
Resistor Nonlinearity <sup>2</sup>	R-INL	$R_{WB}, R_{WA} = NC, V_{DD} = 5.5\text{ V}, \text{AD5251}$	-0.5	$\pm 0.2$	+0.5	LSB
		$R_{WB}, R_{WA} = NC, V_{DD} = 5.5\text{ V}, \text{AD5252}$	-2	$\pm 0.5$	+2	LSB
		$R_{WB}, R_{WA} = NC, V_{DD} = 2.7\text{ V}, \text{AD5251}$	-1	+2.5	+4	LSB
		$R_{WB}, R_{WA} = NC, V_{DD} = 2.7\text{ V}, \text{AD5252}$	-2	+9	+14	LSB
Nominal Resistor Tolerance	$\Delta R_{AB}/R_{AB}$	$T_A = 25^\circ\text{C}$	-30		+30	%
Resistance Temperature Coefficient	$(\Delta R_{AB}/R_{AB}) \times 10^6/\Delta T$			650		ppm/ $^\circ\text{C}$
Wiper Resistance	$R_W$	$I_W = 1\text{ V}/R, V_{DD} = 5\text{ V}$		75	130	$\Omega$
		$I_W = 1\text{ V}/R, V_{DD} = 3\text{ V}$		200	300	$\Omega$
Channel Resistance Matching	$\Delta R_{AB1}/\Delta R_{AB3}$			0.15		%
<b>DC CHARACTERISTIC POTENTIOMETER DIVIDER MODE</b>						
Differential Nonlinearity <sup>3</sup>	DNL	AD5251	-0.5	$\pm 0.1$	+0.5	LSB
		AD5252	-1	$\pm 0.25$	+1	LSB
Integral Nonlinearity <sup>3</sup>	INL	AD5251	-0.5	$\pm 0.2$	+0.5	LSB
		AD5252	-2	$\pm 0.5$	+2	LSB
Voltage Divider Temperature Coefficient	$(\Delta V_W/V_W) \times 10^6/\Delta T$	Code = half scale		25		ppm/ $^\circ\text{C}$
Full-Scale Error	$V_{WFSE}$	Code = full scale, $V_{DD} = 5.5\text{ V}, \text{AD5251}$	-5	-3	0	LSB
		Code = full scale, $V_{DD} = 5.5\text{ V}, \text{AD5252}$	-16	-11	0	LSB
		Code = full scale, $V_{DD} = 2.7\text{ V}, \text{AD5251}$	-6	-4	0	LSB
		Code = full scale, $V_{DD} = 2.7\text{ V}, \text{AD5252}$	-23	-16	0	LSB
Zero-Scale Error	$V_{WZSE}$	Code = zero scale, $V_{DD} = 5.5\text{ V}, \text{AD5251}$	0	3	5	LSB
		Code = zero scale, $V_{DD} = 5.5\text{ V}, \text{AD5252}$	0	11	16	LSB
		Code = zero scale, $V_{DD} = 2.7\text{ V}, \text{AD5251}$	0	4	6	LSB
		Code = zero scale, $V_{DD} = 2.7\text{ V}, \text{AD5252}$	0	15	20	LSB
<b>RESISTOR TERMINALS</b>						
Voltage Range <sup>4</sup>	$V_A, V_B, V_W$		$V_{SS}$		$V_{DD}$	V
Capacitance <sup>5</sup> Ax, Bx	$C_A, C_B$	$f = 1\text{ kHz}$ , measured to GND, Code = half scale		85		pF
Capacitance <sup>5</sup> Wx	$C_W$	$f = 1\text{ kHz}$ , measured to GND, Code = half scale		95		pF
Common-Mode Leakage Current	$I_{CM}$	$V_A = V_B = V_{DD}/2$		0.01	1	$\mu\text{A}$
<b>DIGITAL INPUTS and OUTPUTS</b>						
Input Logic High	$V_{IH}$	$V_{DD} = 5\text{ V}, V_{SS} = 0\text{ V}$	2.4			V
		$V_{DD}/V_{SS} = 2.7\text{ V}/0\text{ V}$ or $V_{DD}/V_{SS} = \pm 2.5\text{ V}$	2.1			V
Input Logic Low	$V_{IL}$	$V_{DD} = 5\text{ V}, V_{SS} = 0\text{ V}$			0.8	V
Output Logic High (SDA)	$V_{OH}$	$R_{PULL-UP} = 2.2\text{ k}\Omega$ to $V_{DD} = 5\text{ V}, V_{SS} = 0\text{ V}$	4.9			V
Output Logic Low (SDA)	$V_{OL}$	$R_{PULL-UP} = 2.2\text{ k}\Omega$ to $V_{DD} = 5\text{ V}, V_{SS} = 0\text{ V}$			0.4	V

# AD5251/AD5252

Parameter	Symbol	Conditions	Min	Typ <sup>1</sup>	Max	Unit
Leakage Current	$I_{WP}$	$\overline{WP} = V_{DD}$			5	$\mu A$
A0 Leakage Current	$I_{A0}$	A0 = GND			3	$\mu A$
Input Leakage Current (Other than $\overline{WP}$ and A0)	$I_I$	$V_{IN} = 0 V$ or $V_{DD}$			$\pm 1$	$\mu A$
Input Capacitance <sup>5</sup>	$C_I$			5		pF
<b>POWER SUPPLIES</b>						
Single-Supply Power Range	$V_{DD}$	$V_{SS} = 0 V$	2.7		5.5	V
Dual-Supply Power Range	$V_{DD}/V_{SS}$		$\pm 2.25$		$\pm 2.75$	V
Positive Supply Current	$I_{DD}$	$V_{IH} = V_{DD}$ or $V_{IL} = GND$		5	15	$\mu A$
Negative Supply Current	$I_{SS}$	$V_{IH} = V_{DD}$ or $V_{IL} = GND$ , $V_{DD} = +2.5 V$ , $V_{SS} = -2.5 V$		-5	-15	$\mu A$
EEMEM Data Storing Mode Current	$I_{DD\_STORE}$	$V_{IH} = V_{DD}$ or $V_{IL} = GND$		35		mA
EEMEM Data Restoring Mode Current <sup>6</sup>	$I_{DD\_RESTORE}$	$V_{IH} = V_{DD}$ or $V_{IL} = GND$		2.5		mA
Power Dissipation <sup>7</sup>	$P_{DISS}$	$V_{IH} = V_{DD} = 5 V$ or $V_{IL} = GND$			0.075	mW
Power Supply Sensitivity	PSS	$\Delta V_{DD} = 5 V \pm 10\%$ $\Delta V_{DD} = 3 V \pm 10\%$	-0.025 -0.04	0.01 0.02	0.025 0.04	%/% %/%
<b>DYNAMIC CHARACTERISTICS<sup>5, 8</sup></b>						
Bandwidth -3 dB	BW	$R_{AB} = 1 k\Omega$		4		MHz
Total Harmonic Distortion	THD	$V_A = 1 V$ rms, $V_B = 0 V$ , $f = 1 kHz$		0.05		%
$V_W$ Settling Time	$t_s$	$V_A = V_{DD}$ , $V_B = 0 V$		0.2		$\mu s$
Resistor Noise Voltage	$e_{N\_WB}$	$R_{WB} = 500 \Omega$ , $f = 1 kHz$ (thermal noise only)		3		$nV/\sqrt{Hz}$
Digital Crosstalk	$C_T$	$V_A = V_{DD}$ , $V_B = 0 V$ , measure $V_W$ with adjacent RDAC making full-scale change		-80		dB
Analog Coupling	$C_{AT}$	Signal input at A1 and measure the output at W3, $f = 1 kHz$		-72		dB

<sup>1</sup> Typical represents the average reading at 25°C and  $V_{DD} = 5 V$ .

<sup>2</sup> Resistor position nonlinearity error (R-INL) is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic, except R-DNL of AD5252 1 k $\Omega$  version at  $V_{DD} = 2.7 V$ ,  $I_W = V_{DD}/R$  for both  $V_{DD} = 3 V$  or  $V_{DD} = 5 V$ .

<sup>3</sup> INL and DNL are measured at  $V_W$  with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter.  $V_A = V_{DD}$  and  $V_B = 0 V$ . DNL specification limits of  $\pm 1$  LSB maximum are guaranteed monotonic operating conditions.

<sup>4</sup> Resistor Terminals A, B, and W have no limitations on polarity with respect to each other.

<sup>5</sup> Guaranteed by design and not subject to production test.

<sup>6</sup> cmd 0 NOP should be activated after cmd 1 to minimize  $I_{DD\_READ}$  current consumption.

<sup>7</sup>  $P_{DISS}$  is calculated from  $I_{DD} \times V_{DD} = 5 V$ .

<sup>8</sup> All dynamic characteristics use  $V_{DD} = 5 V$ .

10 k $\Omega$ , 50 k $\Omega$ , 100 k $\Omega$  Versions.  $V_{DD} = +3\text{ V} \pm 10\%$  or  $+5\text{ V} \pm 10\%$ .  $V_{SS} = 0\text{ V}$  or  $V_{DD}/V_{SS} = \pm 2.5\text{ V} \pm 10\%$ .  $V_A = +V_{DD}$ ,  $V_B = 0\text{ V}$ ,  $-40^\circ\text{C} < T_A < +85^\circ\text{C}$ , unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ <sup>1</sup>	Max	Unit
DC CHARACTERISTICS						
RHEOSTAT MODE						
Resolution	N	AD5251/AD5252			6/8	Bits
Resistor Differential NL <sup>2</sup>	R-DNL	$R_{WB}, R_{WA} = \text{NC}$ , AD5251	-0.75	$\pm 0.1$	+0.75	LSB
		$R_{WB}, R_{WA} = \text{NC}$ , AD5252	-1	$\pm 0.25$	+1	LSB
Resistor Nonlinearity <sup>2</sup>	R-INL	$R_{WB}, R_{WA} = \text{NC}$ , AD5251	-0.75	$\pm 0.25$	+0.75	LSB
		$R_{WB}, R_{WA} = \text{NC}$ , AD5252	-2.5	$\pm 1$	+2.5	LSB
Nominal Resistor Tolerance	$\Delta R_{AB}/R_{AB}$	$T_A = 25^\circ\text{C}$	-20		+20	%
Resistance Temperature Coefficient	$(\Delta R_{AB}/R_{AB}) \times 10^6/\Delta T$			650		ppm/ $^\circ\text{C}$
Wiper Resistance	$R_W$	$I_W = 1\text{ V/R}$ , $V_{DD} = 5\text{ V}$		75	130	$\Omega$
		$I_W = 1\text{ V/R}$ , $V_{DD} = 3\text{ V}$		200	300	$\Omega$
Channel Resistance Matching	$\Delta R_{AB1}/\Delta R_{AB2}$	$R_{AB} = 10\text{ k}\Omega$ , 50 k $\Omega$		0.15		%
		$R_{AB} = 100\text{ k}\Omega$		0.05		%
DC CHARACTERISTICS						
POTENTIOMETER DIVIDER MODE						
Differential Nonlinearity <sup>3</sup>	DNL	AD5251	-0.5	$\pm 0.1$	+0.5	LSB
		AD5252	-1	$\pm 0.3$	+1	LSB
Integral Nonlinearity	INL	AD5251	-0.5	$\pm 0.15$	+0.5	LSB
		AD5252	-1.5	$\pm 0.5$	+1.5	LSB
Voltage Divider Temperature Coefficient	$(\Delta V_W/V_W) \times 10^6/\Delta T$	Code = half scale		15		ppm/ $^\circ\text{C}$
Full-Scale Error	$V_{WFSE}$	Code = full scale, AD5251	-1	-0.3	0	LSB
		Code = full scale, AD5252	-3	-1	0	LSB
Zero-Scale Error	$V_{WZSE}$	Code = zero scale, AD5251	0	0.3	1	LSB
		Code = zero scale, AD5252	0	1.2	3	LSB
RESISTOR TERMINALS						
Voltage Range <sup>4</sup>	$V_A, V_B, V_W$		$V_{SS}$		$V_{DD}$	V
Capacitance <sup>5</sup> Ax, Bx	$C_A, C_B$	$f = 1\text{ kHz}$ , measured to GND, Code = half scale		85		pF
Capacitance <sup>5</sup> Wx	$C_W$	$f = 1\text{ kHz}$ , measured to GND, Code = half scale		95		pF
Common-Mode Leakage Current	$I_{CM}$	$V_A = V_B = V_{DD}/2$		0.01	1	$\mu\text{A}$
DIGITAL INPUTS and OUTPUTS						
Input Logic High	$V_{IH}$	$V_{DD} = 5\text{ V}$ , $V_{SS} = 0\text{ V}$	2.4			V
		$V_{DD}/V_{SS} = +2.7\text{ V}/0\text{ V}$ or $V_{DD}/V_{SS} = \pm 2.5\text{ V}$	2.1			V
Input Logic Low	$V_{IL}$	$V_{DD} = 5\text{ V}$ , $V_{SS} = 0\text{ V}$			0.8	V
		$V_{DD}/V_{SS} = +2.7\text{ V}/0\text{ V}$ or $V_{DD}/V_{SS} = \pm 2.5\text{ V}$			0.6	V
Output Logic High (SDA)	$V_{OH}$	$R_{PULL-UP} = 2.2\text{ k}\Omega$ to $V_{DD} = 5\text{ V}$ , $V_{SS} = 0\text{ V}$	4.9			V
Output Logic Low (SDA)	$V_{OL}$	$R_{PULL-UP} = 2.2\text{ k}\Omega$ to $V_{DD} = 5\text{ V}$ , $V_{SS} = 0\text{ V}$			0.4	V
Leakage Current	$I_{WP}$	$\overline{WP} = V_{DD}$			5	$\mu\text{A}$
A0 Leakage Current	$I_{A0}$	A0 = GND			3	$\mu\text{A}$
Input Leakage Current (Other than $\overline{WP}$ and A0)	$I_i$	$V_{IN} = 0\text{ V}$ or $V_{DD}$			$\pm 1$	$\mu\text{A}$
Input Capacitance <sup>5</sup>	$C_i$			5		pF
POWER SUPPLIES						
Single-Supply Power Range	$V_{DD}$	$V_{SS} = 0\text{ V}$	2.7		5.5	V

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Parameter	Symbol	Conditions	Min	Typ <sup>1</sup>	Max	Unit
Dual-Supply Power Range	$V_{DD}/V_{SS}$		±2.25		±2.75	V
Positive Supply Current	$I_{DD}$	$V_{IH} = V_{DD}$ or $V_{IL} = GND$		5	15	µA
Negative Supply Current	$I_{SS}$	$V_{IH} = V_{DD}$ or $V_{IL} = GND$ , $V_{DD} = +2.5 V$ , $V_{SS} = -2.5 V$		-5	-15	µA
EEMEM Data Storing Mode Current	$I_{DD\_STORE}$	$V_{IH} = V_{DD}$ or $V_{IL} = GND$ , $T_A = 0^{\circ}C$ to $85^{\circ}C$		35		mA
EEMEM Data Restoring Mode Current <sup>6</sup>	$I_{DD\_RESTORE}$	$V_{IH} = V_{DD}$ or $V_{IL} = GND$ , $T_A = 0^{\circ}C$ to $85^{\circ}C$		2.5		mA
Power Dissipation <sup>7</sup>	$P_{DISS}$	$V_{IH} = V_{DD} = 5 V$ or $V_{IL} = GND$			0.075	mW
Power Supply Sensitivity	PSS	$\Delta V_{DD} = 5 V \pm 10\%$	-0.005	+0.002	+0.005	%/%
		$\Delta V_{DD} = 3 V \pm 10\%$	-0.01	+0.002	+0.01	%/%
<b>DYNAMIC CHARACTERISTICS<sup>5, 8</sup></b>						
-3 dB Bandwidth	BW	$R_{AB} = 10 k\Omega/50 k\Omega/100 k\Omega$		400/80/40		kHz
Total Harmonic Distortion	THD <sub>W</sub>	$V_A = 1 V_{rms}$ , $V_B = 0 V$ , $f = 1 kHz$		0.05		%
$V_W$ Settling Time	$t_s$	$V_A = V_{DD}$ , $V_B = 0 V$ , $R_{AB} = 10 k\Omega/50 k\Omega/100 k\Omega$		1.5/7/14		µs
Resistor Noise Voltage	$e_{N\_WB}$	10 kΩ/50 kΩ/100 kΩ, code = midscale, $f = 1 kHz$ (thermal noise only)		9/20/29		nV/ $\sqrt{Hz}$
Digital Crosstalk	$C_T$	$V_A = V_{DD}$ , $V_B = 0 V$ , Measure $V_W$ with adjacent RDAC making full scale change		-80		dB
Analog Coupling	$C_{AT}$	Signal input at A1 and measure output at W3, $f = 1 kHz$		-72		dB

<sup>1</sup> Typical represents the average reading at 25°C and  $V_{DD} = 5 V$ .

<sup>2</sup> Resistor position nonlinearity error (R-INL) is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic, except R-DNL of AD5252 1 kΩ version at  $V_{DD} = 2.7 V$ ,  $I_W = V_{DD}/R$  for both  $V_{DD} = 3 V$  or  $V_{DD} = 5 V$ .

<sup>3</sup> INL and DNL are measured at  $V_W$  with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter.  $V_A = V_{DD}$  and  $V_B = 0 V$ . DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.

<sup>4</sup> Resistor Terminals A, B, and W have no limitations on polarity with respect to each other.

<sup>5</sup> Guaranteed by design and not subject to production test.

<sup>6</sup> cmd 0 NOP should be activated after cmd 1 to minimize  $I_{DD\_READ}$  current consumption.

<sup>7</sup>  $P_{DISS}$  is calculated from  $I_{DD} \times V_{DD} = 5 V$ .

<sup>8</sup> All dynamic characteristics use  $V_{DD} = 5 V$ .

**INTERFACE TIMING CHARACTERISTICS**

Guaranteed by design, not subject to production test. See Figure 3 for location of measured values. All input control voltages are specified with  $t_R = t_F = 2.5$  ns (10% to 90% of 3 V), and timed from a voltage level of 1.5 V. Switching characteristics are measured using both  $V_{DD} = 3$  V and 5 V.

**Table 3. Interface Timing and EEMEM Reliability Characteristics (All Parts).**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>INTERFACE TIMING</b>						
SCL Clock Frequency	$f_{SCL}$				400	kHz
tBUF Bus Free Time between STOP and START	$t_1$		1.3			$\mu$ s
t <sub>HD,STA</sub> Hold Time (Repeated START)	$t_2$	After this period, the first clock pulse is generated	0.6			$\mu$ s
t <sub>LOW</sub> Low Period of SCL Clock	$t_3$		1.3			$\mu$ s
t <sub>HIGH</sub> High Period of SCL Clock	$t_4$		0.6			$\mu$ s
t <sub>SU,STA</sub> Setup Time For START Condition	$t_5$		0.6			$\mu$ s
t <sub>HD,DAT</sub> Data Hold Time	$t_6$		0		0.9	$\mu$ s
t <sub>SU,DAT</sub> Data Setup Time	$t_7$		100			ns
t <sub>F</sub> Fall Time of Both SDA and SCL Signals	$t_8$				300	ns
t <sub>R</sub> Rise Time of Both SDA and SCL Signals	$t_9$				300	ns
t <sub>SU,STO</sub> Setup Time for STOP Condition	$t_{10}$		0.6			$\mu$ s
EEMEM Data Storing Time	$t_{EEMEM\_STORE}$			26		ms
EEMEM Data Restoring Time at Power-On <sup>1</sup>	$t_{EEMEM\_RESTORE1}$	$V_{DD}$ rise time dependent. Measure without decoupling capacitors at $V_{DD}$ and $V_{SS}$ .		300		$\mu$ s
EEMEM Data Restoring Time Upon Restore Command or RESET Operation <sup>1</sup>	$t_{EEMEM\_RESTORE2}$	$V_{DD} = 5$ V		300		$\mu$ s
EEMEM Rewritable Time (delay time after Power On or RESET before EEMEM can be written)	$t_{EEMEM\_REWRITE}$			540		$\mu$ s
<b>FLASH/EE MEMORY RELIABILITY</b>						
Endurance <sup>2</sup>			100			kCycles
Data Retention <sup>3</sup>				100		Years

<sup>1</sup> During power-up, all outputs preset to midscale before restoring to the final EEMEM contents. RDAC0 has the shortest, whereas RDAC3 has the longest EEMEM data restoring time.

<sup>2</sup> Retention lifetime equivalent at junction temperature  $T_J = 55^\circ\text{C}$  per JEDEC Std. 22, Method A117. Retention lifetime based on an activation energy of 0.6 eV derates with junction temperature.

<sup>3</sup> When the part is not in operation, the SDA and SCL pins should be pulled to high. When these pins are pulled to low, the I<sup>2</sup>C interface at these pins conducts current of about 0.8 mA at  $V_{DD} = 5.5$  V and 0.2 mA at  $V_{DD} = 2.7$  V.

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 4.

Parameter	Rating
$V_{DD}$ to GND	-0.3 V, +7 V
$V_{SS}$ to GND	+0.3 V, -7 V
$V_{DD}$ to $V_{SS}$	7 V
$V_A, V_B, V_W$ to GND	$V_{SS}, V_{DD}$
Maximum Current	
IWB, IWA Pulsed	$\pm 20$ mA
$I_{WB}$ Continuous ( $R_{WB} \leq 1$ k $\Omega$ , A Open) <sup>1</sup>	$\pm 5$ mA
$I_{WA}$ Continuous ( $R_{WA} \leq 1$ k $\Omega$ , B Open)	$\pm 5$ mA
$I_{AB}$ Continuous ( $R_{AB} = 1$ k $\Omega$ /10 k $\Omega$ /50 k $\Omega$ /100 k $\Omega$ )	$\pm 5$ mA/ $\pm 500$ $\mu$ A/ $\pm 100$ $\mu$ A/ $\pm 50$ $\mu$ A
Digital Inputs and Output Voltage to GND	0 V, 7 V
Operating Temperature Range	-40°C to +85°C
Maximum Junction Temperature ( $T_{JMAX}$ )	150°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
TSSOP-14 Thermal Resistance <sup>2</sup> $\theta_{JA}$	136°C/W

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

<sup>1</sup> Maximum terminal current is bounded by the maximum applied voltage across any two of the A, B, and W terminals at a given resistance, the maximum current handling of the switches, and the maximum power dissipation of the package.  $V_{DD} = 5$  V.

<sup>2</sup> Package power dissipation =  $(T_{JMAX} - T_A)/\theta_{JA}$ .

## ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.





## PIN CONFIGURATION AND FUNCTION DESCRIPTION

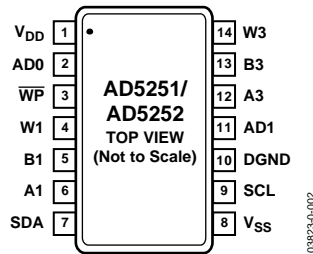


Figure 2. AD5251/AD5252 in TSSOP-14

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V <sub>DD</sub>	Positive Power Supply Pin. Connect +2.7 V to +5 V for single supply or $\pm 2.7$ V for dual supply, where $V_{DD} - V_{SS} \leq 5.5$ V. V <sub>DD</sub> must be able to source 35 mA for 26 ms when storing data to EEMEM.
2	AD0	I <sup>2</sup> C Device Address 0. AD0 and AD1 allow four AD5251/AD5252s to be addressed.
3	WP	Write Protect, Active Low. $V_{WP} \leq V_{DD} + 0.3$ V.
4	W1	Wiper Terminal of RDAC1. $V_{SS} \leq V_{W1} \leq V_{DD}$ . <sup>1</sup>
5	B1	B Terminal of RDAC1. $V_{SS} \leq V_{B1} \leq V_{DD}$ . <sup>1</sup>
6	A1	A Terminal of RDAC1. $V_{SS} \leq V_{A1} \leq V_{DD}$ . <sup>1</sup>
7	SDA	Serial Data Input/Output Pin. Shifts in one bit at a time on positive clock edges. MSB loaded first. Open-drain MOSFET requires pull-up resistor.
8	V <sub>SS</sub>	Negative Supply. Connect to 0 V for single supply or $-2.7$ V for dual supply, where $V_{DD} - V_{SS} \leq +5.5$ V. If V <sub>SS</sub> is used, other than grounded, in dual supply, V <sub>SS</sub> must be able to sink 35 mA for 26 ms when storing data to EEMEM.
9	SCL	Serial Input Register Clock Pin. Shifts in one bit at a time on positive clock edges. $V_{SCL} \leq (V_{DD} + 0.3$ V). Pull-up resistor is recommended for SCL to ensure minimum power.
10	DGND	Digital Ground. Connect to system analog ground at a single point.
11	AD1	I <sup>2</sup> C Device Address 1. AD0 and AD1 allow four AD5251/AD5252s to be addressed.
12	A3	A Terminal of RDAC3. $V_{SS} \leq V_{A3} \leq V_{DD}$ . <sup>1</sup>
13	B3	B Terminal of RDAC3. $V_{SS} \leq V_{B3} \leq V_{DD}$ . <sup>1</sup>
14	W3	W Terminal of RDAC3. $V_{SS} \leq V_{W3} \leq V_{DD}$ . <sup>1</sup>

<sup>1</sup> For quad-channel device software compatibility, the dual potentiometers in the parts are designated as RDAC1 and RDAC3.

### I<sup>2</sup>C INTERFACE TIMING DIAGRAM

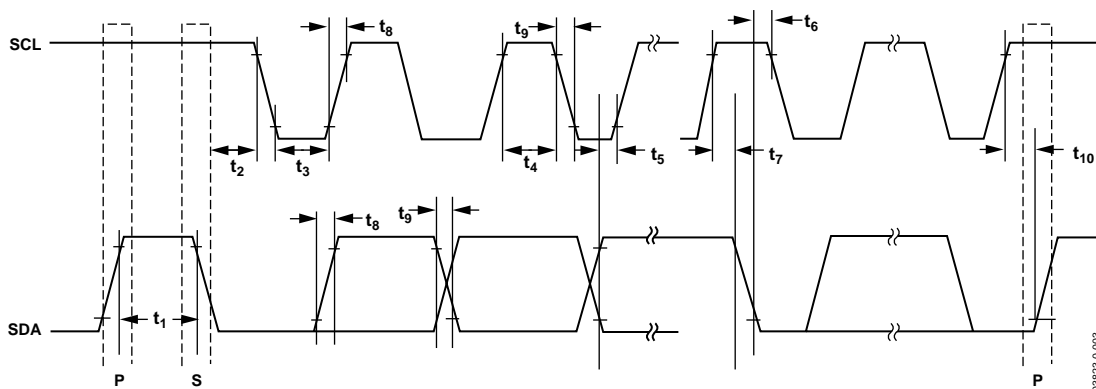


Figure 3. I<sup>2</sup>C Timing Diagram

# I<sup>2</sup>C INTERFACE GENERAL DESCRIPTION

FROM MASTER TO SLAVE  
 FROM SLAVE TO MASTER  
 S = START CONDITION  
 P = STOP CONDITION  
 A = ACKNOWLEDGE (SDA LOW)  
 $\bar{A}$  = NOT ACKNOWLEDGE (SDA HIGH)  
 $R/\bar{W}$  = READ ENABLE AT HIGH AND WRITE ENABLE AT LOW

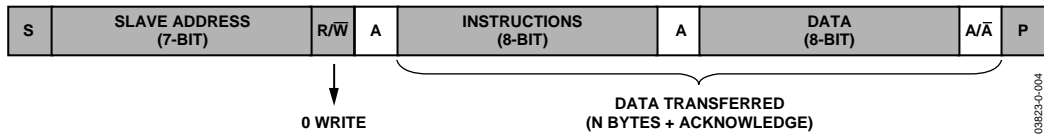


Figure 4. I<sup>2</sup>C—Master Writing Data to Slave

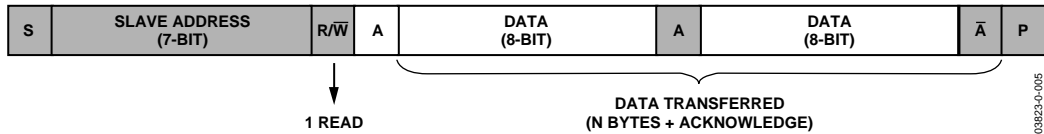


Figure 5. I<sup>2</sup>C—Master Reading Data from Slave

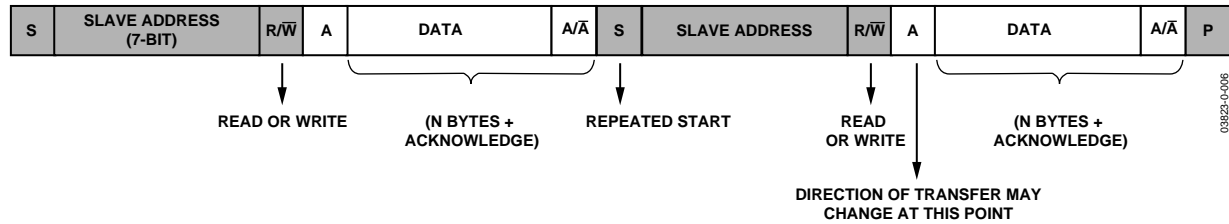


Figure 6. I<sup>2</sup>C—Combined Write/Read

## I<sup>2</sup>C INTERFACE DETAIL DESCRIPTION

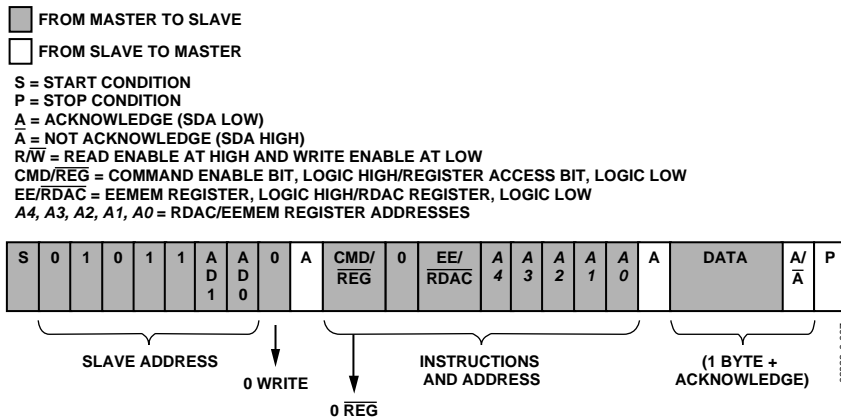


Figure 7. Single Write Mode

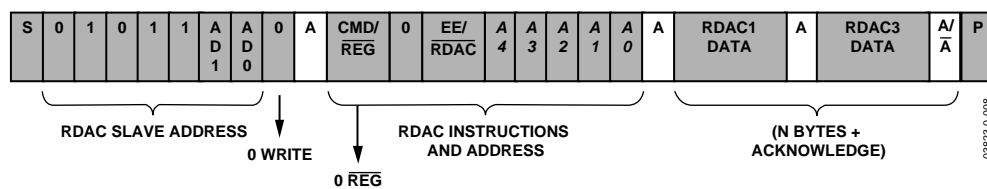


Figure 8. Consecutive Write Mode

Table 6. Addresses for Writing Data Byte Contents to RDAC Registers ( $R/\bar{W} = 0$ ,  $CMD/\bar{REG} = 0$ ,  $EE/\bar{RDAC} = 0$ )

A4	A3	A2	A1	A0	RDAC	Data Byte Description
0	0	0	0	0	Reserved	
0	0	0	0	1	RDAC1	6- or 8 bit wiper setting (2 MSBs of AD5251 are X)
0	0	0	1	0	Reserved	
0	0	0	1	1	RDAC3	6- or 8 bit wiper setting (2 MSBs of AD5251 are X)
0	0	1	0	0	Reserved	
:	:	:	:	:		
0	1	1	1	1	Reserved	

### RDAC/EEMEM WRITE

Setting the wiper position requires an RDAC write operation. The single write operation is shown in Figure 7, and the consecutive write operation is shown in Figure 8. In the consecutive write operation, if the RDAC is selected and the address starts at 00001, the first data byte goes to RDAC1 and the second data byte goes to RDAC3. The RDAC address is shown in Table 6.

While the RDAC wiper setting is controlled by a specific RDAC register, each RDAC register corresponds to a specific EEMEM location, which provides nonvolatile wiper storage functionality. The addresses are shown in Table 7. The single and consecutive write operations apply also to EEMEM write operations.

There are 12 nonvolatile memory locations: EEMEM4 to EEMEM15. Users can store a total of 12 bytes of information, such as memory data for other components, look-up tables, or system identification information.

In a write operation to the EEMEM registers, the device disables the I<sup>2</sup>C interface during the internal write cycle. Acknowledge polling is required to determine the completion of the write cycle. See EEMEM Write-Acknowledge Polling.

# AD5251/AD5252

**Table 7. Addresses for Writing (Storing) RDAC Settings and User-Defined Data to EEMEM Registers (R/W = 0, CMD/REG = 0, EE/RDAC = 1)**

A4	A3	A2	A1	A0	Data Byte Description
0	0	0	0	0	Reserved
0	0	0	0	1	Store RDAC1 setting to EEMEM1 <sup>1</sup>
0	0	0	1	0	Reserved
0	0	0	1	1	Store RDAC3 setting to EEMEM3 <sup>1</sup>
0	0	1	0	0	Store user data to EEMEM4
0	0	1	0	1	Store user data to EEMEM5
0	0	1	1	0	Store user data to EEMEM6
0	0	1	1	1	Store user data to EEMEM7
0	1	0	0	0	Store user data to EEMEM8
0	1	0	0	1	Store user data to EEMEM9
0	1	0	1	0	Store user data to EEMEM10
0	1	0	1	1	Store user data to EEMEM11
0	1	1	0	0	Store user data to EEMEM12
0	1	1	0	1	Store user data to EEMEM13
0	1	1	1	0	Store user data to EEMEM14
0	1	1	1	1	Store user data to EEMEM15

<sup>1</sup> User can store any of the 64 RDAC settings for AD5251 or any of the 256 RDAC settings for AD5252.

## RDAC/EEMEM Read

The AD5251/AD5252 provide two different RDAC or EEMEM read operations. For example, Figure 9 shows the method of reading the RDAC0 to RDAC3 contents without specifying the address, assuming Address RDAC0 was already selected from the previous operation. If RDAC\_N, other than Address 0, is

selected previously, readback starts with Address N, followed by N + 1, and so on.

Figure 10 illustrates a random RDAC or EEMEM read operation. This operation lets users specify which RDAC or EEMEM register is read by first issuing a dummy write command to change the RDAC address pointer, and then proceeding with the RDAC read operation at the new address location.

**Table 8. Addresses for Reading (Restoring) RDAC Settings and User Data from EEMEM (R/W = 1, CMD/REG = 0, EE/RDAC = 1)**

A4	A3	A2	A1	A0	Data Byte Description
0	0	0	0	0	Reserved
0	0	0	0	1	Read RDAC1 Setting from EEMEM1
0	0	0	1	0	Reserved
0	0	0	1	1	Read RDAC3 Setting from EEMEM3
0	0	1	0	0	Read user data from EEMEM4
0	0	1	0	1	Read user data from EEMEM5
0	0	1	1	0	Read user data from EEMEM6
0	0	1	1	1	Read user data from EEMEM7
0	1	0	0	0	Read user data from EEMEM8
0	1	0	0	1	Read user data from EEMEM9
0	1	0	1	0	Read user data from EEMEM10
0	1	0	1	1	Read user data from EEMEM11
0	1	1	0	0	Read user data from EEMEM12
0	1	1	0	1	Read user data from EEMEM13
0	1	1	1	0	Read user data from EEMEM14
0	1	1	1	1	Read user data from EEMEM15

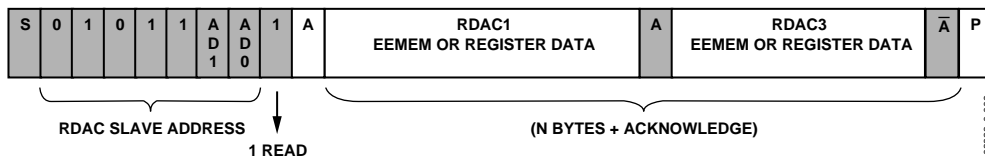


Figure 9. RDAC Current Read (Restricted to Previously Selected Address Stored in the Register).

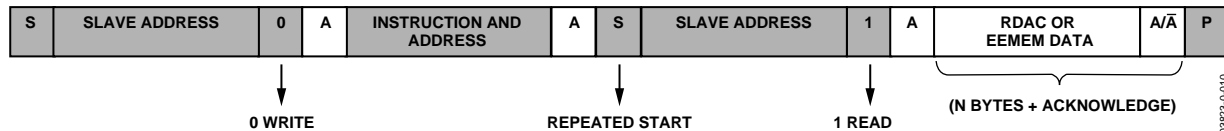


Figure 10. RDAC or EEMEM Random Read

**RDAC/EEMEM Quick Commands**

The AD5251/AD5252 feature 12 quick commands that facilitate easy manipulation of RDAC wiper settings and provide RDAC-to-EEMEM storing and restoring functions. The command

format is shown in Figure 11 and the command descriptions are shown in Table 9.

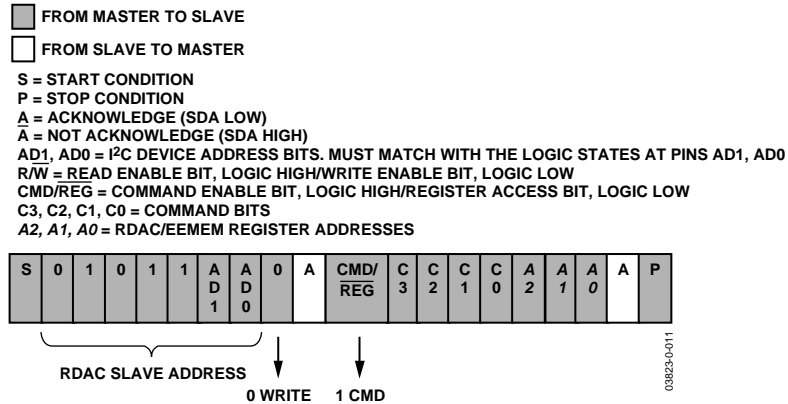


Figure 11. RDAC Quick Command Write (Dummy Write)

**Table 9. RDAC-to-EEMEM Interface and RDAC Operation Quick Command Bits (CMD/ $\overline{\text{REG}}$  = 1, A2 = 0)**

C3	C2	C1	C0	Command Description
0	0	0	0	NOP
0	0	0	1	Restore EEMEM (A1, A0) to RDAC (A1, A0) <sup>1</sup>
0	0	1	0	Store RDAC (A1, A0) to EEMEM (A1, A0)
0	0	1	1	Decrement RDAC (A1, A0) 6 dB
0	1	0	0	Decrement all RDACs 6 dB
0	1	0	1	Decrement RDAC (A1, A0) one step
0	1	1	0	Decrement all RDACs one step
0	1	1	1	Reset: Restore EEMEMs to all RDACs
1	0	0	0	Increment RDACs (A1, A0) 6 dB
1	0	0	1	Increment all RDACs 6 dB
1	0	1	0	Increment RDACs (A1, A0) one step
1	0	1	1	Increment all RDACs one step
1	1	0	0	Reserved
:	:	:	:	
1	1	1	1	Reserved

<sup>1</sup> This command leaves the device in the EEMEM read power state, which consumes power. Users should issue the NOP command to return the device to the idle state.

**Table 10. Address Table for Reading Tolerance (CMD/ $\overline{\text{REG}}$  = 0, EE/ $\overline{\text{RDAC}}$  = 1, A4 = 1)**

A4	A3	A2	A1	A0	Data Byte Description
0	0	0	0	0	Reserved
:	:	:	:	:	
1	1	0	0	1	Reserved
1	1	0	1	0	Sign and 7-bit integer values of RDAC1 tolerance (read only)
1	1	0	1	1	8-bit decimal value of RDAC1 tolerance (read only)
1	1	1	0	0	Reserved
1	1	1	0	1	Reserved
1	1	1	1	0	Sign and 7-bit integer values of RDAC3 tolerance (read only)
1	1	1	1	1	8-bit decimal value of RDAC3 tolerance (read only)

# AD5251/AD5252

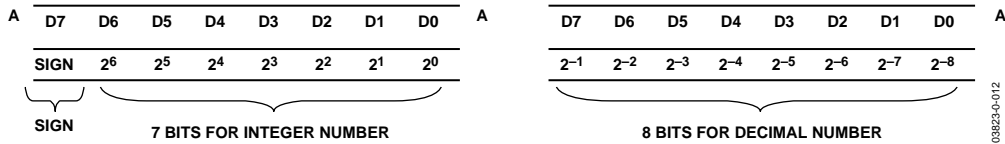


Figure 12. Format of Stored Tolerance in Sign Magnitude Format with Bit Position Descriptions. (Unit is percent. Only data bytes are shown.)

## R<sub>AB</sub> Tolerance Stored in Read-Only Memory

The AD5251/AD5252 feature patented R<sub>AB</sub> tolerances storage in the nonvolatile memory. The tolerance of each channel is stored in the memory during the factory production and can be read by users at any time. The knowledge of stored tolerance, which is the average of R<sub>AB</sub> over all codes (see Figure 28), allows users to predict R<sub>AB</sub> accurately. This feature is valuable for precision, rheostat mode, and open-loop applications where knowledge of absolute resistance is critical.

The stored tolerances reside in the read-only memory, and are expressed as a percentage. The tolerance is stored in two memory locations (see Table 10). The data format of the tolerance is in sign magnitude binary form. An example is shown in Figure 11. In the first memory location, the MSB is designated for the sign (0 = + and 1 = -) and the 7 LSBs are designated for the integer portion of the tolerance. In the second memory location, all eight data bits are designated for the decimal portion of tolerance. As shown in Table 10 and Figure 12 for example, if the rated R<sub>AB</sub> = 10 kΩ and the data readback from Address 11000 shows 0001 1100 and Address 11001 shows 0000 1111, then RDAC0 tolerance can be calculated as

$$\begin{aligned} \text{MSB: } 0 &= + \\ \text{Next 7 MSB: } 001\ 1100 &= 28 \\ \text{8 LSB: } 0000\ 1111 &= 15 \times 2^{-8} = 0.06 \\ \text{Tolerance} &= +28.06\% \text{ and therefore} \\ R_{AB\_ACTUAL} &= 12.806\ \text{k}\Omega \end{aligned}$$

## EEMEM Write-Acknowledge Polling

After each write operation to the EEMEM registers, an internal write cycle begins. The I<sup>2</sup>C interface of the device is disabled. To determine if the internal write cycle is complete and the I<sup>2</sup>C interface is enabled, interface polling can be executed. I<sup>2</sup>C interface polling can be conducted by sending a start condition followed by the slave address + the write bit. If the I<sup>2</sup>C interface responds with an ACK, the write cycle is complete and the interface is ready to proceed with further operations. Otherwise, I<sup>2</sup>C interface polling can be repeated until it succeeds. Commands 2 and 7 also require acknowledge polling.

## EEMEM Write Protection

Setting the  $\overline{\text{WP}}$  pin to a logic LOW after EEMEM programming protects the memory and RDAC registers from future write operations. In this mode, the EEMEM and RDAC read operations operate as normal. When write protection is enabled, Command 1 (Restore from EEMEM to RDAC) and Command 7 (Reset) function normally to allow RDAC settings to be refreshed from the EEMEM to the RDAC registers.

## I<sup>2</sup>C COMPATIBLE 2-WIRE SERIAL BUS

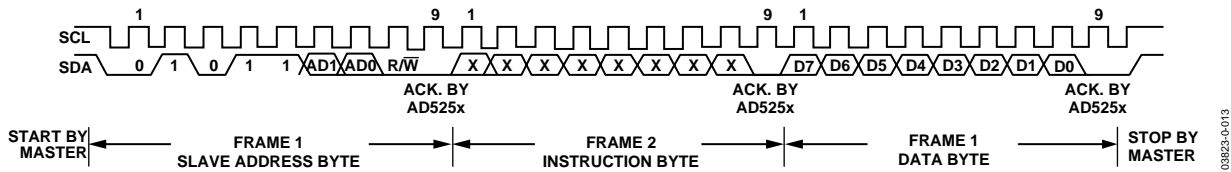


Figure 13. General I<sup>2</sup>C Write Pattern

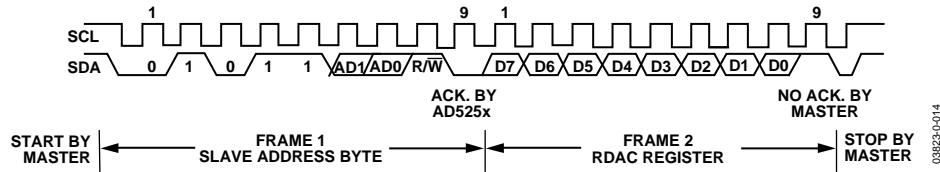


Figure 14. General I<sup>2</sup>C Read Pattern

The first byte of the AD5251/AD5252 is a slave address byte (see Figure 12 and Figure 13). It has a 7-bit slave address and an  $\overline{R/W}$  bit. The 5 MSBs of the slave address are 01011, and the following 2 LSBs are determined by the states of the AD1 and AD0 pins. AD1 and AD0 allow the user to place up to four parts on one bus.

AD5251/AD5252 can be controlled via an I<sup>2</sup>C compatible serial bus, and are connected to this bus as slave devices. The 2-wire I<sup>2</sup>C serial bus protocol (see Figure 13 and Figure 14) follows:

1. The master initiates a data transfer by establishing a start condition, such that SDA goes from high to low while SCL is high (see Figure 13). The following byte is the slave address byte, which consists of the 5 MSBs of a slave address defined as 01011. The next two bits are AD1 and AD0, I<sup>2</sup>C device address bits. Depending on the states of their AD1 and AD0 bits, four parts can be addressed on the same bus. The last LSB, the  $\overline{R/W}$  bit, determines whether data is read from or written to the slave device.

The slave whose address corresponds to the transmitted address responds by pulling the SDA line low during the ninth clock pulse (this is called an acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to or read from its serial register.

2. In the write mode (except when restoring EEMEM to the RDAC register), there is an instruction byte that follows the slave address byte. The MSB of the instruction byte is labeled  $\overline{CMD/REG}$ . MSB = 1 enables CMD, the command instruction byte; MSB = 0 enables general register writing. The third MSB in the instruction byte, labeled  $\overline{EE/RDAC}$ , is true only when MSB = 0 or is in general writing mode. EE enables the EEMEM register and REG enables the RDAC register. The 5 LSBs, A4 to A0, designate the

addresses of the EEMEM and RDAC registers, (see Figure 7 and Figure 8). When MSB = 1 or when in CMD mode, the four bits following MSB are C3 to C1, which correspond to 12 predefined EEMEM controls and quick commands; there also are four factory reserved commands. The 3 LSBs—A2, A1, and A0—are four addresses, but only 001 and 011 are used for RDAC1 and RDAC3, respectively (see Figure 10). After acknowledging the instruction byte, the last byte in the write mode is the data byte. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (see Figure 13).

3. In current read mode, the RDAC0 data byte immediately follows the acknowledgment of the slave address byte. After an acknowledgement, RDAC1 follows, then RDAC2, and so on (there is a slight difference in write mode, where the last eight data bits representing RDAC3 data are followed by a no acknowledge bit). Similarly, the transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL (see Figure 14). Another reading method, random read method, is shown in Figure 10.
4. When all data bits have been read or written, a stop condition is established by the master. A stop condition is defined as a low-to-high transition on the SDA line while SCL is high. In write mode, the master pulls the SDA line high during the 10th clock pulse to establish a stop condition (see Figure 13). In read mode, the master issues a no acknowledge for the ninth clock pulse, i.e., the SDA line remains high. The master then brings the SDA line low before the 10<sup>th</sup> clock pulse, which goes high to establish a stop condition (see Figure 14).

TYPICAL PERFORMANCE CHARACTERISTICS

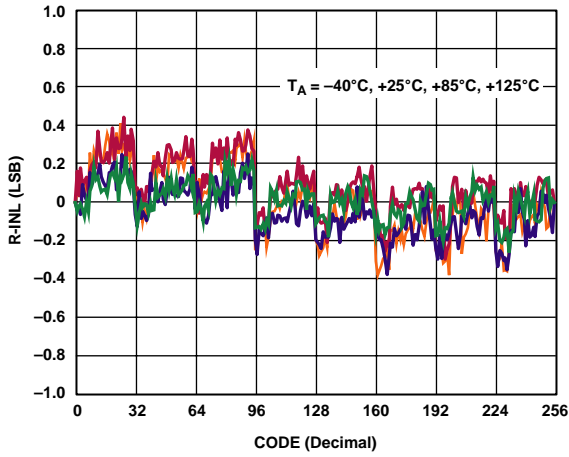


Figure 15. R-INL vs. Code

03823-0-015

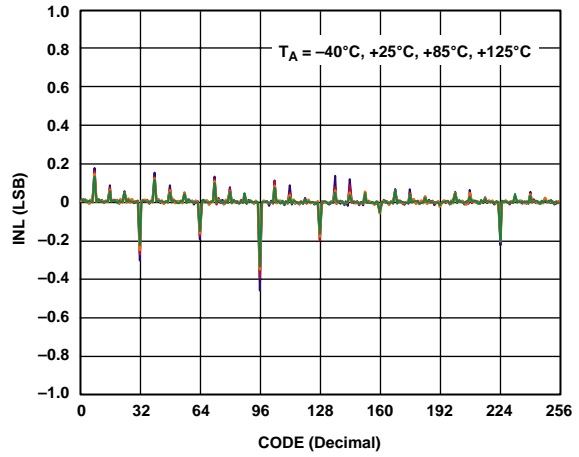


Figure 18. DNL vs. Code

03823-0-018

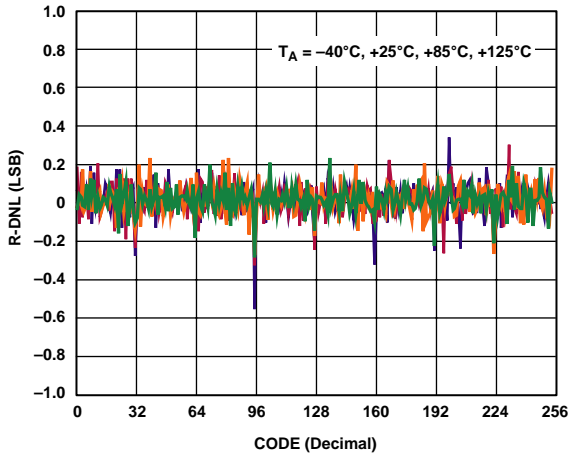


Figure 16. R-DNL vs. Code

03823-0-016

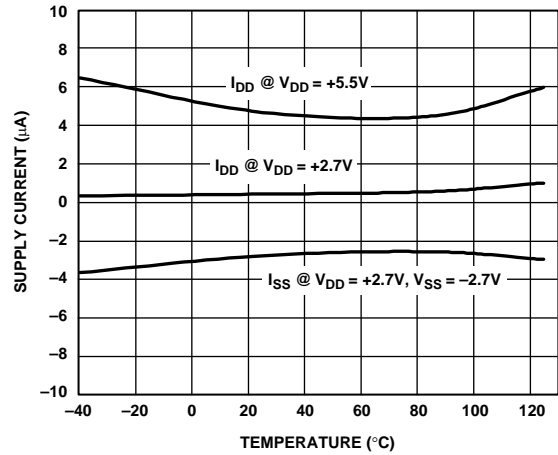


Figure 19. Supply Current vs. Temperature

03823-0-019

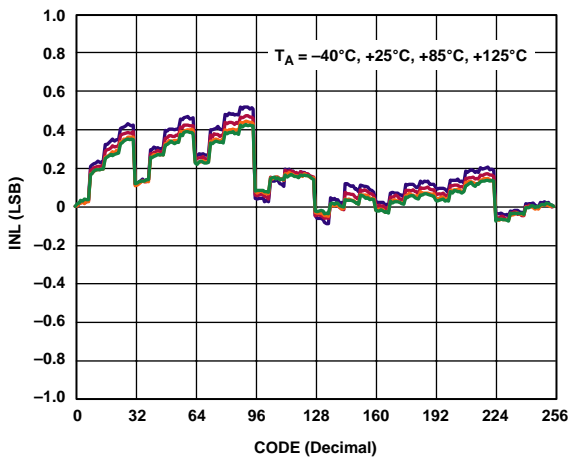


Figure 17. INL vs. Code

03823-0-017

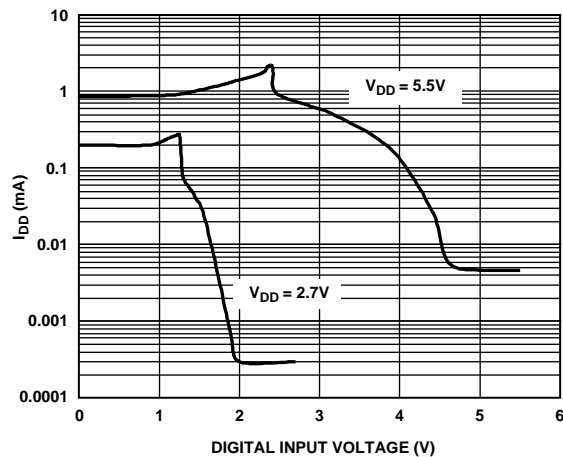


Figure 20. Supply Current vs. Digital Input Voltage,  $T_A = 25^\circ\text{C}$

03823-0-020



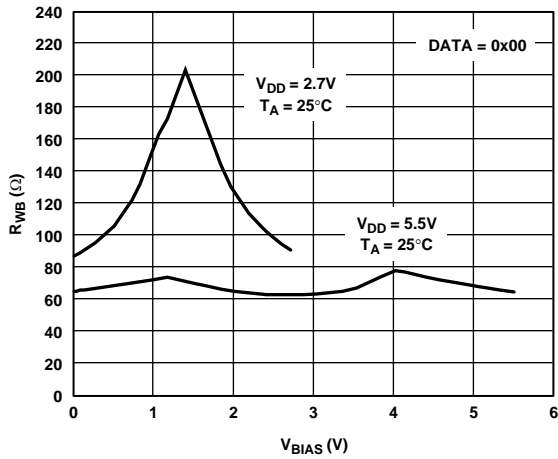


Figure 21. Wiper Resistance vs.  $V_{BIAS}$

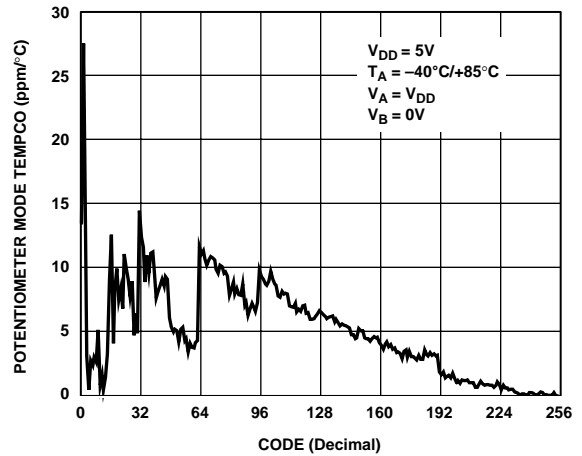


Figure 24. AD5252 Potentiometer Mode Tempco  $\Delta V_{WB}/\Delta T$  vs. Code

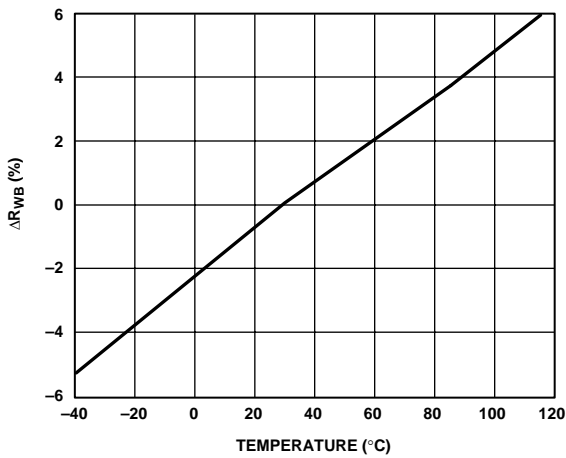


Figure 22. Change of  $R_{AB}$  vs. Temperature

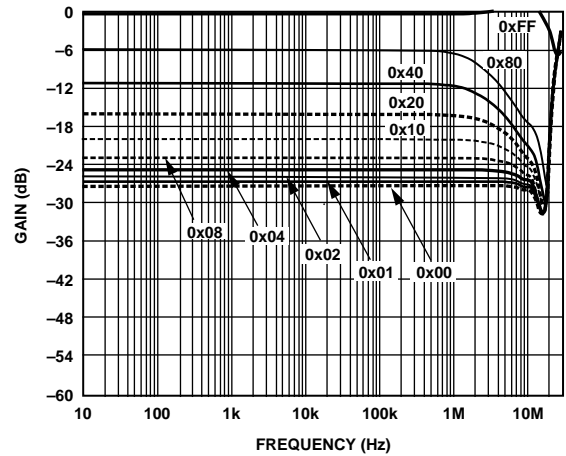


Figure 25. AD5252 Gain vs. Frequency vs. Code,  $R_{AB} = 1\text{ k}\Omega$

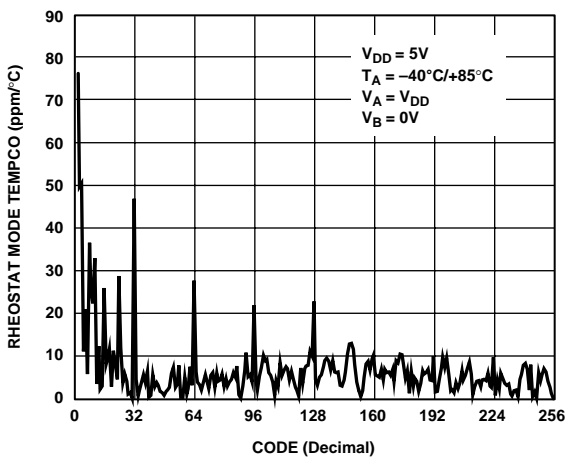


Figure 23. AD5252 Rheostat Mode Tempco  $\Delta R_{WB}/\Delta T$  vs. Code

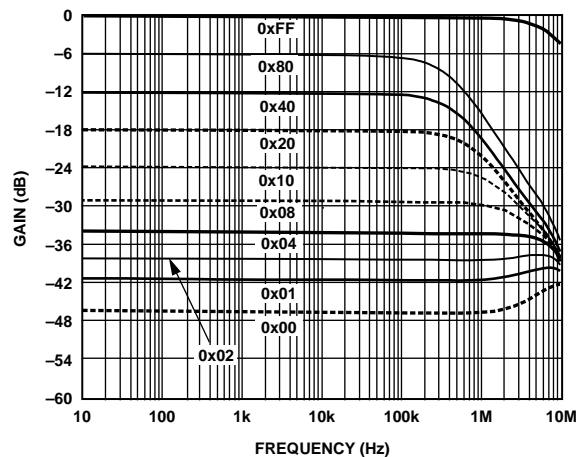


Figure 26. AD5252 Gain vs. Frequency vs. Code,  $R_{AB} = 10\text{ k}\Omega$

# AD5251/AD5252

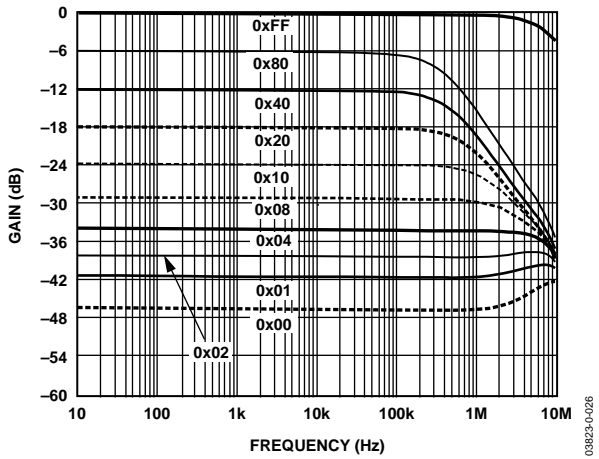


Figure 27. AD5252 Gain vs. Frequency vs. Code,  $R_{AB} = 50\text{ k}\Omega$

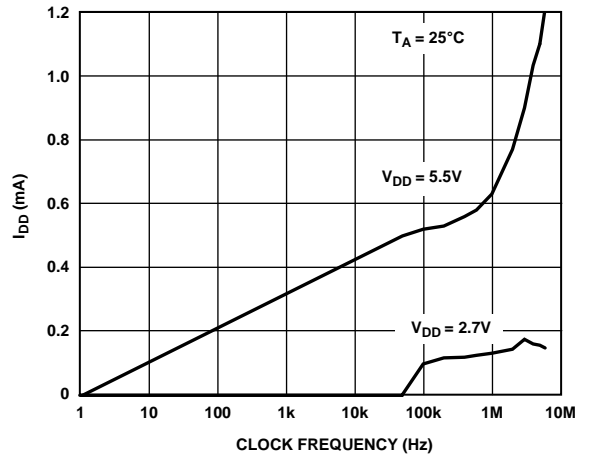


Figure 30. Supply Current vs. Digital Input Clock Frequency

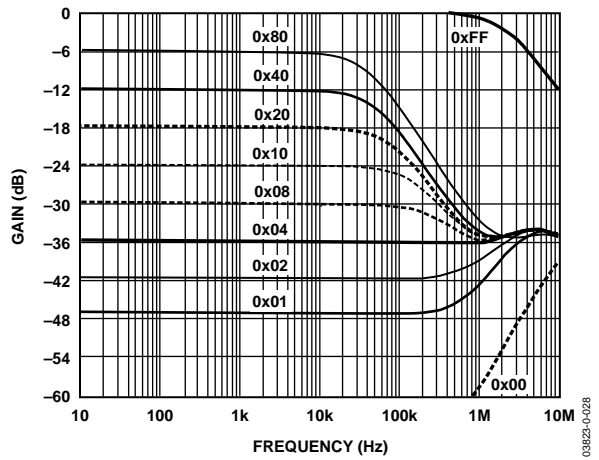


Figure 28. AD5252 Gain vs. Frequency vs. Code,  $R_{AB} = 100\text{ k}\Omega$

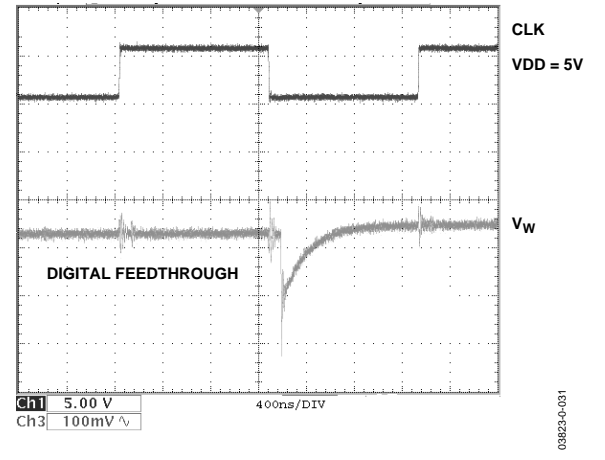


Figure 31. Clock Feedthrough and Midscale Transition Glitch

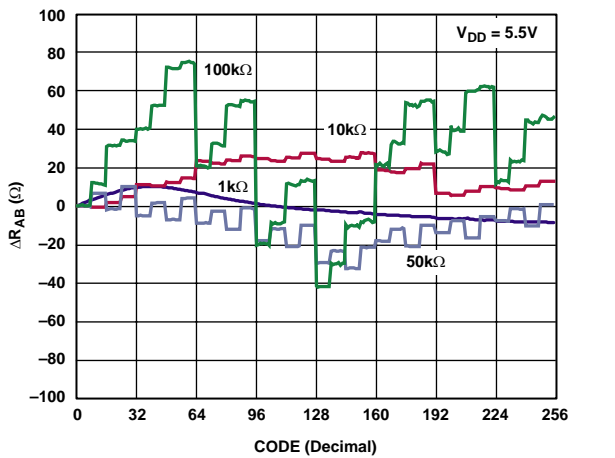


Figure 29. AD5252  $\Delta R_{AB}$  vs. Code,  $T_A = 25^\circ\text{C}$

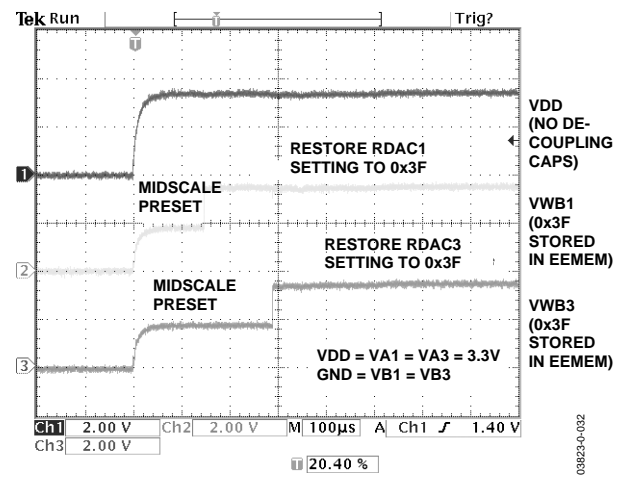


Figure 32.  $t_{EMEM\_RESTORE}$

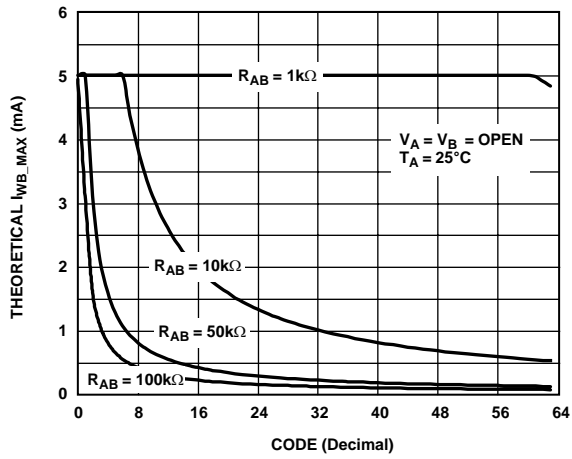


Figure 33. AD5251  $I_{WBmax}$  vs. Code

03823-0-033

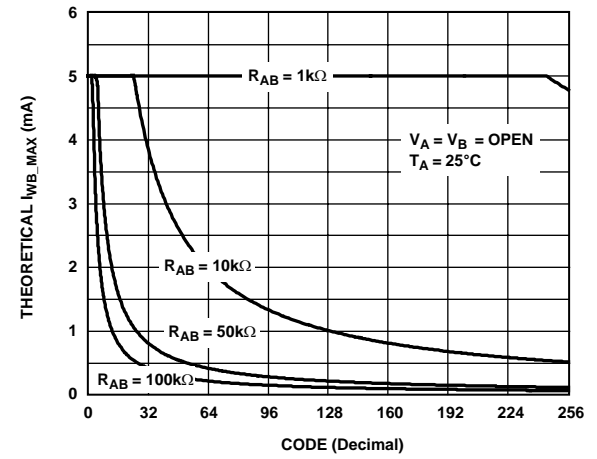


Figure 34. AD5252  $I_{WBmax}$  vs. Code

03823-0-034

## OPERATIONAL OVERVIEW

The AD5251/AD5252 are dual-channel digital potentiometers in 1 k $\Omega$ , 10 k $\Omega$ , 50 k $\Omega$ , or 100 k $\Omega$  that allow 64 and 256 linear resistance step adjustments. The AD5251/AD5252 employ double-gate CMOS EEPROM technology that allows resistance settings and user-defined data to be stored in the EEMEM registers. The EEMEM is nonvolatile, such that settings remain when power is removed. The RDAC wiper settings are restored from the non-volatile memory settings during device power-up and can also be restored at any time during operation.

The AD5251/AD5252 resistor wiper positions are determined by the RDAC register contents. The RDAC register acts like a scratch-pad register, allowing unlimited changes of resistance settings. RDAC register contents can be changed using the device's serial I<sup>2</sup>C interface. The format of the data-words and the commands to program the RDAC registers are discussed in the I2C Interface Detail Description section.

The four RDAC registers have corresponding EEMEM memory locations that provide nonvolatile storage of resistor wiper position settings. The AD5251/AD5252 provide commands to store the RDAC register contents to their respective EEMEM memory locations. During subsequent power-on sequences, the RDAC registers are automatically loaded with the stored value.

Whenever the EEMEM write operation is enabled, the device activates the internal charge pump and raises the EEMEM cell gate bias voltage to a high level, essentially erasing the current content in the EEMEM register and allowing subsequent storage of the new content. Saving data to an EEMEM register consumes about 35 mA of current and lasts about 26 ms. Because of charge pump operation, all RDAC channels may experience noise coupling during the EEMEM writing operation.

The EEMEM restore time in power-up or during operation is about 300  $\mu$ s. Note that the power up EEMEM refresh time depends on how fast V<sub>DD</sub> reaches its final value. As a result, any supply voltage decoupling capacitors limit the EEMEM restore time during power-up. Figure 32 shows the power up profile where V<sub>DD</sub>, without any decoupling capacitors connected to it, is applied with a digital signal. The device initially resets the measured RDACs to midscale before reaching their final values during EEMEM restoration.

In addition, users should issue a NOP Command 0 immediately after using Command 1 to restore the EEMEM setting to RDAC, to minimize supply current dissipation. Directly reading user data from EEMEM does not require similar NOP command execution.

In addition to the movement of data between RDAC registers and EEMEM memory, the AD5251/AD5252 provide other shortcut commands that facilitate the users' programming needs, as shown in Table 11.

**Table 11. AD5251/AD5252 Quick Commands**

Command	Description
0	NOP
1	Restore EEMEM content to RDAC. User should issue NOP immediately after this command to conserve power.
2	Store RDAC register setting to EEMEM.
3	Decrement RDAC 6 dB (shift data bits right).
4	Decrement all RDACs 6 dB (shift all data bits right).
5	Decrement RDAC one step.
6	Decrement all RDACs one step.
7	Reset EEMEM contents to all RDACs.
8	Increment RDAC 6 dB (shift data bits left).
9	Increment All RDACs 6 dB (shift all data bits left).
10	Increment RDAC one step.
11	Increment all RDACs one step.
12–15	Reserved.

### LINEAR INCREMENT AND DECREMENT COMMANDS

The increment and decrement commands (10, 11, 5, and 6) are useful for linear step adjustment applications. These commands simplify microcontroller software coding by allowing the controller to send just an increment or decrement command to the AD5251/AD5252. The adjustments can be directed to an individual RDAC or to all four RDACs.

### $\pm 6$ dB ADJUSTMENTS (DOUBLING/HALVING WIPER SETTING)

The AD5251/AD5252 accommodates  $\pm 6$  dB adjustments of the RDAC wiper positions by shifting the register contents to left/right for increment/decrement operations, respectively. Commands 3, 4, 8, and 9 can be used to increment or decrement the wiper positions in 6 dB steps synchronously or asynchronously.

Incrementing the wiper position by +6 dB is essentially doubling the RDAC register value, while decrementing by –6 dB is halving the register content. Internally, the AD5251/AD5252 use shift registers to shift the bits left and right to achieve a  $\pm 6$  dB increment or decrement. The maximum number of adjustments is nine and eight steps for increment from zero scale and decrement from full scale, respectively. These functions are useful for various audio/video level adjustments, especially for white LED brightness settings where human visual responses are more sensitive to large than small adjustments.

## DIGITAL INPUT/OUTPUT CONFIGURATION

SDA is a digital input/output with an open-drain MOSFET that requires a pull-up resistor for proper communication. On the other hand, SCL and  $\overline{WP}$  are digital inputs for which pull-up resistors are recommended to minimize the MOSFETs cross conduction current when the driving signals are lower than  $V_{DD}$ . SCL and  $\overline{WP}$  have ESD protection diodes, as shown in Figure 35 and Figure 36.

$\overline{WP}$  can be permanently tied to  $V_{DD}$  without a pull-up resistor if the write-protect feature is not used. If  $\overline{WP}$  is left floating, an internal current source pulls it low to enable write-protect. In applications where the device is not being programmed on a frequent basis, this allows the part to default to write-protect after any one-time factory programming or field calibration without the use of an on board pull-down resistor. Because there are protection diodes on all these inputs, their signal levels must not be greater than  $V_{DD}$  to prevent forward biasing of the diodes.

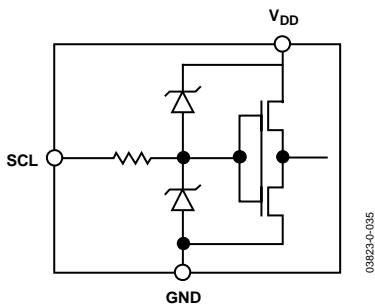


Figure 35. SCL Digital Input

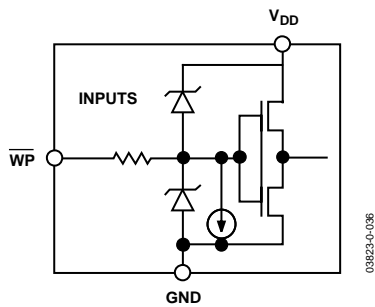


Figure 36. Equivalent  $\overline{WP}$  Digital Input

## MULTIPLE DEVICES ON ONE BUS

The AD5251/AD5252 are equipped with two addressing pins, AD1 and AD0, that allow up to four AD5251/AD5252s to be operated on one I<sup>2</sup>C bus. To achieve this result, the states of AD1 and AD0 on each device must first be defined. An example is shown in Table 12 and Figure 37. In I<sup>2</sup>C programming, each device is issued a different slave address—01011(AD1)(AD0)—to complete the addressing.

Table 12. Multiple Devices Addressing

AD1	AD0	Device Addressed
0	0	U1
0	1	U2
1	0	U3
1	1	U4

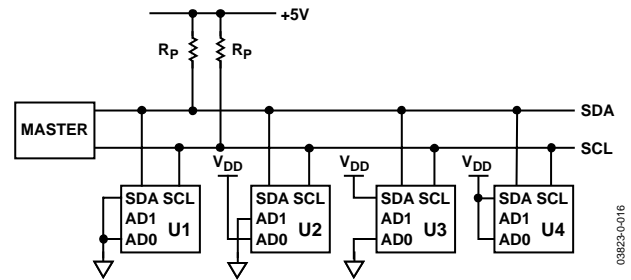


Figure 37. Multiple AD5251/AD5252s on a Single Bus

## TERMINAL VOLTAGE OPERATION RANGE

The AD5251/AD5252 are designed with internal ESD diodes for protection; these diodes also set the boundary of the terminal operating voltages. Positive signals present on Terminal A, B, or W that exceed  $V_{DD}$  are clamped by the forward biased diode. Similarly, negative signals on Terminal A, B, or W that are more negative than  $V_{SS}$  are also clamped (see Figure 38). In practice, users should not operate  $V_{AB}$ ,  $V_{WA}$ , and  $V_{WB}$  to be higher than the voltage across  $V_{DD}$  to  $V_{SS}$ , but  $V_{AB}$ ,  $V_{WA}$ , and  $V_{WB}$  have no polarity constraint.

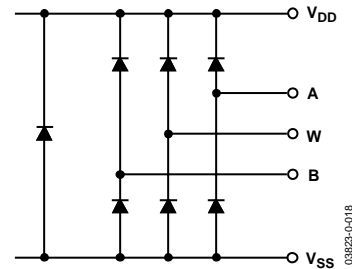


Figure 38. Maximum Terminal Voltages Set by  $V_{DD}$  and  $V_{SS}$

## POWER-UP AND POWER-DOWN SEQUENCES

Because the ESD protection diodes limit the voltage compliance at terminals A, B, and W (see Figure 38), it is important to power-on  $V_{DD}/V_{SS}$  before applying any voltage to Terminals A, B, and W. Otherwise, the diodes are forward-biased such that  $V_{DD}/V_{SS}$  are powered unintentionally and may affect the rest of the user's circuit. Similarly,  $V_{DD}/V_{SS}$  should be powered down last. The ideal power-up sequence is in the following order: GND,  $V_{DD}$ ,  $V_{SS}$ , digital inputs, and  $V_A/V_B/V_W$ . The order of powering  $V_A$ ,  $V_B$ ,  $V_W$ , and the digital inputs is not important, as long as they are powered after  $V_{DD}/V_{SS}$ .

# AD5251/AD5252

## LAYOUT AND POWER SUPPLY BIASING

It is always a good practice to employ a compact, minimum lead-length layout design. The leads to the input should be as direct as possible, with a minimum conductor length. Ground paths should have low resistance and low inductance.

Similarly, it is also good practice to bypass the power supplies with quality capacitors. Low equivalent series resistance (ESR) 1  $\mu\text{F}$  to 10  $\mu\text{F}$  tantalum or electrolytic capacitors should be applied at the supplies to minimize any transient disturbance and filter low frequency ripple. Figure 39 illustrates the basic supply bypassing configuration for the AD5251/AD5252.

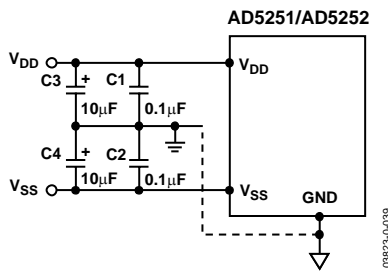


Figure 39. Power Supply Bypassing

The ground pin of the AD5251/AD5252 is used primarily as a digital ground reference. To minimize the digital ground bounce, the AD5251/AD5252 ground terminal should be joined remotely to the common ground (see Figure 39).

## DIGITAL POTENTIOMETER OPERATION

The structure of the RDAC is designed to emulate the performance of a mechanical potentiometer. The RDAC contains a string of resistor segments, with an array of analog switches acting as the wiper connection to the resistor array. The number of points is the resolution of the device. For example, the AD5251/AD5252 emulates 64 or 256 connection points with 64 or 256 equal resistance,  $R_S$ , allowing it to provide better than 1.5%/0.4% settability resolution.

Figure 40 provides an equivalent diagram of the connections between the three terminals that make up one channel of the RDAC. Switches  $SW_A$  and  $SW_B$  are always ON, while one of switches  $SW(0)$  to  $SW(2^N-1)$  is ON one at a time, depending on the setting decoded from the data bit. Because the switches are nonideal, there is a 75  $\Omega$  wiper resistance,  $R_W$ . Wiper resistance is a function of supply voltage and temperature; lower supply voltages and higher temperatures result in higher wiper resistances. Consideration of wiper resistance dynamics is important in applications where accurate prediction of output resistance is required.

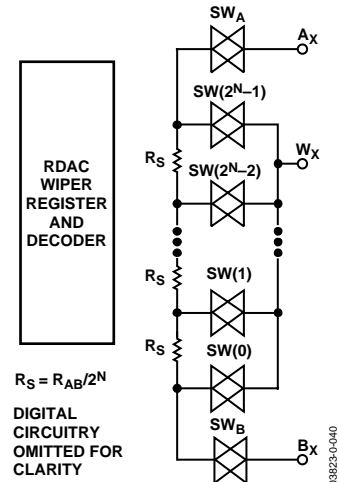


Figure 40. Equivalent RDAC Structure

## PROGRAMMABLE RHEOSTAT OPERATION

If either the W-to-B or W-to-A terminal is used as a variable resistor, the unused terminal can be opened or shorted with W; such operation is called rheostat mode (see Figure 41). The resistance tolerance can range  $\pm 20\%$ .

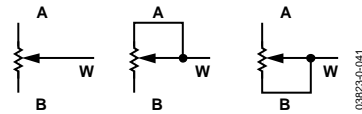


Figure 41. Rheostat Mode Configuration

The nominal resistance of the AD5251/AD5252 has 64 or 256 contact points accessed by the wiper terminal, plus the B terminal contact. The 6- or 8-bit data-word in the RDAC register is decoded to select one of the 64 or 256 settings. The wiper's first connection starts at the B terminal for Data 0x00. This B-terminal connection has a wiper contact resistance,  $R_W$ , of 75  $\Omega$ , regardless of the nominal resistance. The second connection (the AD5251 10 k $\Omega$  part) is the first tap point where  $R_{WB} = 231 \Omega$  ( $R_{WB} = R_{AB}/64 + R_W = 156 \Omega + 75 \Omega$ ) for Data 0x01, and so on. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at  $R_{WB} = 9893 \Omega$ . See Figure 40 for a simplified diagram of the equivalent RDAC circuit.

The general equation that determines the digitally programmed output resistance between W and B, is

$$\text{AD5251: } R_{WB}(D) = (D/64) \times R_{AB} + 75 \Omega \quad (1)$$

$$\text{AD5252: } R_{WB}(D) = (D/256) \times R_{AB} + 75 \Omega \quad (2)$$

Where  $D$  is the decimal equivalent data contained in the RDAC latch and  $R_{AB}$  is the nominal end-to-end resistance.

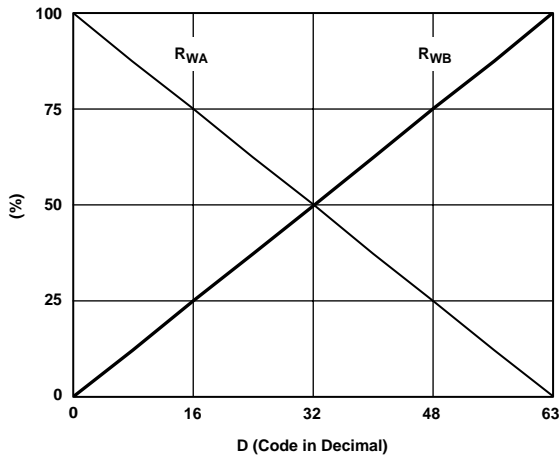


Figure 42. AD5251  $R_{WA}(D)$  and  $R_{WB}(D)$  vs. Decimal Code

Table 13.  $R_{WB}$  vs. Codes;  $R_{AB} = 10\text{ k}\Omega$ , A Terminal = Open

D (DEC)	$R_{WB}$ ( $\Omega$ )	Output State
63	9918	Full scale
32	5075	Midscale
1	231	1 LSB
0	75	Zero scale (wiper resistance)

Note that in the zero-scale condition, a  $75\ \Omega$  finite wiper resistance is present. Care should be taken to limit the current conduction between W and B in this state to no more than  $\pm 5\text{ mA}$  continuous for a total resistance of  $1\text{ k}\Omega$ , or a  $\pm 20\text{ mA}$  pulse, to avoid degradation or possible destruction of the internal switch contact.

Similar to the mechanical potentiometer, the resistance of the RDAC between Wiper W and Terminal A also produces a digitally controlled complementary resistance,  $R_{WA}$ . When these terminals are used, the B terminal can be opened. Setting the resistance value for  $R_{WA}$  starts at a maximum value of resistance and decreases as the data loaded in the latch increases in value (see Figure 40). The general equation for this operation is

$$AD5251: R_{WA}(D) = [(64 - D)/64] \times R_{AB} + 75\ \Omega \quad (3)$$

$$AD5252: R_{WA}(D) = [(256 - D)/256] \times R_{AB} + 75\ \Omega \quad (4)$$

Table 14.  $R_{WA}$  vs. Codes; AD5251,  $R_{AB}=10\text{ k}\Omega$ , B Terminal Open

D (DEC)	$R_{WA}$ ( $\Omega$ )	Output State
63	231	Full scale
32	5075	Midscale
1	9918	1 LSB
0	10075	Zero scale

The typical distribution of  $R_{AB}$  from channel-to-channel matches about  $\pm 0.15\%$  within a given device. On the other hand, device-to-device matching is process-lot dependent with  $\pm 20\%$  tolerance.

### PROGRAMMABLE POTENTIOMETER OPERATION

If all three terminals are used, the operation is called potentiometer mode and the most common configuration is the voltage divider operation (see Figure 43).

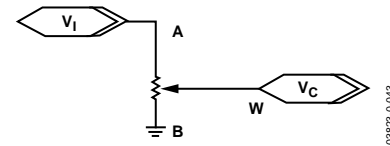


Figure 43. Potentiometer Mode Configuration

If the wiper resistance is ignored, the transfer function is simply

$$AD5251: V_W = \frac{D}{64} \times V_{AB} + V_B \quad (5)$$

$$AD5252: V_W = \frac{D}{256} \times V_{AB} + V_B \quad (6)$$

A more accurate calculation, which includes the wiper resistance effect, yields

$$V_W(D) = \frac{D}{2^N} \frac{R_{AB} + R_W}{R_{AB} + 2R_W} V_A \quad (7)$$

Where  $2^N$  is the number of steps. Unlike in rheostat mode operation where the tolerance is high, potentiometer mode operation yields an almost ratiometric function of  $D/2^N$  with a relatively small error contributed by the  $R_W$  terms. Therefore, the tolerance effect is almost cancelled. Similarly, the ratiometric adjustment also reduces the temperature coefficient effect to  $50\text{ ppm}/^\circ\text{C}$ , except at low value codes where  $R_W$  dominates.

Potentiometer mode operations include other applications such as op amp input, feedback resistor networks, and other voltage scaling applications. The A, W, and B terminals can in fact be input or output terminals, provided  $|V_A|$ ,  $|V_W|$ , and  $|V_B|$  do not exceed  $V_{DD}$  to  $V_{SS}$ .

## APPLICATIONS

### LCD PANEL $V_{COM}$ ADJUSTMENT

Large LCD panels usually require an adjustable  $V_{COM}$  voltage centered around 6 V to 8 V with  $\pm 1$  V swing and small steps adjustment. This example represents common DAC applications where the window of adjustments is small and centered at any level. High voltage and high resolution DACs can be used but it is far more cost-effective to use low voltage digital potentiometers with level shifting, such as the AD5251 or AD5252, to achieve the objective.

Assume a  $V_{COM}$  voltage requirement of  $6\text{ V} \pm 1\text{ V}$  with a  $\pm 20\text{ mV}$  step adjustment, as shown in Figure 44. The AD5252 can be configured in voltage divider mode with an op amp gain. With  $\pm 20\%$  tolerance accounted for by the AD5252, this circuit can still be adjusted from 5 V to 7 V with an 8 mV/step in the worst case.

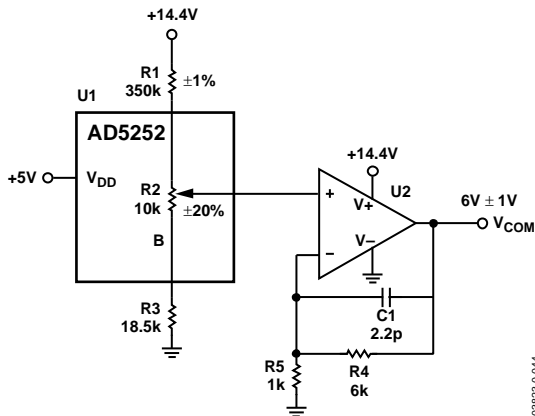


Figure 44. Apply 5 V Digital Potentiometer AD5251 in a  $6\text{ V} \pm 1\text{ V}$  Application.

### CURRENT-SENSING AMPLIFIER

The dual channel, synchronous update, and channel-to-channel resistance matching characteristics make the AD5251/AD5252 suitable for current sensing applications, such as LED brightness control. In the circuit shown in Figure 45, when RDAC1 and RDAC3 are programmed to the same settings, it can be shown that

$$V_o = \frac{D}{2^N - D} (V_2 - V_1) + V_{REF} \quad (8)$$

As a result, the current through a sense resistor connected between  $V_1$  and  $V_2$  can be known. The programmability of this circuit makes it adaptable to systems that require different sensitivities. If the op amp has very low offset and low bias current, the major source of error comes from the digital potentiometer channel-to-channel resistance mismatch, which is typically 0.15%. The circuit accuracy is about 9 bits, which is adequate for LED control and other general purpose applications.

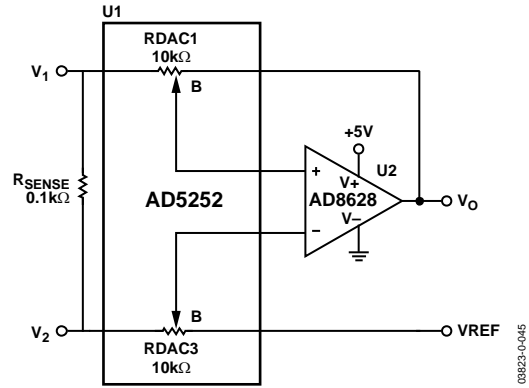


Figure 45. Current-Sensing Amplifier.

### ADJUSTABLE HIGH POWER LED DRIVER

Figure 46 shows a circuit that can drive three to four high power LEDs. The ADP1610 is an adjustable boost regulator that provides adequate headroom and current for the LEDs. Because its FB pin voltage is 1.2 V, the digital potentiometer AD5252 and the op amp form an average gain of 12 feedback networks that servo the sensing and feedback voltages. As a result, the voltage across  $R_{SET}$  is regulated around 0.1 V, depending on the AD5252's setting. An adjustable LED current is

$$I_{LED} = \frac{V_{R_{SET}}}{R_{SET}} \quad (9)$$

$R_{SET}$  should be small to conserve power but large enough to limit the maximum LED current. R3 should also be used in parallel with the AD5252 to limit the LED current within an achievable range.

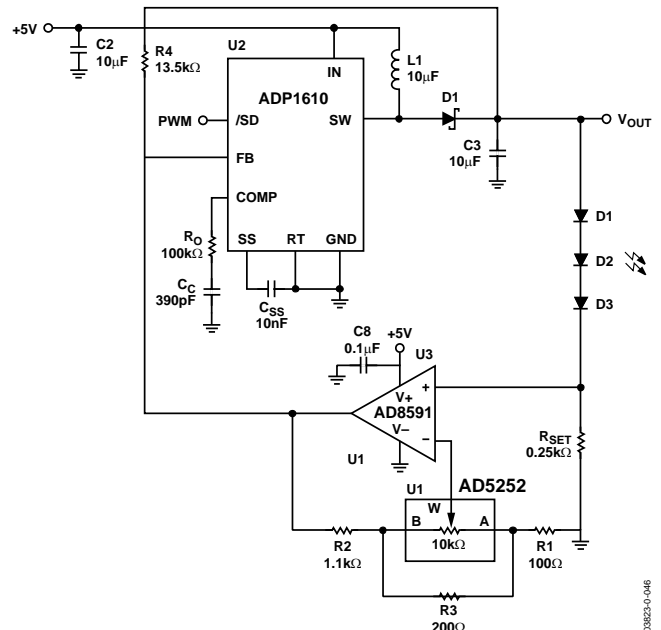


Figure 46. High Power Adjustable LED Driver



## OUTLINE DIMENSIONS

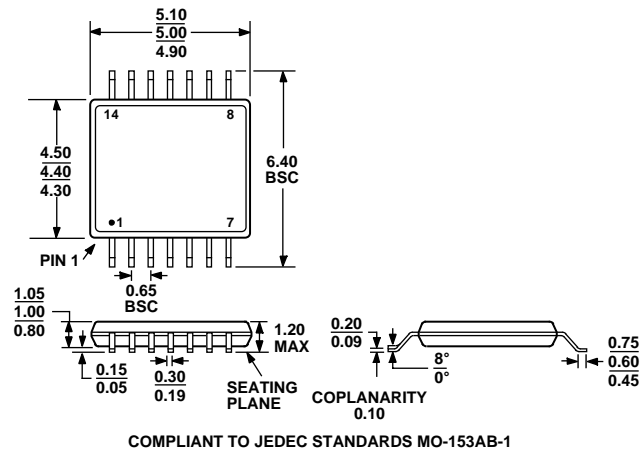


Figure 47. 14-Lead Thin Shrink Small Outline Package [TSSOP]  
(RU-14)  
Dimensions shown in millimeters

## ORDERING GUIDE

Model	Step	R <sub>AB</sub> (kΩ)	Temperature Range (°C)	Package Description	Package Option	Full Container Quantity	Branding <sup>1</sup>
AD5251BRU1	64	1	-40 to +85	TSSOP	RU-14	96	B1
AD5251BRU1-RL7	64	1	-40 to +85	TSSOP	RU-14	1,000	B1
AD5251BRU10	64	10	-40 to +85	TSSOP	RU-14	96	B10
AD5251BRU10-RL7	64	10	-40 to +85	TSSOP	RU-14	1,000	B10
AD5251BRU50	64	50	-40 to +85	TSSOP	RU-14	96	B50
AD5251BRU50-RL7	64	50	-40 to +85	TSSOP	RU-14	1,000	B50
AD5251BRU100	64	100	-40 to +85	TSSOP	RU-14	96	B100
AD5251BRU100-RL7	64	100	-40 to +85	TSSOP	RU-14	1,000	B100
AD5251EVAL	64	10		Evaluation Board		1	
AD5252BRU1	256	1	-40 to +85	TSSOP	RU-14	96	B1
AD5252BRU1-RL7	256	1	-40 to +85	TSSOP	RU-14	1,000	B1
AD5252BRU10	256	10	-40 to +85	TSSOP	RU-14	96	B10
AD5252BRU10-RL7	256	10	-40 to +85	TSSOP	RU-14	1,000	B10
AD5252BRU50	256	50	-40 to +85	TSSOP	RU-14	96	B50
AD5252BRU50-RL7	256	50	-40 to +85	TSSOP	RU-14	1,000	B50
AD5252BRU100	256	100	-40 to +85	TSSOP	RU-14	96	B100
AD5252BRU100-RL7	256	100	-40 to +85	TSSOP	RU-14	1,000	B100
AD5252EVAL	256	10		Evaluation Board		1	

<sup>1</sup> In the package marking, Line 1 shows the part number; Line 2 shows the branding information, such that B1 = 1 kΩ, B10 = 10 kΩ, B50 = 50 kΩ, and B100 = 100 kΩ; Line 3 shows the date code in YYWW.

**NOTES**

**NOTES**

**NOTES**

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