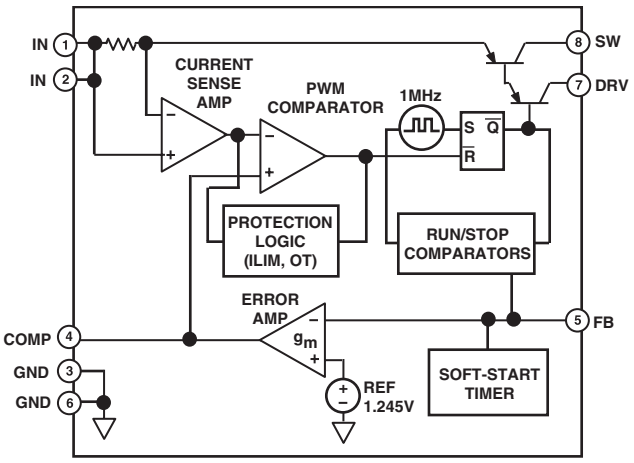
1 MHz, 750 mA Buck Regulator

Preliminary Technical Data — ADP3088

FEATURES
- 1 MHz PWM Frequency
- Automatic PWM to Power Saving Mode at Light Load
- Fully Integrated 1 A Power Switch
- 3% Output Regulation Accuracy over Temperature, Line, and Load
- 100% Duty Cycle Operation
- Simple Compensation
- Output Voltage: 1.25 V to 10.5 V
- Small Inductor and MLC Capacitors
- Low Quiescent Current while Pulse Skipping
- Thermal Shutdown
- Fully Integrated Soft Start
- Cycle-by-cycle Current Limit

APPLICATONS
- PDAs and Palmtop Computers
- Notebook Computers
- PCMCIA Cards
- Bus Products
- Portable Instruments

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADP3088 is a high frequency, non-synchronous PWM step-down DC-DC regulator with an integrated 1A power switch in a space-saving MSOP8 package. It provides high efficiency, excellent dynamic response, and is very simple to use.

The ADP3088's 1 MHz switching frequency allows for small, inexpensive external components, and the current mode control loop is simple to compensate and eases noise filtering. It operates in PWM current mode under heavy loads and saves energy at lighter loads by switching automatically into Power Saving mode. Soft start is integrated completely on chip, as is the cycle-by-cycle current limit.

Capable of operating from 2.5 V to 11 V input, it is ideal for many applications, including portable, battery power applications, where local point-of-use power regulation is required. Supporting output voltages down to 1.25 V, the ADP3088 is ideal to generate low voltage rails, providing the optimal solution in its class for delivering power efficiently, responsively, and simply with minimal printed circuit board area.

The device is specified over the industrial temperature range of -40 °C to +85°C.

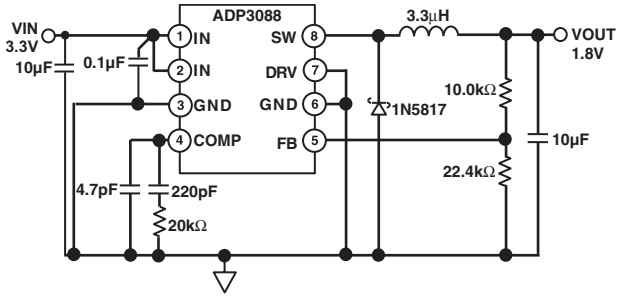


Figure 1. Typical Application

REV. PrK 3/28/02

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703

ADP3088–SPECIFICATIONS[1] (V_{IN} = +3.3 V, T_A = -40°C to +85°C, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
SUPPLY						
Input Voltage Range	V_{IN}	DRV = GND	2.5		11	V
Quiescent Current Operating	I_Q	V_{IN} = 10 V, I_L = 500 mA, DRV = GND		6		mA
Quiescent Current Operating	I_Q	No load		150	250	µA
Shutdown	I_{SD}	V_{COMP} = 0 V		15	40	
Ground Current	I_{GND}[2]					
Normal Operation		V_{IN} = 11 V, I_L = 500 mA, DRV = 2 V		2.5	3.6	mA
Thermal Shutdown Threshold	T_{SD}			160		°C
OSCILLATOR						
Oscillator Frequency	f_{SW}		0.75	1	1.25	MHz
Minimum Sleep Duty Cycle	D_{PSM}	I_L = 500 mA		14		%
Maximum Duty Cycle	D_{MAX}		100			%
Wake up Hysteresis	V_{HYST}	FB voltage drops below V_{REF}	20	30	40	mV
OUTPUT SWITCH						
Switch On Voltage	V_{IO}[3]	I_L = 500 mA, FB and DRV = GND		0.25	0.4	V
Current Limit Threshold	I_{LIM}		1.0	1.2	1.4	A
Leakage Current		V_{IN} = 12 V		0.5		µA
ERROR AMPLIFIER						
Reference Voltage Accuracy	V_{REF}	FB = COMP	1.222	1.245	1.265	V
Reference Voltage Line Regulation		FB = COMP, V_{IN}= 3 V to 12 V		.02		%/V
Feedback Input Bias Current	I_{FB}	soft start expired	-50	1	50	nA
Sink/Source Current	I_{COMP}		35	60	85	µA
Short Circuit Current	$I_{COMP, SD}$	V_{COMP} = 0 V, activating shutdown		20	40	µA
Transconductance	$g_{m, EA}$	FB = COMP		480		µA/V
MODULATOR						
Transconductance	$g_{m, MOD}$	V_{COMP} to I_L		1		A/V
Control Offset Voltage	$V_{PWM, OS}$			0.90		V
Soft Start Time	t_{SS}			250	600	µs
Shutdown Threshold Voltage	$V_{COMP, SD}$		340		750	mV
Slope Compensation	m_{SC}	Effectively summed to I_{SW}		0.7		A/µs

NOTES

1 All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC).

2 For higher efficiency operation, tie the DRV pin to the output for I_L < 250 mA, and VIN > 3 V.

3 V(IN) - V(SW), includes voltage drop across internal current sensor.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Input Supply Voltage ..... –0.3 V to +12 V
Voltage on any pin with respect to GND .. –0.3 V to +12 V
(voltage on any pin may not exceed V_{IN})
Operating Ambient Temperature Range .. –40°C to +85°C
Operating Junction Temperature ..... +125°C
θ_{JA} (4-layer board) ..... +116°C/W
θ_{JA} (2-layer board) ..... +159°C/W
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature Range (Soldering, 10 sec.) ..... +300°C
Vapor Phase (60 sec) ..... +215°C
Infrared (15 sec) ..... +220°C

*This is a stress rating only; operation beyond these limits can cause the device to be permanently damaged. Unless otherwise specified, all voltages are referenced to GND.

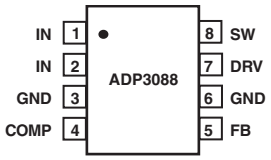
PIN FUNCTION DESCRIPTIONS

Pin	Mnemonic	Function
1, 2	IN	Power Supply Input. Both pins must be connected.
3,6	GND	Ground. Both pins must be connected.
4	COMP	Feedback Loop Compensation and Shutdown Input. An open drain or collector used to pull the pin to ground will shutdown the device.
5	FB	Feedback Voltage Sense Input. This pin senses the voltage via an external resistor divider.
7	DRV	This pin provides a separate path for drive current to be connected to ground.
8	SW	Switching Output.

ORDERING GUIDE

Model	Temperature Range	Package Option	Branding Information
ADP3088ARM	-40°C to +85°C	MSOP-8	P0A

PIN CONFIGURATION



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the device features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

THEORY OF OPERATION

The ADP3088 is a fixed frequency buck switching regulator in an MSOP-8 package using an external Schottky rectifier. It features an integrated 1A power switch and switches at 1MHz. ADP3088 utilizes PWM operation and incorporates soft-start for controlled start-up sequence and over temperature switch protection. The ADP3088 draws low current while running in power saving mode, and even lower current in shutdown.

Refer to the functional block diagram on page 1. The system shown is configured for a 1.8 V output using a 10 μH inductor. At the beginning of a cycle the 1 MHz oscillator enables an SR latch, enabling the internal 1 A power switch. The current sense amplifier and the protection logic block monitor the current flowing between the IN and SW pins. The switch is turned off when the current reaches a level determined by the protection logic block or PWM comparator, whichever is lower. The error amplifier measures the output voltage through an external resistor divider tied to the FB pin. This amplifier servos the switch current to regulate the FB pin voltage to 1.245 V. An internal regulator provides power to the control circuitry. The COMP pin can be used to shutdown the ADP3088. When pulled low it turns off the internal regulator, thus biasing down the chip, reducing the input current and disconnecting the output from the input. Anti-saturation circuitry is used to drive the switch to the edge of saturation. This allows the driver to quickly switch at 1 MHz and maintain good efficiency. And for improved efficiency, the DRV pin may be connected to the output provided that the input voltage is at least 1 V greater than the output.

If the output load increases, the error amplifier will detect a lower voltage on the FB pin, via the resistor divider on the output, and send a signal to the PWM comparator to increase the on time of the switch. This in effect increases the duty cycle and provides more current to drive the increased load during the transient event, until a new operating point is established.

Reference

The ADP3088 incorporates an internal bandgap reference, it includes curvature correction for extremely low temperature coefficient. The reference can be disabled by grounding the COMP pin which also turns off the bias for the rest of the chip.

Error Amplifier

The error amplifier provides a control voltage to the PWM stage to set the peak inductor current which sets the output current of the regulator. It is a g_m amplifier in that its output is a current to the COMP pin.

Protection Logic

The protection logic block provides current limit and over-temperature protection. The over temperature protection is enabled when the temperature of the chip exceeds a specified preset temperature; the switch will be disabled until the temperature drops below a specified level, then normal operation will resume. The thermal shutdown only stops switching, but does not put the chip to power saving mode, nor does it re-initiate soft start. As the chip cools slightly, it will cycle in and out of thermal shutdown rapidly, maintaining the die temp at 150°C, but allowing the output voltage and current to swing up and down. The current limit protection overrides the PWM comparator; if this occurs then the switch pulse will be terminated and the soft start mode will be reset.

Current Sense Amplifier

The voltage on the internal current sense resistor is sensed and passed to the ramp input of the PWM comparator. This current sense signal is also passed to the current limit comparator for peak current limit shutdown . At current limit the soft-start capacitor is reset and soft-start is re-initiated. The current limit is normally 1.2 peak switch current. Slope compensation is added to ADP3088 to stabilize the loop. A generated ramped signal is summed with the current sense signal to provide slope compensation. Slope compensation is needed to close the inner loop so subharmonic oscillation is avoided. The ramp is reset with each clock cycle so that the ADP3088 is capable of true 100% duty cycle.

Run/Stop Comparators

This block creates the 1 MHz signal sent to the SR latch which is used for the switching frequency. It also takes the FB voltage and decides when to go into and wake up from power saving mode. The decision to induce power saving mode is based upon duty ratio. During steady-state continuous operation, the duty ratio of a PWM buck regulator is simply a function of input/output voltage ratio, with second order effects including the voltage drop of the internal switch and the external diode. Once the load drops to a certain point, discontinuous operation occurs, and the duty ratio begins to modulate to maintain regulation. In the ADP3088, the regulator goes to sleep when the integrated duty ratio measurements drops to less than half of the minimum expected integrated duty ratio. The minimum expected duty ratio occurs at max input voltage, min output voltage in continuous mode operation.

PWM Comparator

The PWM comparator looks at the signal from the current sense amplifier and the error amplifier to determine the correct switch on time to regulate the output voltage under a given load.

Soft-Start Timer

Soft start will prevent saturating the inductor which could cause uncontrolled overshoot of the output voltage and electrical stress to the system at start up. When first powered up, an internal soft start capacitor is discharged and the soft start circuitry provides a gradually decaying offset to the error amplifier to prevent it from saturating and from commanding maximum switch current to charge the output capacitor. The output voltage approaches the final regulation voltage with a smooth exponential decay. This will reduce electrical stress to the system.

Output

The output stage contains the bipolar power switch, and the circuits necessary to switch it on and off quickly. The pass switch is driven to the edge of saturation and the result is a fast switching response and low switch resistance. For improved efficiency, the DRV pin may be connected to the output provided that the input voltage is at least 1 V higher than the output. This will send the current needed to drive the bipolar switch to the output load instead of routing it to

ground. For some V_{IN} and I_{LOAD} configurations, the DRV pin must be grounded for reliable operation.

APPLICATION INFORMATION

Output Voltage Setting

In its standard usage, the output voltage of the ADP3088 is programmed to a desired fixed value by a resistor divider from the output voltage into the feedback node, the pin FB, at which node the control loop ensures regulation at the reference level, V_{REF}. The divider should be designed to satisfy the formula:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_B}{R_A}\right) \quad (1)$$

where R_A is the upper divider resistor (between the output and FB) and R_B is the lower one (between FB and ground). R_A and R_B are recommended to have values in the range of 2~200 kΩ and are likely to require a 1% tolerance or better to attain acceptable output voltage tolerance.

In less conventional applications described separately, the resistor feedback configuration can be modified or tapped with other resistors to affect current flow into the FB node that, in turn, influences the output voltage. Even a switched voltage can be summed into the FB node as long as it is sufficiently integrated and does not intolerably compromise the transient response. This latter application is considered further below in an application for powering a DSP.

Input Voltage, Power Dissipation Considerations, and Power Savings Mode

The input voltage range is not typically considered a critical parameter for electrical functionality, but there are several considerations, upon which there is further elaboration below:

1. V_{IN} must never exceed the maximum rated voltage
2. V_{IN} must be within the specified operating range when normal operation is expected
3. V_{IN} must be greater than V_{OUT} by at least the specified headroom when DC regulation is expected
4. V_{IN}, if not sufficiently greater than V_{OUT}, may limit the large signal transient response of a buck converter
5. V_{IN}, if much greater than V_{OUT}, may give rise to such a low duty ratio that it activates power savings mode even at static higher load conditions or upon dynamic load changes when it is not desired.
6. V_{IN} affects the device power dissipation (a lower value causes higher dissipation), which in turn affects die temperature that must be kept below a maximum rating.

The lowest input voltage together with the maximum output voltage and maximum current create the conditions for maximum power dissipation in the device, which determine maximum temperature rise that should be checked against the maximum junction temperature rating. The formula for maximum power dissipation in the device is given by:

$$P_{D,MAX} = \frac{V_O + V_{F@IO,MAX}}{V_{IN}} \times I_{O,MAX} \times V_{SW@IO,MAX} \quad (2)$$

where V_F is the diode forward voltage drop and V_{SW} is the drop across the internal switch and current sensing resistor that appears between the VIN and SW pins of the ADP3088 during the on state of the switch. Both of these variables can be approximated from a combination of worst-case specs and typical graphs. Multiply the power dissipation by the thermal resistance from junction to case or ambient, as desired, to determine internal temperature rise.

If the input voltage were so much higher than the output voltage that it required an average duty ratio less than an internally preset threshold, then power savings mode ("PSM") – that is characterized by periodic shutdown and wakeup of the device that reduces average quiescent current – would be active for all load conditions rather than only at lighter loads, for which it is intended. PSM operation is characterized by low-frequency ripple on the output that appears similar to the behavior of a hysteretic regulator. This is usually not a factor for consideration and may be ignored if PSM operation is acceptable for all load conditions, but in case it is relevant, the following recommendation is offered:

$$V_{IN} < \frac{V_O + V_F}{D_{PSM(MAX)}} \quad (3)$$

It is not possible to prevent the duty ratio from tending towards zero in non-synchronous buck converters below a certain minimum load current level called "borderline current" or "critical current" for the power converter. That corresponds to the inductor ripple current reaching zero at its bottom peak - sometimes called the "valley current". If PSM activation strains the lower regulation limit due to the hysteretic ripple, the output voltage can be offset slightly upward by readjusting the nominal voltage setpoint with the resistor divider.

Even though a buck converter may have a low dropout voltage that allows the static regulation to be maintained as the input voltage drops near to the output voltage, in buck converters the slew rate limitation of inductor current can compromise the dynamic regulation in response to load current step increases. That is because the maximum rate that current can be increased in the inductor is proportional to the voltage available to impress across it, which is compromised as the input voltage reduces toward the output voltage. This is not a limitation of the device but of buck converters in general. The limitation is considered as part of the output filter design, although it could also be considered in terms of a minimum acceptable input voltage for a given output filter that will ensure that the dynamic response is acceptably maintained.

Output Filter Components

In most applications it is desirable to use the smallest inductor value that does not introduce practical problems, as this tends to yield the lowest cost inductor. One reason for using an even larger inductor than the minimum tolerable might be to reduce output ripple voltage further, but cost being

equal, this is generally better accomplished with a better quality or proportionally larger output capacitor instead, since a larger inductor degrades the large-signal transient performance capability.

A conservative nominal design target value for the inductor of a typical application circuit is that which creates a peak-to-peak ripple current, ΔI_L, for the nominal input voltage that is approximately a third of the nominal 500mA rating of the ADP3088. The reason for not suggesting to base the ripple current on the maximum load current is for concern of overload protection. Scaling of the ripple currents with lower load currents would yield higher inductor values that might give satisfactory operation, but in order for overload operation up to the current limit level of the ADP3088 to be satisfactory, it would be necessary to choose an inductor rated up to that higher current, which would likely yield an unsatisfactory inductor size and cost. In any case, having chosen a target level for ΔI_L, the recommended inductor value is given by:

$$L = \frac{(1-D)\times(V_O + V_F)}{f_{SW}\times\Delta I_L} \quad (4)$$

where D is the duty ratio - the suffix indicating continuous inductor current - and is given by:

$$D = \frac{V_O + V_F}{V_{IN} + V_F - V_{SW}} \quad (5)$$

and V_{SW} and V_F are assessed at full load, and f_{SW} is the fixed switching frequency of the ADP3088. The formula suggests the calculation of L using a nominal input voltage, and for applications requiring a large ranges of V_{IN} the limitations of transient response at $V_{IN(MIN)}$ versus the higher ripple at $V_{IN(MAX)}$ may warrant deeper consideration of how to optimize the design. In applications where load transients are not severe, this conservative design for L is recommended. A more aggressive minimization of L is outlined below, but a few restrictions are noted.

As inductance becomes smaller the ripple current becomes larger. If the ripple becomes particularly large or, as an additional factor, if the load is particularly dynamic, then there is an increasing possibility that the peak inductor current will undesirably reach the current limit shutdown threshold, I_{CL}. This should be avoided by restricting the minimum inductor value to keep the ripple current moderated. An alternate way to prevent excessive dynamic overshoot of inductor current during a load transient is to reduce the DC gain of the error amplifier by adding resistive feedback; this idea is discussed below.

Another important restriction of the minimum inductor value may apply. The design should ensure against possible subharmonic oscillation that can occur in all fixed-frequency current-controlled switching power supplies when switching at high duty ratios. The subharmonic oscillation phenomenon will not be explained here - there are plenty of papers written on the subject - except to say that it is characterized by alternating high and low duty ratios - i.e., every other cycle - that produces additional ripple on the output. To prevent subharmonic oscillation the following restriction for the minimum inductor value is recommended:

$$L > \frac{2\mu H}{V}\times(V_O + V_F)\times\frac{V_O + V_F}{V_{IN(MIN)} - 0.35} \quad (6)$$

The value used for $V_{IN(MIN)}$ should be only the minimum input voltage for which normal high performance operation must be assured. Note the value returned for L may be negative in which case the restriction does not apply. If the preceding formula yields a lower inductor value than the conservative recommendation given previously, as is likely for most applications, then it is time to consider further limitations to see how low the value can be minimized.

For a given inductor selection, the earlier formula is rearranged for convenience and skewed to the worst case input voltage to determine the maximum inductor ripple current, ΔI_L:

$$\Delta I_{L(MAX)} = \frac{V_{IN(MAX)} - V_O - V_{SW}}{V_{IN(MAX)} + V_F - V_{SW}}\times\frac{V_O + V_F}{f_{SW}\times L} \quad (7)$$

Performance degradation of the inductor - consisting of some loss of inductance or excessive power loss - may be encountered at higher ripple currents, so the ripple current figure, together with knowledge of the expected DC current should be checked against specifications of the inductor.

If the ESR of the output capacitor is substantial - as it is likely to be if a MLC capacitor is not used - then the ripple voltage on the output, dominated by the ESR, may be substantial and of concern for regulation specifications. The resistive component of the output voltage ripple is simply the ripple current times the ESR, and if it is more than a few millivolts it will dominate the output capacitance in contributing to output ripple voltage.

The boundary condition of the inductor reaching the borderline current, $I_{O(BL)}$ can be determined by the formula:

$$I_{O(BL)} = \frac{V_O + V_F}{2f_{SW}L}\times\frac{V_{IN} - V_O - V_{SW}}{V_{IN} + V_F - V_{SW}} \quad (8)$$

Below this output current level, the inductor current will be discontinuous and the duty ratio will be modulated to lower values, by factors substantially more than thus the losses that cause only a small amount of modulation in continuous inductor current operation. PSM is initiated automatically by a proprietary technique comprising a duty ratio amplifier with an internal time constant. As load current drops well into the low current region and the duty ratio passes below the threshold of D_{PSM} for a sufficient time, PSM is activated. The corresponding level of output current is given by:

$$I_{O(PSM)} = \frac{1}{2}\times D_{PSM}{}^2\,\frac{V_{IN} + V_F - V_{SW}}{V_O + V_F}\times\frac{V_{IN} - V_0 - V_{SW}}{f_{SW}\times L} \quad (9)$$

It can be seen in the formula that this current threshold is inversely proportional to inductance, so although it is usually not a relevant concern, it is noted that an aggressively

low output inductance should be avoided to keep the PSM threshold current at a desirably low level.

For the user's reference, when current is below the borderline level, the duty ratio is modulated according to the formula:

$$D_D = \sqrt{2 \times I_O \times \frac{V_O + V_F}{V_{IN} + V_F - V_{SW}} \times \frac{f_{SW} \times L}{V_{IN} - V_O - V_{SW}}} \quad (10)$$

where the suffix indicates that the inductor current is discontinuous.

For controlling the capacitive component of the output ripple voltage, the following constraint on the minimum output capacitance should be applied:

$$C_O > \frac{\Delta I_L}{8 f_{SW} \Delta V_R} \quad (11)$$

where ΔV_R is the tolerable ripple voltage. However, this constraint is rarely relevant, as the typical capacitance requirement is driven more by dynamic response requirements than by ripple concerns. In a typical application circuit, a 10 µF capacitor produces a capacitive output voltage ripple component of only about 2 mV. 10 µF is usually sufficient for applications that do not impose particularly HF load transients, which imposes additional constraints that are elaborated upon in the next section.

Load Characterization

Optimization of the compensation, as well as the output filter, requires some knowledge of a fundamental characteristic of the load. Qualitatively, there are two types of loads with which we are concerned: fast-slew-rate and slow-slew-rate. These slew rates are assessed with respect to the minimum [absolute] inductor [current] slew rate as given by:

$$\left| \left(\frac{dI_L}{dt} \right), MIN \right| = < \left\{ \frac{V_{IN(MIN)} - V_{SW} - V_O}{L_{MAX}} \; and \; \frac{V_O + V_F}{L_{MAX}} \right\} \quad (12)$$

where the "<" sign indicates a selection of whichever of the bracketed terms is the lesser.

If the slew rate of the load is fast compared to the minimum inductor slew rate, then the ability of the power converter to contain the output voltage deviation following a load change is limited not only by the response of the control loop - i.e., by its speed to demand zero or maximum duty ratio from the modulator - but by the power stage as well. In such a case, beginning with the recognition that output voltage deviation would be substantial even if the loop response were instantaneous, it can be shown that one can achieve better overall voltage containment by degenerating the DC loop gain. As a technical matter, it should be noted that there will always be some minimum output voltage deviation downward due to a load step even if the inductor slew is as fast as the load slew rate, because, during a switching cycle, the modulator latches its "decision" to turn off the switch and it cannot rescind that decision but must wait for the next clock cycle to turn on the switch again and begin slewing the inductor current upward. This is only a second order consideration.

Slow slew rate loads may be referred to simply as conventional loads, since these have been the more prevalent type of load. Optimally compensating a conventional load is synonymous with small signal AC considerations: the objective is to maximize the AC gain up to the crossover frequency, ensure sufficient phase margin at the unity gain crossover frequency, and keep the gain rolling off at higher frequencies to avoid gain margin problems.

Fast slew rate loads may be referred to as digital loads since, from the perspective of the power converter, they have a digital characteristic when changing between two extremes, and also because such fast slew rates tends to characterize modern digital circuits, which often feature power management interrupts - i.e., interrupt signals used to turn on and off circuitry on an as-needed basis during normal system operation. Optimally compensating a digital load is more a task of impedance matching and DC gain determination than a task of AC loop optimization.

Returning to constraints for choosing the output capacitor, for digital loads another criteria for ensuring sufficient output capacitance applies:

$$C_O > \frac{\Delta I_O{}^2}{2 \Delta V_O \left| \frac{dI_L}{dt} MIN \right|} \quad (13)$$

where ΔI_O is the maximum HF load step. It should be noted that the formula results strictly from the physical limitation of the output filter; the compensation must also be optimized to maximize the response of the control loop to avoid substantial additional output voltage deviation. The formula might be also written in to describe a maximum inductance for a given capacitance, but it is generally better practice to choose the inductor first and add capacitance as needed.

The he impedance of the output capacitor together with a digital load creates some limiting considerations, also. Series resistance (ESR) rather than capacitance can be a dominant design consideration with non-MLC capacitors. If the load is essentially digital, then the dynamic deviation of the output voltage cannot be limited to any better than the dynamic load current step times the ESR. In a formula:

$$\Delta V_O \geq \Delta I_O \times ESR \quad (14)$$

In such a case, it is often important to choose a capacitor that controls the ESR to a sufficiently small value, and MLC capacitors are often chosen to practically eliminate the consideration of ESR entirely.

Closing the Loop - Compensation

The factors determining the response of the power converter are noted: the feedback input resistor divider, a lead network if applicable, the transconductance of the error

amplifier, its frequency response limitation (i.e., as adequately modeled by a capacitance from output to ground) its external termination impedance (i.e., the compensation, that may or may not include DC feedback), the modulator transconductance, and the power converter's termination impedance (i.e., the output capacitor and load resistance).

Since the ADP3088 has a current controlled loop, the particular inductor value does not by first order consideration affect small signal stability. However, slew rate limitations as discussed earlier - a large signal limitation consideration - set boundaries that are often relevant for optimizing compensation of the feedback loop. If the compensation of the current control signal, i.e., the COMP pin, is designed to promote a current response that is faster than the inductor current can slew, then when a step load is applied the control signal will tend to initially respond in excess (of the actual current change that is occurring) and then allow an overshoot of the current and output voltage as it is delayed in correcting its excess.

For conventional loads, the following describes how the frequency corners (poles and zeroes) are positioned or should be chosen to optimize the loop gain, beginning in the low frequency spectrum:

1. The DC loop gain is limited by the applied load resistance and the output resistance of the error amplifier, but it is not important to determine how high the DC gain is.
2. Two poles in the LF spectrum begin to roll off the gain, one determined by the load resistance and output capacitor, C_O, and the other by the error amplifier's output resistance and its termination capacitance - the equivalent feedback capacitance and the added compensation capacitance C_{HF}; determining the location of these poles is not relevant to compensation design - it suffices to know that both are decades below the crossover frequency.
3. A lead network is especially desirable for a variable output voltage application in order to keep a fairly constant crossover frequency and phase margin for all output voltages; if used, this lead network consists of simply a capacitor, C_{FF}, in parallel with the upper feedback divider resistor, R_A; this creates a closely spaced zero/pole pair that provides a gain boost before crossover so that, above the pole frequency, the loop gain and phase are similar for all output voltages; if the lead network is used for a fixed voltage application, the pole should be chosen to align with the following described zero; for variable voltage applications, the maximum frequency of the pole should be placed as high as is comfortable without substantially degrading phase margin (e.g., not within an octave or, more conservatively, a half decade of the crossover frequency).
4. A zero turns the gain rolloff back to 1-pole sufficiently in advance of the crossover frequency to create ample phase margin, e.g., half a decade; the zero could feasibly be that of the output capacitor itself - i.e., the zero formed by the ESR and the capacitance C_O - but that is both unlikely (since the zero frequency will likely be higher than where the loop zero is desired) and generally imprudent (since the loop performance would depend on the stability of the ESR, which often is poor or unknown); as recommended, the zero, f_Z, is created by an R_C circuit terminating the COMP pin (a resistor, R_C, in series with a capacitor, C_C), while the capacitance terminating the error amplifier, C_{HF}, forms a pole, f_P, with R_C to cancel the zero of the output capacitor, or, if the zero is well above the crossover frequency, as may be the case when using an MLC output capacitor, that pole is set high enough above the crossover frequency, again e.g., half a decade, so that it doesn't cut substantially into the phase margin at crossover, but still ensures continued gain rolloff so that the gain margin is acceptably high; note that the previous guidelines suggest that $C_C \geq 10 \times C_{HF}$.
5. The gain crosses 0 dB (unity) at a crossover frequency that is typically a tenth and advisably not greater than a fourth of the switching frequency - one primary reason for this approximate upper limit being the extra phase margin loss due to the switching interval that is not predicted by the linear model.

Assuming no lead network is used, the open loop gain is given by:

$$A_{OL} \approx \frac{600\mu\left(\frac{V}{\Omega^2}\right) \times Z_{COMP} \times Z_O}{V_{OUT}} \qquad (15)$$

where V_{OUT} is the nominal DC level. This equation together with the preceding recommendations should suffice to determine compensation component selection for users familiar with loop design. This begins with deciding the crossover frequency, f_C, evaluating the impedances at that frequency, and setting the open loop gain, A_{OL}, to unity. By example, f_C = 125 kHz is chosen.

Assuming a well chosen C_{HF} as described previously - i.e., such that it creates a pole well above crossover or approximately matches the zero of the output capacitor, the following equation approximates the calculation of the crossover frequency:

$$f_C = 1 + \sqrt{\frac{1 + \left[50k(\Omega/A) \times f_Z \times k_1\right]}{21k(\Omega/A) \times k_1}} \qquad (16)$$

where $k_1 = C_O \times V_{OUT}/R_C$ and $f_Z = 1/2\pi R_C C_C$ - the zero frequency set by the compensation - and the units are shown with the constants in the equation for clarification.

The preceding equation cannot readily be solved in terms of k_1, but it can be solved closely enough by a few iterations beginning with values for k_1 around 1×10^9 (FA). For the example below, set the zero about a half decade below f_C as previously advised, that is, choose $f_Z \sim f_C/\sqrt{10}$ = 40 kHz. Using the previously stated values for f_Z and f_C, the value of k_1 = 800 p(FA) satisfies the equation. R_A and R_B are presumed to be already chosen per earlier guidelines to set the output voltage. As an example, $R_A = R_B$ = 10 kΩ (implying an output voltage of 2.5 V). Similarly it is presumed that C_O was chosen; let C_O = 15 µF. Then, finally, R_C and then also C_C can be determined by rearrangement of simple formulas previously given. The example yields $R_C \sim$ 47 kΩ and $C_C \sim$ 82 pF. Assuming an MLC output capaci-

tor of reasonable quality, the pole setting capacitor could be chosen to be C_{HF} = 4.7 pF.

A general purpose application circuit is shown in Figure 2.

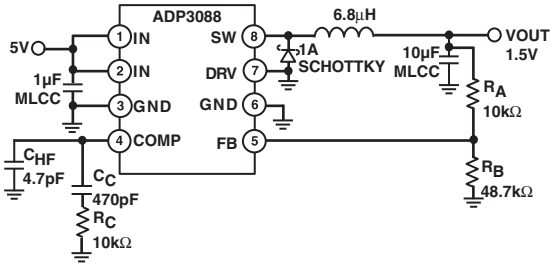


Figure 2. +5 V to 1.5 V, General Purpose Application

Another application circuit features a voltage inversion and regulation design such that the output voltage is negative, see Figure 3. Negative output voltages are allowed in the case that the input plus the output voltage does not exceed the rating of the device. In the voltage inverting configuration, the ground reference of the ADP3088 is the negative output voltage and the conventional output voltage point is tied to ground. Operation is bootstrapped: the power converter behaves as if the input voltage were equal to the actual input voltage plus the magnitude of the output voltage and as if the output voltage were not inverted. This implies that it is possible to have the input voltage be less than the magnitude of the output voltage - provided that the input voltage alone is sufficient to start the operation of the IC - i.e., before the negative output voltage has been developed. (The circuit below with a -3.3V output works fine over an input range from 2.5 V to 7.5 V.) Since the ADP3088 features a current controlled loop, the feedback effect of essentially boosting the input voltage atop the output (with respect to the ground connection of the ADP3088) is reduced to a negligible second-order effect.

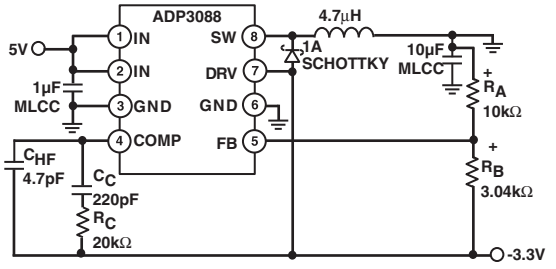


Figure 3. +5V to -3.3V, General Purpose Inverting Application

Voltage Positioning Designs

For digital loads a different compensation technique is recommended that involves implementing "voltage positioning", that is now commonly used on CPUs but is equally applicable to any dynamic device. Voltage positioning is the intentional and controlled variation of output voltage with load current, such that the power supply appears to have a substantial output resistance. The key to voltage positioning optimization for a digital load is to degenerate the loop gain just enough so that the static load regulation allows a similar voltage deviation with current as would be the peak voltage deviation, ΔV_O, that could not be avoided in the event that a step change of current were to occur even if the loop response were instantaneous. The reason for even an instantaneous response in the control loop allowing an output voltage deviation is that the slew-rate of current in the output is limited by to the inductor, and a corresponding dynamic burden is placed on the output capacitor to maintain the output voltage. Therefore, inductor value minimization is desired both for concern of its size and cost, and also to maximize the slew rate of current to the output so that a smaller output capacitor is needed.

To implement voltage positioning, a resistor, R_{FB}, should be placed between the COMP and FB pins according to the formula:

$$R_{FB} = \frac{\Delta I_O R_A}{g_{MOD} \times \Delta V_O} \qquad (17)$$

where g_{MOD} is the modulator gain and ΔI_O must be assessed over the entire operating load range as the difference between maximum and minimum load. C_O must be chosen at least large enough to support the targeted ΔV_O according to the earlier stated formula governing the relationship between minimum output capacitance, voltage deviation, and load current. In order to ensure that the output voltage will be constrained within the limitations of ΔV_O, the limitations noted earlier for PSM hysteretic ripple if applicable in the operating load range and ESR. Also an experimental adjustment downward to the value of R_B may be needed, as the DC bias point of the COMP node is usually a little higher than V_{REF}, which would result in a slight downward shift of the nominal output voltage.

Having chosen this design approach, the series RC of the compensation network can be removed and the single remaining capacitor, C_{HF}, should be increased to approximately:

$$C_{HF} = \frac{C_O \times ESR}{R_{FB}} \qquad (18)$$

If an MLC capacitor is used for C_O, the value of C_{HF} might be calculated to be less than a few picofarads, in which case it is recommended to use a 4.7~10 pF capacitor. The formula is derived from a patented design technique called ADOPT™ - Analog Devices' Optimal Positioning Technology. This creates AC and DC impedance matching, and the increased complexity of the DC regulation design is moderated by the simplicity of the frequency compensation.

In this design approach, at higher currents the output voltage will be appreciably lower than at low currents. This is equivalent to saying that the load regulation appears to be poor. But, paradoxically perhaps to the user unfamiliar with voltage positioning, the overall containment of voltage within a given window will be improved, and that tends to be of particularly importance in many highly dynamic loads.

The application circuit in Figure 4 features a 3.3 V input and a 2.5 V output at 100~400 mA which constrains the

output voltage within a ~100 mV range with only a 4.7 µF output capacitor, even when the load slew rate is extremely fast. This does not include the initial tolerance of the voltage setting that is separately accounted with voltage positioning designs. Note that the lower resistor, R_B, of the feedback divider is reduced from the 10 kΩ value that one would use for a standard (non-voltage-positioned) design that had no voltage positioning resistor R_{VP}.

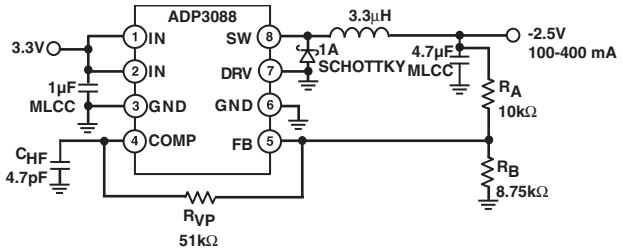


Figure 4. Application Circuit using Voltage Positioning, Allowing Small Output Capacitance

Extra-Low-Voltage Outputs

Some newer power management applications require voltage levels below the normal adjustable voltage range of the ADP3088, i.e., below 1.25 V. Such applications can be accommodated using the ADP3088 by modifying the application circuit to sum in a resistor-weighted portion of another regulated system voltage, e.g., 3.3 V, to the feedback node (FB). The tolerance of the ADP3088's output voltage will increase by an amount proportional to the tolerance of the summed in system voltage times the ratio of the conductance from that node to that of the output voltage. The below example in Figure 5 shows an implementation of this technique together with another special implementation described below. The resistor R_{TT} sums from a 2.5 V system voltage to the FB node that will reduce the output voltage according to the formula:

$$\Delta V_{OUT} = -V_{TT} \times \frac{R_A}{R_{TT}} \qquad (19)$$

Dynamic Voltage Control

Some newer power management applications also require an ability to adjust the voltage being delivered to a load during operation. Although there is no integration of this feature in the ADP3088, it can readily be accommodated with a few components. Dynamic voltage control can be implemented either by parallel bus control or by PWM. In both cases, the output voltage is modified by summing either switched bits with, presumably binary, weighting resistors or a switched PWM node via a single resistor into the FB pin. (The switched PWM node refers to an external PWM control signal, not the switched node of the power converter itself.) Since the PWM technique modulates a current into the FB node, it is necessary both to integrate that signal and to avoid slowing down the response of the power converter to output voltage transitions. This can be accomplished by placing a capacitor between the output voltage and the feedback node, which serves to provide a zero/pole pair in the main regulation loop, and appears as an integration pole to the PWM signal.

The design of either parallel bit or PWM type of voltage control must consider whether the interface node(s) - from parallel switched bits or a single PWM signal - has an active pullup state (in which case it must be to a known voltage) or a passive pullup (open drain) that floats up to the FB node voltage, 1.25 V, in its high state. If at least the lower extreme of the desired output voltage range must be lower than 1.25 V, either technique can be combined with the technique for lowering the output voltage below 1.25 V. Such an example of an application having this requirement is the BlackFin™ DSP. Figure 5 shows an implementation of this technique.

Input Voltage: 4.75 V ~ 7.5 V

Output Voltage: 0.9 V ~ 1.5 V

Dynamic voltage control interface technique: PWM, active high to V_{IO}

System voltage used for lowering output voltage below 1.25 V: $V_{TT} = V_{IO} = 2.5$ V

Maximum output current: 700 mA

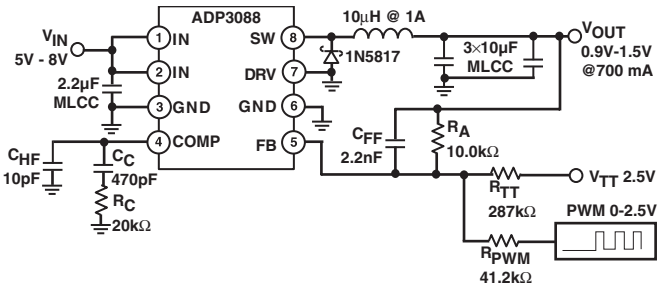


Figure 5. BlackFin DSP Application

RM-8
8-Lead Mini/micro SOIC Package [Mini_SO]