3 A, 1.2 MHz/600 kHz High Efficiency Synchronous Step-Down DC-to-DC Converter

ADP2118

FEATURES

- 3 A continuous output current
- 75 mΩ and 40 mΩ integrated FET
- ±1.5% output accuracy
- Input voltage range from 2.3 V to 5.5 V
- Output voltage from 0.6 V to V_{IN}
- 600 kHz or 1.2 MHz fixed switching frequency
- Synchronizable between 600 kHz and 1.4 MHz
- Selectable synchronize phase shift: 0° or 180°
- Selectable PWM or PFM mode operation
- Current mode architecture
- Precision enable input
- Power good output
- Voltage tracking input
- Integrated soft start
- Internal compensation
- Starts up into a precharged output
- UVLO, OVP, OCP, and thermal shutdown
- Available in 16-lead 4mm × 4mm LFCSP_WQ package

APPLICATIONS

- DSP/FPGA/ASIC core power
- Telecommunication/networking equipment
- PDAs and palmtop computers
- Audio/video consumer electronics

GENERAL DESCRIPTION

The ADP2118 is a low quiescent current, synchronous, step-down, dc-to-dc converter in a compact 4mm × 4mm LFCSP_WQ package. It uses a current mode, constant frequency pulse-width modulation (PWM) control scheme for excellent stability and transient response. Under light loads, the ADP2118 can be configured to operate in pulse frequency modulation (PFM) mode that reduces switching frequency to save power.

The ADP2118 runs from input voltages of 2.3 V to 5.5 V. The output voltage of the ADP2118ACPZ-R7 is adjustable from 0.6 V to input voltage (V_{IN}), and the ADP2118ACPZ-x.x-R7 are available in preset output voltage options of 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, and 1.0 V. The ADP2118 requires minimal external parts and provides a high efficiency solution with its integrated power switch, synchronous rectifier, and internal compensation. The IC draws less than 3 µA from the input source when it is disabled. Other key features include undervoltage lockout (UVLO), integrated soft start to limit inrush current at startup, overvoltage protection (OVP), overcurrent protection (OCP), and thermal shutdown (TSD).

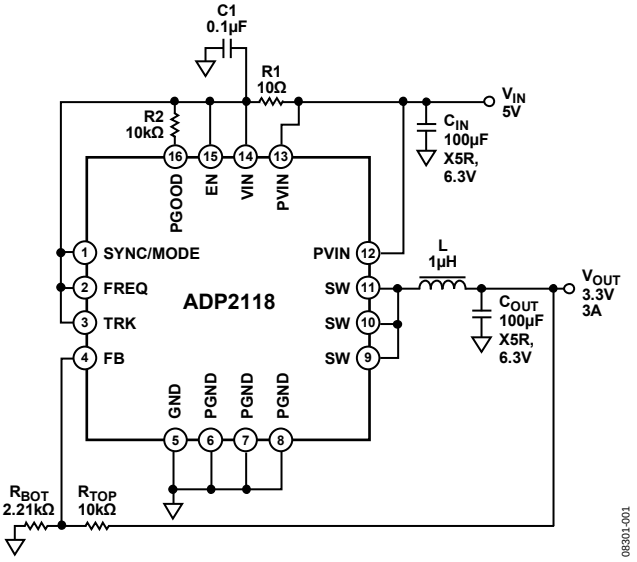

Figure 1. Typical Applications Circuit

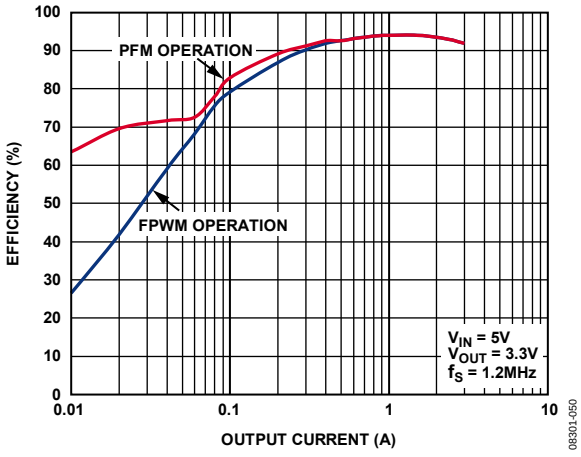

Figure 2. Efficiency vs. Output Current

Rev. 0

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REVISION HISTORY

7/09—Revision 0: Initial Version

SPECIFICATIONS

VIN = PVIN = 3.3 V, EN = VIN, SYNC/MODE = high @ T_J = −40°C to +125°C, unless otherwise noted. Typical values are at T_J = 25°C.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
VIN AND PVIN						
VIN Voltage Range	VIN		2.3		5.5	V
PVIN Voltage Range	PVIN		2.3		5.5	V
Quiescent Current	I_{VIN}	No switching, SYNC/MODE = GND		100	150	µA
		Switching, no load, SYNC/MODE = high		680	900	µA
Shutdown Current	I_{SHDN}	VIN = PVIN = 5.5 V, EN = GND		0.3	3	µA
VIN Undervoltage Lockout Threshold	UVLO	VIN rising		2.2	2.3	V
		VIN falling	2	2.1		V
OUTPUT CHARACTERISTICS						
Load Regulation[1]		I_o = 0 A to 3 A		0.08		%/A
Line Regulation[1]		I_o = 1.5 A		0.05		%/V
FB						
FB Regulation Voltage	V_{FB}	VIN = 2.3 V to 5.5 V	0.591	0.6	0.609	V
FB Bias Current	I_{FB}			0.01	0.1	µA
SW						
High-Side On Resistance[2]		VIN = PVIN = 3.3 V, I_{SW} = 500 mA		75	110	mΩ
Low-Side On Resistance[2]		VIN = PVIN = 3.3 V, I_{SW} = 500 mA		40	60	mΩ
SW Peak Current Limit		High-side switch, VIN = PVIN = 3.3 V	4	5.2	6.4	A
SW Maximum Duty Cycle		VIN = PVIN = 5.5 V, full frequency			100	%
SW Minimum On Time[3]		VIN = PVIN = 5.5 V, full frequency		100		ns
TRK						
TRK Input Voltage Range			0		600	mV
TRK to FB Offset Voltage		TRK = 0 mV to 500 mV	−10		+10	mV
TRK Input Bias Current					100	nA
FREQUENCY						
Oscillator Frequency		FREQ = VIN	1.0	1.2	1.4	MHz
		FREQ = GND	500	600	700	kHz
FREQ Input High Voltage			1.2			V
FREQ Input Low Voltage					0.4	V
SYNC/MODE						
Synchronization Range			0.6		1.4	MHz
SYNC Minimum Pulse Width			100			ns
SYNC Minimum Off Time			100			ns
SYNC Input High Voltage			1.2			V
SYNC Input Low Voltage					0.4	V
INTEGRATED SOFT START						
Soft Start Time		All switching frequency		2048		Clock cycles
PGOOD						
Power Good Range		FB rising threshold	105	110	115	%
		FB rising hysteresis		2.5		%
		FB falling threshold	85	90	94	%
		FB falling hysteresis		2.5		%
Power Good Deglitch Time		From FB to PGOOD		16		Clock cycles
PGOOD Leakage Current		V_{PGOOD} = 5 V		0.1	1	µA
PGOOD Output Low Voltage		I_{PGOOD} = 1 mA		140	200	mV

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
EN						
EN Input Rising Threshold		VIN = 2.3 V to 5.5 V	1.12	1.2	1.28	V
EN Input Hysteresis		VIN = 2.3 V to 5.5 V		100		mV
EN Pull-Down Resistor				1		MΩ
THERMAL						
Thermal Shutdown Threshold				140		°C
Thermal Shutdown Hysteresis				15		°C

[1] Specified by the circuit in Figure 45.
[2] Pin-to-pin measurements.
[3] Guaranteed by design.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VIN, PVIN	−0.3 V to +6 V
SW	−0.3 V to +6 V
FB, SYNC/MODE, EN, TRK, FREQ, PGOOD	−0.3 V to +6 V
PGND to GND	−0.3 V to +0.3 V
Operating Junction Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Soldering Conditions	JEDEC J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	Unit
16-Lead LFCSP_WQ	38.3	°C/W

Boundary Conditions

θ_{JA} is measured using natural convection on a JEDEC 4-layer board, and the exposed pad is soldered to the printed circuit board with thermal vias.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

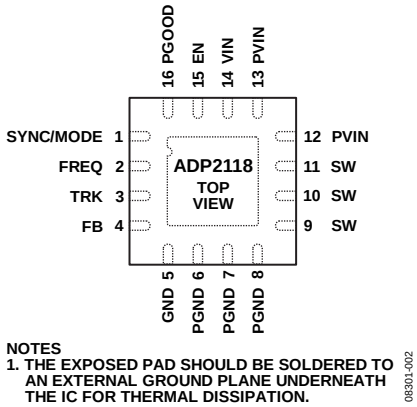


Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	SYNC/MODE	Synchronization Input (SYNC). Connect this pin to an external clock between 600 kHz and 1.4 MHz to synchronize the switching frequency to the external clock (see the Oscillator and Synchronization section for details). CCM/PFM Selection (MODE). When this pin is connected to VIN, PFM mode is disabled and the ADP2118 only works in continuous conduction mode (CCM). When this pin is connected to ground, PFM mode is enabled and becomes active at light loads.
2	FREQ	Frequency Selection. Connect to GND to select 600 kHz and VIN for 1.2 MHz.
3	TRK	Tracking Input. To track a master voltage, drive TRK from a voltage divider from the master voltage. If the tracking function is not used, connect TRK to VIN.
4	FB	Feedback Voltage Sense Input. Connect to a resistor divider from V_{OUT}. For the fixed output version, connect to V_{OUT} directly.
5	GND	Analog Ground. Connect to the ground plane.
6, 7, 8	PGND	Power Ground. Connect to the ground plane and to the output return side of the output capacitor.
9, 10, 11	SW	Switch Node Output. Connect to the output inductor.
12, 13	PVIN	Power Input Pin. Connect this pin to the input power source. Connect a bypass capacitor between this pin and PGND.
14	VIN	Bias Voltage Input Pin. Connect a bypass capacitor between this pin and GND and a small (10 Ω) resistor between this pin and PVIN.
15	EN	Precision Enable Pin. The external resistor divider can be used to set the turn-on threshold. To enable the part automatically, connect the EN pin to VIN. This pin has a 1 MΩ pull-down resistor to GND.
16	PGOOD	Power-Good Output (Open Drain). Connect to a resistor to any pull-up voltage <5.5 V.
17 (EPAD)	Exposed Pad	The exposed pad should be soldered to an external ground plane underneath the IC for thermal dissipation.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{IN} = 5 V, V_{OUT} = 1.2 V, L = 1 µH, C_{IN} = 100 µF, C_{OUT} = 100 µF, unless otherwise noted.

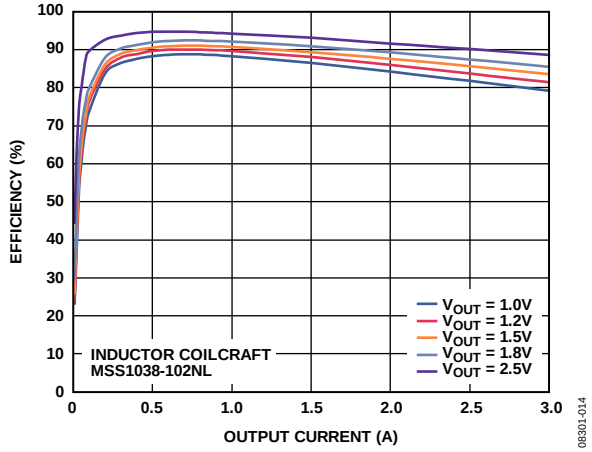


Figure 4. Efficiency (1.2 MHz, V_{IN} = 3.3 V, FPWM) vs. Output Current

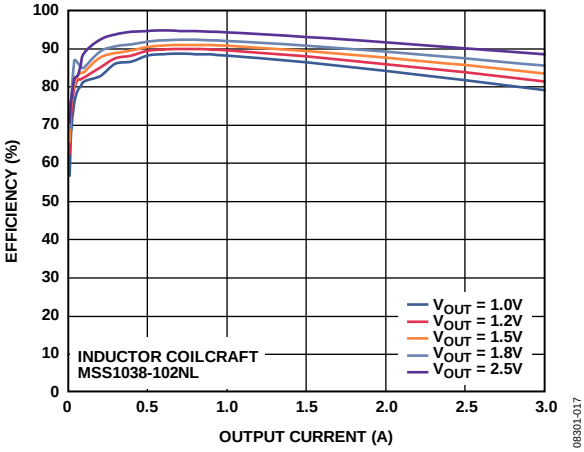


Figure 7. Efficiency (1.2 MHz, V_{IN} = 3.3 V, PFM) vs. Output Current

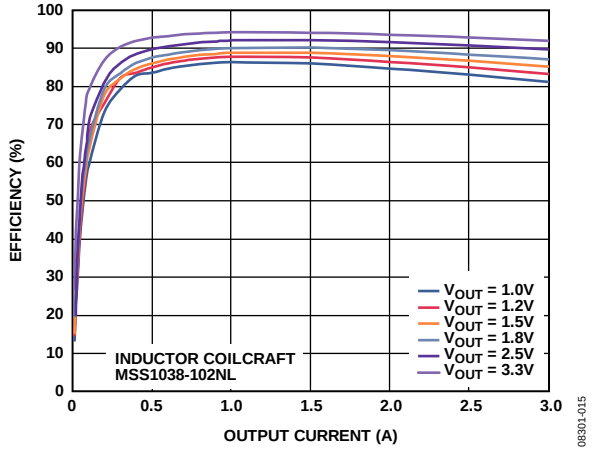


Figure 5. Efficiency (1.2 MHz, V_{IN} = 5 V, FPWM) vs. Output Current

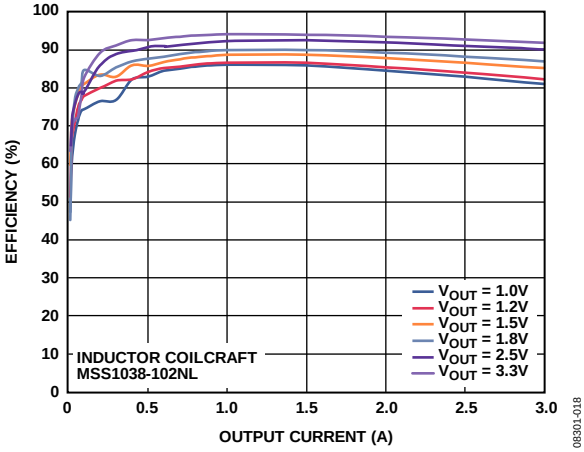


Figure 8. Efficiency (1.2 MHz, V_{IN} = 5 V, PFM) vs. Output Current

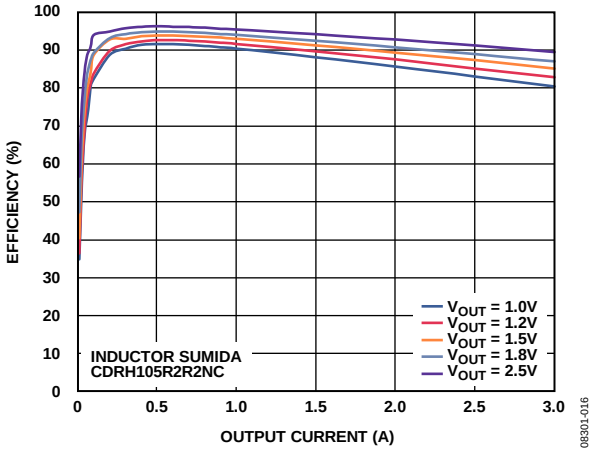


Figure 6. Efficiency (600 kHz, V_{IN} = 3.3 V, FPWM) vs. Output Current

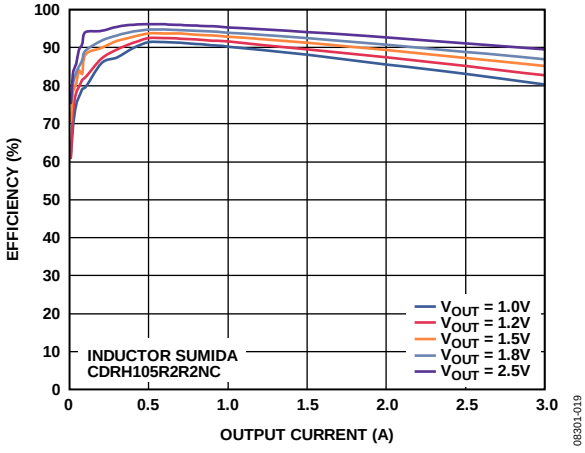


Figure 9. Efficiency (600 kHz, V_{IN} = 3.3 V, PFM) vs. Output Current

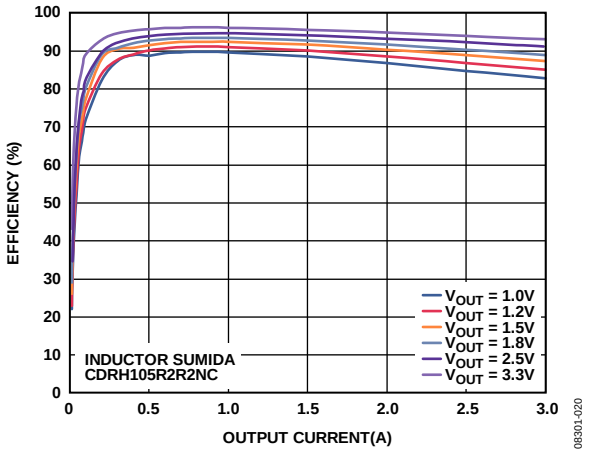


Figure 10. Efficiency (600 kHz, V_{IN} = 5 V, FPWM) vs. Output Current

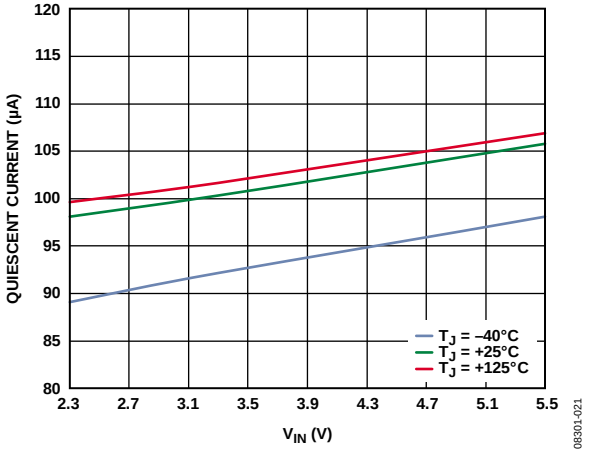


Figure 11. Quiescent Current vs. V_{IN} (No Switching)

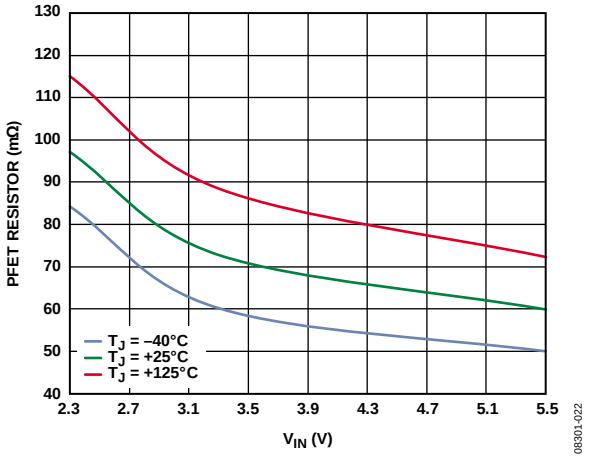


Figure 12. PFET Resistor vs. V_{IN} (Pin-to-Pin Measurements)

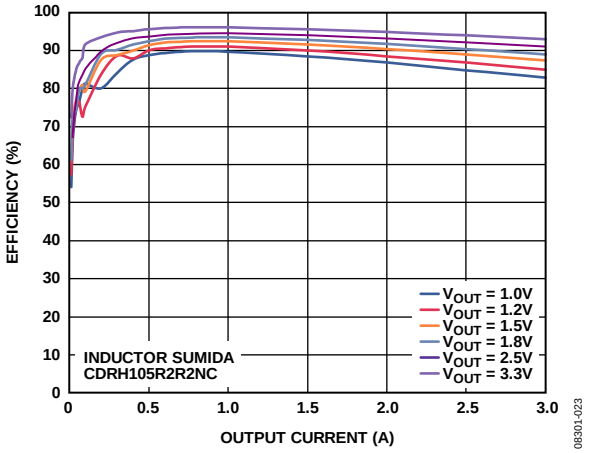


Figure 13. Efficiency (600 kHz, V_{IN} = 5 V, PFM) vs. Output Current

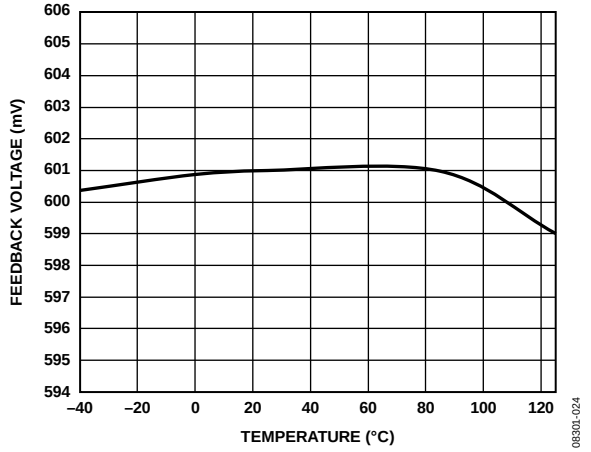


Figure 14. Feedback Voltage vs. Temperature (V_{IN} = 3.3 V)

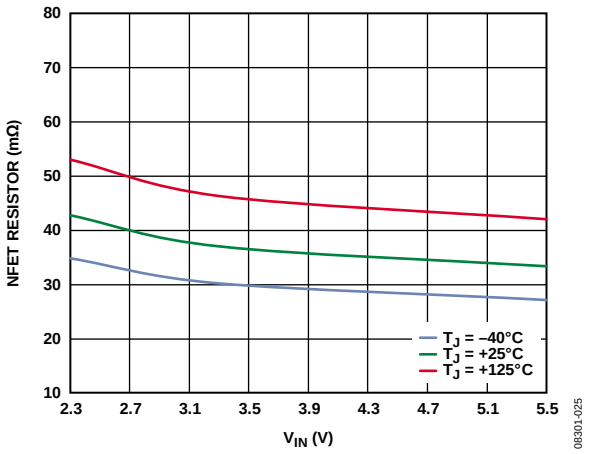


Figure 15. NFET Resistor vs. V_{IN} (Pin-to-Pin Measurements)

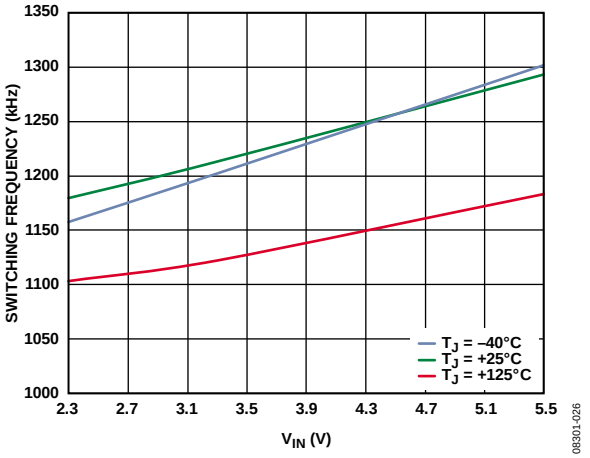


Figure 16. Switching Frequency vs. V_{IN} at 1.2 MHz

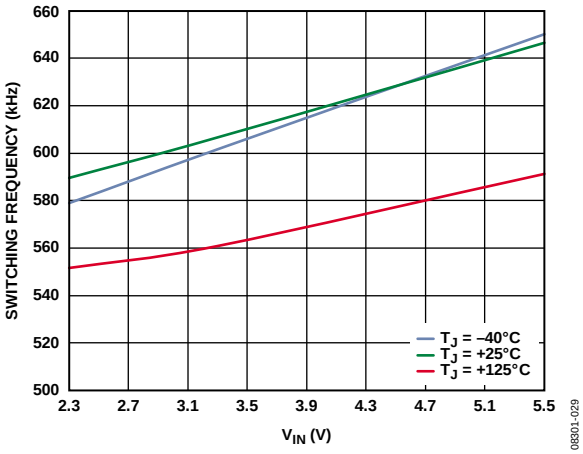


Figure 19. Switching Frequency vs. V_{IN} at 600 kHz

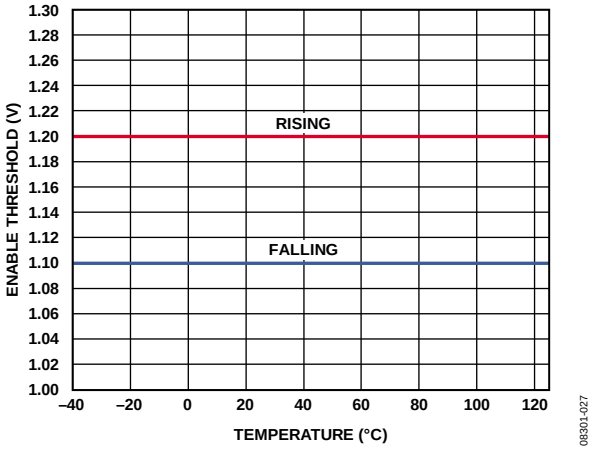


Figure 17. EN Threshold vs. Temperature

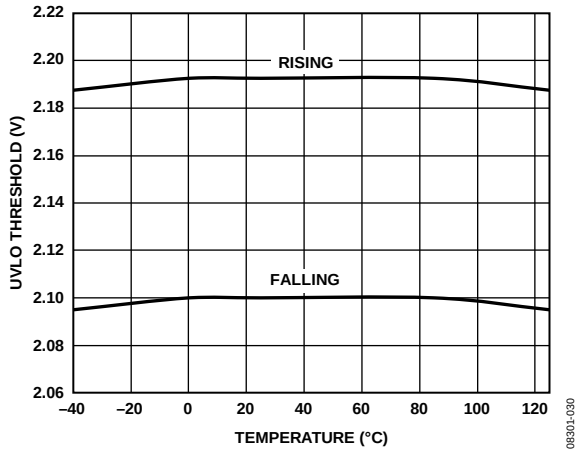


Figure 20. UVLO Threshold vs. Temperature (V_{IN} = 3.3 V)

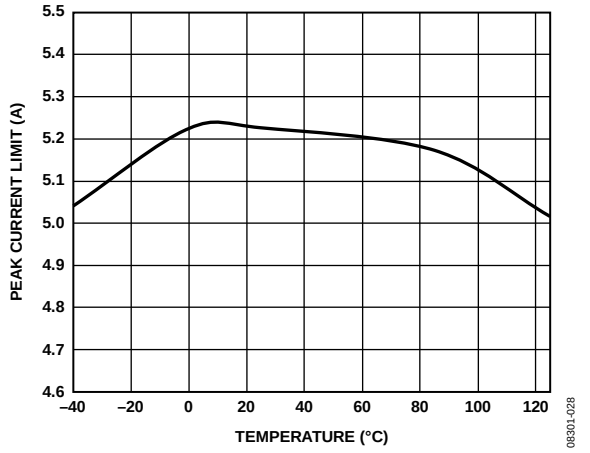


Figure 18. Peak Current Limit vs. Temperature (V_{IN} = 3.3 V)

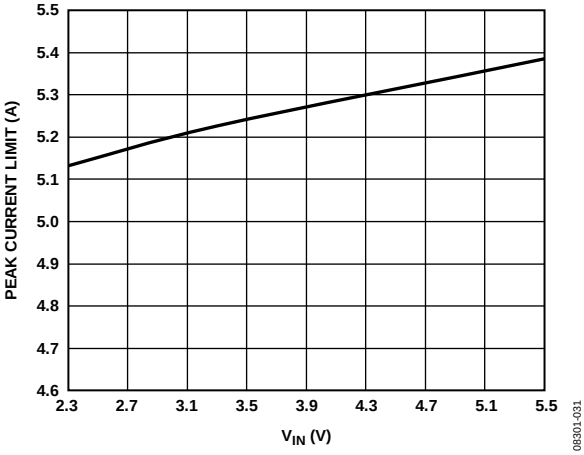


Figure 21. Peak Current Limit vs. V_{IN} (T_J = 25°C)

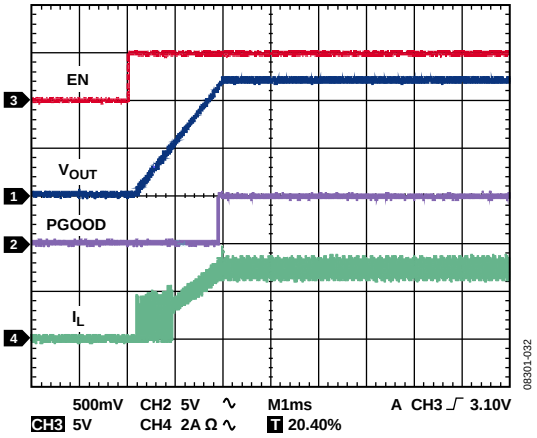


Figure 22. Soft Start with Full Load (1.2 MHz, V_{IN} = 5 V)

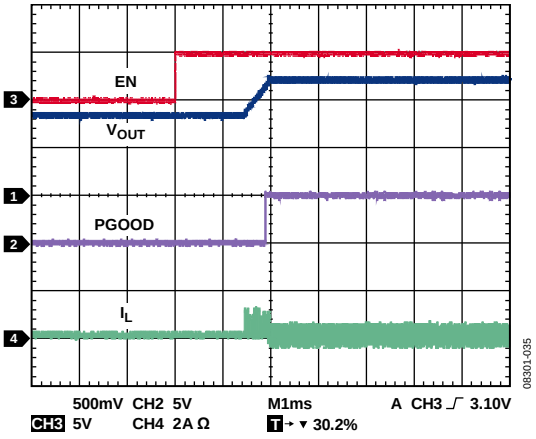


Figure 25. Soft Start with Precharge (1.2 MHz, V_{IN} = 5 V)

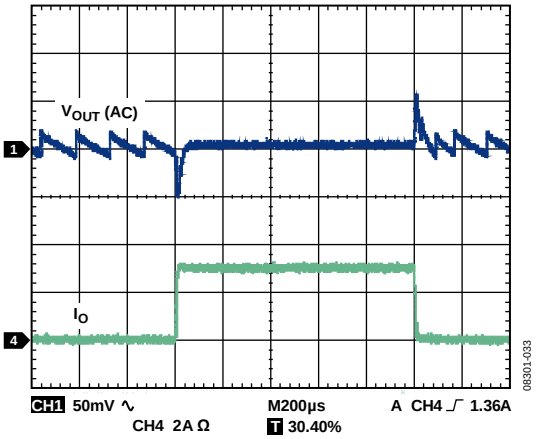


Figure 23. Load Transient (1.2 MHz, PFM, V_{IN} = 5 V)

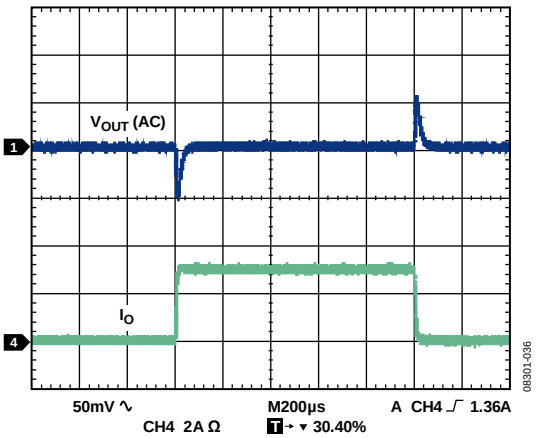


Figure 26. Load Transient (1.2 MHz, FPWM, V_{IN} = 5 V)

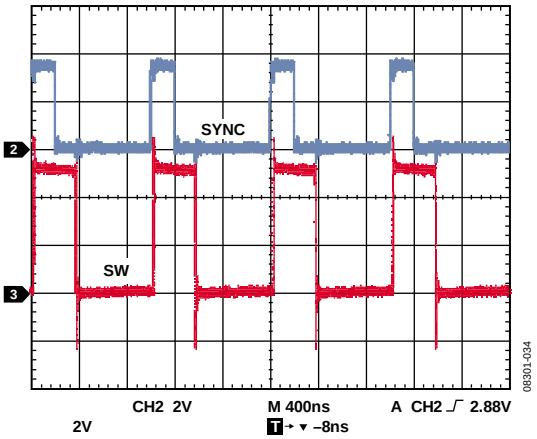


Figure 24. Synchronized to 1 MHz In Phase

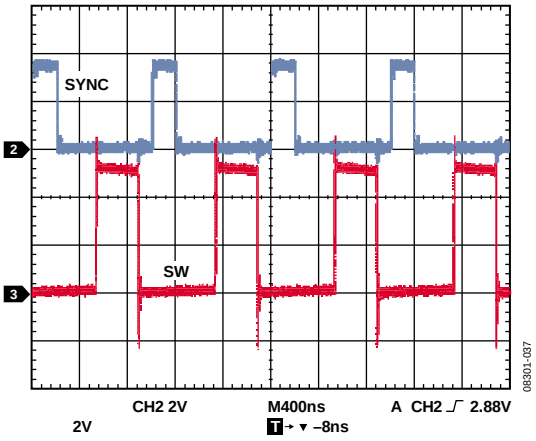


Figure 27. Synchronized to 1 MHz 180° Out of Phase

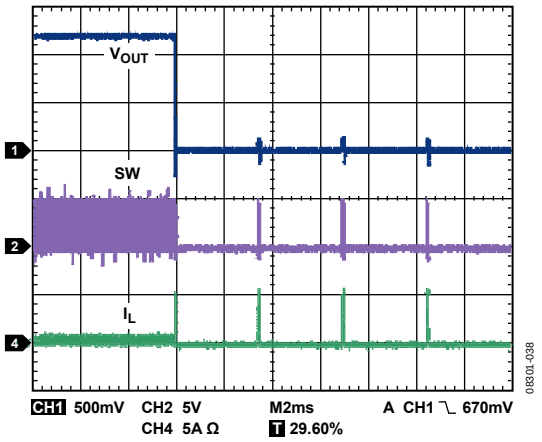


Figure 28. Output Short

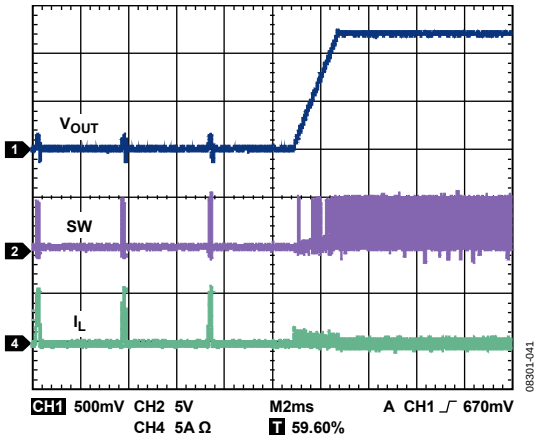


Figure 31. Output Short Recovery

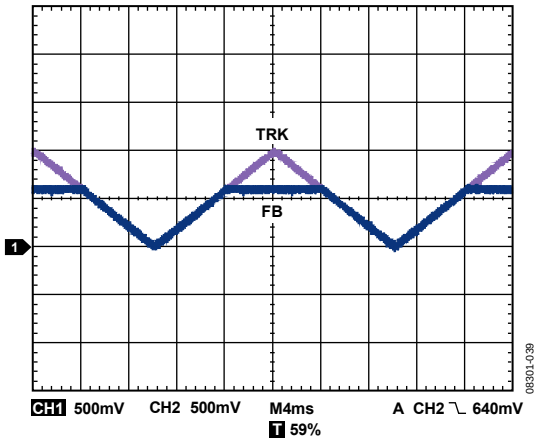


Figure 29. Tracking Function

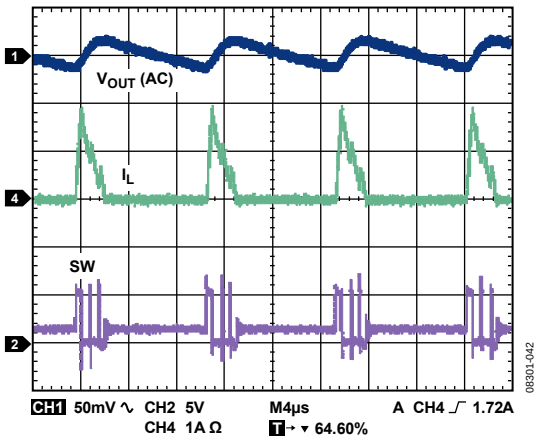


Figure 32. PFM Mode

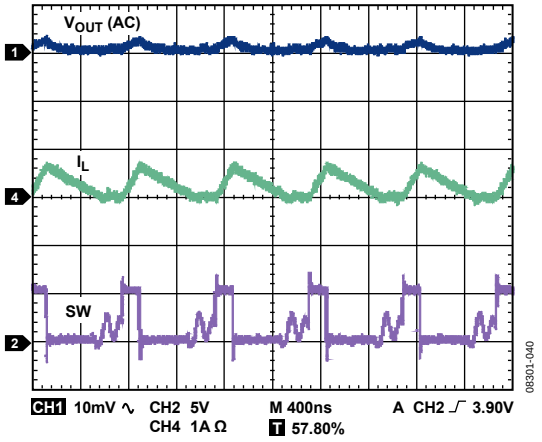


Figure 30. Discontinuous Conduction Mode (DCM)

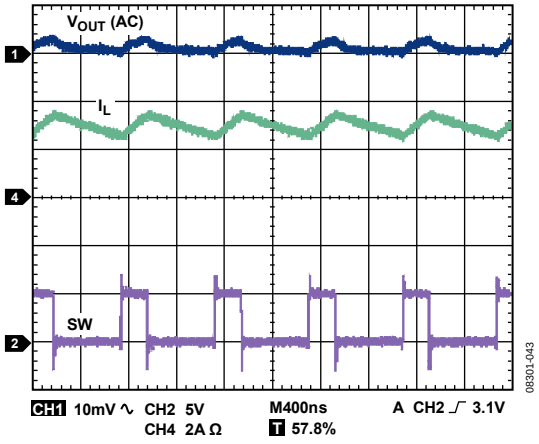


Figure 33. Continuous Conduction Mode (CCM)

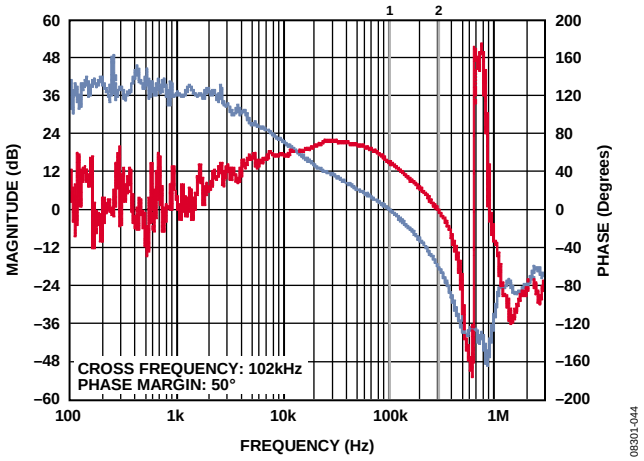


Figure 34. Bode Plot at V_{IN} = 5 V, V_{OUT} = 1.0 V, I_O = 3 A, f_S = 1.2 MHz

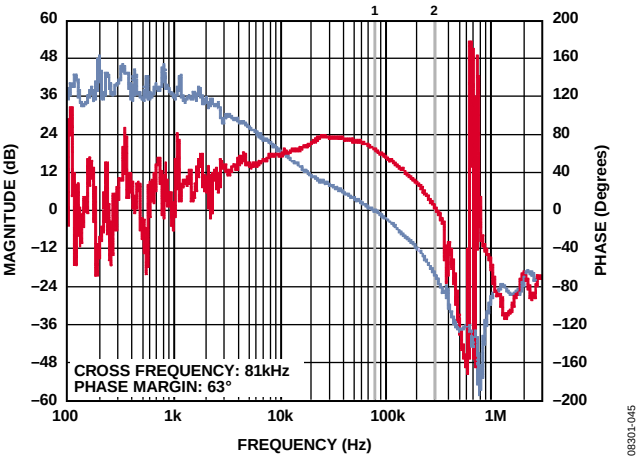


Figure 35. Bode Plot at V_{IN} = 5 V, V_{OUT} = 1.5 V, I_O = 3 A, f_S = 1.2 MHz

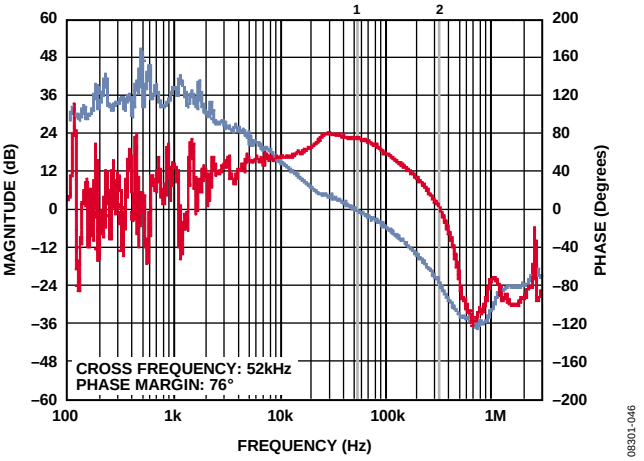


Figure 36. Bode Plot at V_{IN} = 5 V, V_{OUT} = 2.5 V, I_O = 3 A, f_S = 1.2 MHz

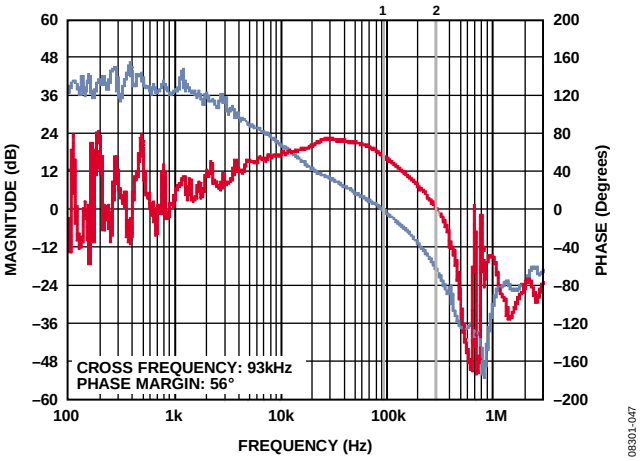


Figure 37. Bode Plot at V_{IN} = 5 V, V_{OUT} = 1.2 V, I_O = 3 A, f_S = 1.2 MHz

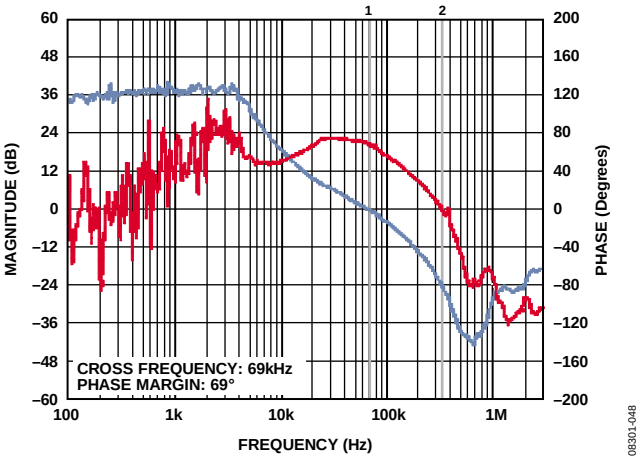


Figure 38. Bode Plot at V_{IN} = 5 V, V_{OUT} = 1.8 V, I_O = 3 A, f_S = 1.2 MHz

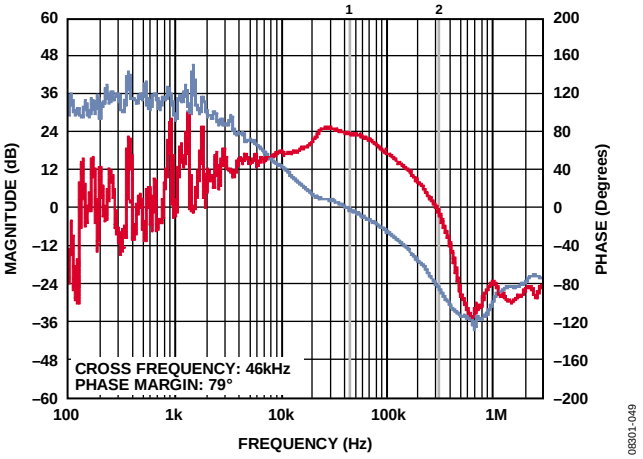


Figure 39. Bode Plot at V_{IN} = 5 V, V_{OUT} = 3.3 V, I_O = 3 A, f_S = 1.2 MHz

FUNCTIONAL BLOCK DIAGRAM

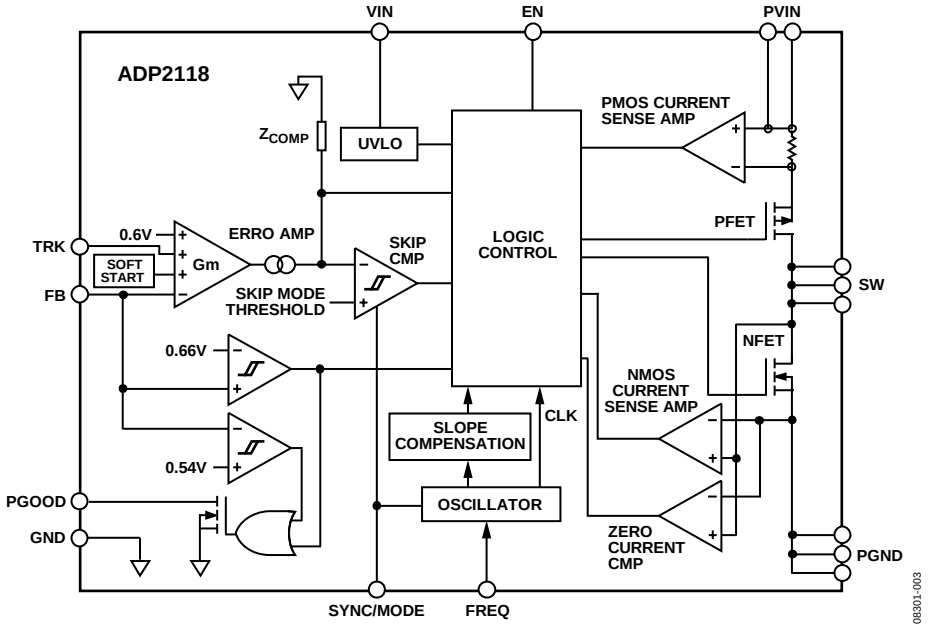


Figure 40. Functional Block Diagram

THEORY OF OPERATION

The ADP2118 is a step-down, dc-to-dc converter that uses fixed frequency, peak current-mode architecture with an integrated high-side switch and low-side synchronous rectifier. The high switching frequency and tiny 16-lead, 4 mm × 4 mm LFCSP_WQ package allow for a small step-down dc-to-dc converter solution. The integrated high-side switch (P-channel MOSFET) and synchronous rectifier (N-channel MOSFET) yield high efficiency at medium-to-full loads, and light load efficiency is improved by PFM mode.

The ADP2118 operates with an input voltage from 2.3 V to 5.5 V and regulates the output voltage down to 0.6 V. The ADP2118 is also available with preset output voltage options of 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, and 1.0 V.

CONTROL SCHEME

The ADP2118 uses the fixed frequency, peak current mode PWM control architecture and operates in PWM mode for medium-to-full loads but shifts to PFM mode (if enabled) at light loads to maintain high efficiency. When operating in fixed frequency PWM mode, the duty cycle of the integrated switches is adjusted to regulate the output voltage. When operating in PFM mode at light loads, the switching frequency is adjusted to regulate the output voltage.

The ADP2118 operates in PWM mode when the load current is greater than the pulse-skipping threshold current. At load currents below this value, the converter smoothly transitions to the PFM mode of operation.

PWM MODE OPERATION

In PWM mode, the ADP2118 operates at a fixed frequency set by the FREQ pin. At the start of each oscillator cycle, the P-channel MOSFET switch is turned on, putting a positive voltage across the inductor. Current in the inductor increases until the current sense signal crosses the peak inductor current level, turns off the P-channel MOSFET switch, and turns on the N-channel MOSFET synchronous rectifier. This puts a negative voltage across the inductor, causing the inductor current to decrease. The synchronous rectifier stays on for the rest of the cycle or until the inductor current reaches zero, which causes the zero-crossing comparator to turn off the N-channel MOSFET as well.

The peak inductor current level is set by V_{COMP}. The V_{COMP} is the output of a transconductance error amplifier that compares the feedback voltage with an internal 0.6 V reference.

PFM MODE OPERATION

When PFM mode is enabled, the ADP2118 smoothly transitions to the variable frequency PFM mode of operation when the load current decreases below the pulse-skipping threshold current, switching only as necessary to maintain the output voltage within regulation. When the output voltage drops below regulation, the ADP2118 enters PWM mode for a few oscillator cycles to increase the output voltage back to regulation. During the wait time between bursts, both power switches are off, and the output capacitor supplies all the load current. Because the output voltage dips and recovers occasionally, the output voltage ripple in this mode is larger than the ripple in the PWM mode of operation.

SLOPE COMPENSATION

Slope compensation stabilizes the internal current control loop of the ADP2118 when operating close to and beyond 50% duty cycle to prevent subharmonic oscillations. It is implemented by summing an artificial voltage ramp to the current sense signal during the on-time of the P-channel MOSFET switch. This voltage ramp depends on the output voltage. When operating at high output voltages, there is more slope compensation. The slope compensation ramp value determines the minimum inductor that can be used to prevent subharmonic oscillations.

ENABLE/SHUTDOWN

The EN pin is a precision analog input that enables the device when the voltage exceeds 1.2 V (typical) and has 100 mV hysteresis. When the enable voltage falls below 1.1 V (typical) the part turns off. To force the ADP2118 to automatically start when input power is applied, connect EN to VIN.

When the ADP2118 is shut down, the soft start capacitor is discharged. This causes a new soft start cycle to begin when the part is reenabled.

An internal pull-down resistor (1 MΩ) prevents an accidental enable if EN is left floating.

INTEGRATED SOFT START

The ADP2118 has integrated soft start circuitry to limit the output voltage rise time and reduce inrush current at startup. The soft start time is fixed at 2048 clock cycles.

If the output voltage is precharged prior to turn-on, the ADP2118 prevents a reverse inductor current (that would discharge the output capacity) until the soft start voltage exceeds the voltage on the FB pin.

TRACKING

The ADP2118 has a tracking input, TRK, that allows the output voltage to track another voltage (master voltage). It is especially useful in core and I/O voltage tracking for FPGAs, DSPs, and ASICs.

The internal error amplifier includes three positive inputs: the internal reference voltage, the soft start voltage, and the TRK voltage. The error amplifier regulates the FB voltage to the lowest of the three voltages. To track a master voltage, tie the TRK pin to a resistor divider from the master voltage.

If the TRK function is not used, connect the TRK pin to VIN.

OSCILLATOR AND SYNCHRONIZATION

The internal oscillator of ADP2118 can be set to 600 kHz or 1.2 MHz. Drive the FREQ pin low for 600 kHz; drive FREQ pin high for 1.2 MHz.

To synchronize the ADP2118, drive an external clock at the SYNC/MODE pin. The frequency of the external clock can be in the range of 600 kHz to 1.4 MHz. During synchronization, the converter operates in CCM mode only.

If the FREQ pin is low, the switching frequency is in phase with the external clock; if the FREQ pin is high, the switching frequency is 180° out of phase with the external clock.

CURRENT LIMIT AND SHORT-CIRCUIT PROTECTION

The ADP2118 has a peak current limit protection circuit to prevent current runaway. The peak current is limited at 5.2 A. When the inductor peak current reaches the current limit value, the high-side MOSFET turns off and the low-side MOSFET turns on until the next cycle while the overcurrent counter increments. If the overcurrent counter count exceeds 10, the part enters hiccup mode. The high-side FET and low-side FET are both turned off. The part remains in this mode for 4096 clock cycles and then attempts to restart from soft start. If the current limit fault has cleared, the part resumes normal operation. Otherwise, it reenters hiccup mode again after counting 10 current-limit violations.

OVERVOLTAGE PROTECTION (OVP)

The output voltage is continuously monitored by a comparator through the FB pin, which is at 0.6 V (typical) under normal operation. This comparator is set to activate when the FB voltage exceeds 0.66 V (typical), thus indicating an output overvoltage condition. If the voltage remains above this threshold for 16 clock cycles, the high-side MOSFET turns off and the low-side MOSFET turns on until the current through it reaches the limit (−0.9 A for forced continuous mode and 0 A for PFM mode). Thereafter, both the MOSFETs are held in the off state until FB falls below 0.54 V (typical), and then the part restarts. The behavior of PGOOD under this condition is described in the Power Good section.

UNDERVOLTAGE LOCKOUT (UVLO)

Undervoltage lockout circuitry is integrated on the ADP2118. If the input voltage drops below 2.1 V, the ADP2118 shuts down, and both the power switch and the synchronous rectifier turn off. When the voltage rises again above 2.2 V, the soft start period is initiated, and the part is enabled.

THERMAL SHUTDOWN

In the event that the ADP2118 junction temperature rises above 140°C, the thermal shutdown circuit turns off the converter. Extreme junction temperatures can be the result of high current operation, poor circuit board design, and/or high ambient temperature. A 15°C hysteresis is included so that when thermal shutdown occurs, the ADP2118 does not return to operation until the on-chip temperature drops below 125°C. When coming out of thermal shutdown, soft start is initiated.

POWER GOOD

PGOOD is an active high, open-drain output and requires a resistor to pull it up to a voltage. A high indicates that the voltage on the FB pin (and therefore the output voltage) is within 10% of the desired value. A low on this pin indicates that the voltage on the FB pin is not within 10% of the desired value. There is a 16 cycle waiting period after FB is detected as being out of bounds. If FB returns to within the ±10% range, it is ignored by PGOOD circuitry.

APPLICATIONS INFORMATION

This section describes the external components selection for the ADP2118. The typical application circuit is shown in Figure 41.

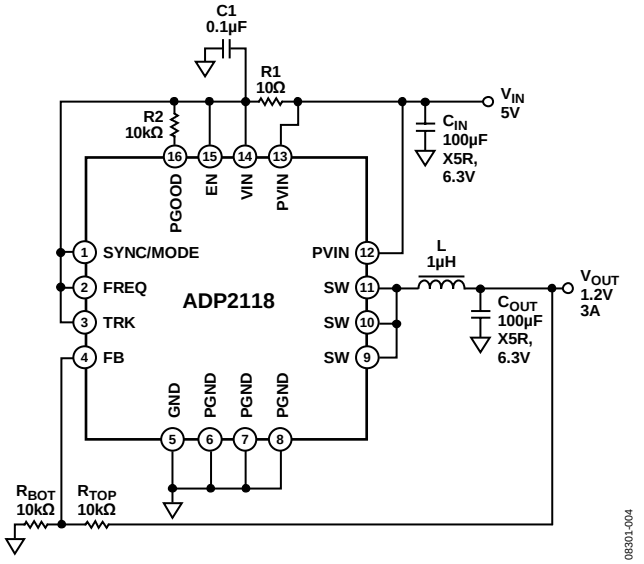


Figure 41. Application Circuit

OUTPUT VOLTAGE SELECTION

The output voltage of the adjustable version of the ADP2118 can be set by an external resistive voltage divider by using the following equation to set the voltage:

$$V_{OUT} = 0.6 \times \left(1 + \frac{R_{TOP}}{R_{BOT}}\right)$$

To limit output voltage accuracy degradation due to FB bias current (0.1 µA maximum) to less than 0.5% (maximum), ensure that R_{BOT} is less than 30 kΩ.

INDUCTOR SELECTION

The inductor value is determined by the operating frequency, input voltage, output voltage, and ripple current. Using a small inductor leads to larger inductor current ripple and provides fast transient response but degrades efficiency, whereas a large inductor value leads to small current ripple and good efficiency but slow transient response. As a guideline, the inductor current ripple, ΔI_L, is typically set to 1/3 of the maximum load current trade-off between the transient response and efficiency. The inductor can be calculated using the following equation:

$$L = \frac{(V_{IN} - V_{OUT}) \times D}{\Delta I_L \times f_S}$$

where:
V_{IN} is the input voltage.
V_{OUT} is the output voltage.
ΔI_L is the inductor current ripple.
D is the duty cyle.

$$D = \frac{V_{OUT}}{V_{IN}}$$

The ADP2118 uses slope compensation in the current loop to prevent subharmonic oscillations when the duty cycle is larger than 50%. The internal slope compensation limits the minimum inductor value.

The negative current limit (−0.9 A) also limits the minimum inductor value. The inductor current ripple (ΔI_L) calculated by the selected inductor should not exceed 1.8 A.

The peak inductor current should be kept below the peak current limit threshold value and can be calculated as

$$I_{PEAK} = I_O + \frac{\Delta I_L}{2}$$

Ensure that the rms current of the selected inductor is greater than the maximum load current and that its saturation current is greater than the peak current limit of the converter.

OUTPUT CAPACITOR SELECTION

The output voltage ripple, load step transient, and loop stability determine the output capacitor selection.

The output ripple is determined by the ESR and the capacitance.

$$\Delta V_{OUT} = \Delta I_L \times \left(ESR + \frac{1}{8 \times C_{OUT} \times f_S}\right)$$

The load transient response depends on the inductor, output capacitor, and the control loop.

The ADP2118 has integrated loop compensation for simple power design. Table 5 and Table 6 show the typical recommended inductors and capacitors for the ADP2118. X5R or X7R ceramic capacitors are highly recommended.

Table 5. Recommended L and C_{OUT} Value at f_S = 1.2 MHz

V_{IN} (V)	V_{OUT} (V)	L (µH)	C_{OUT} (µF)
3.3	1.0	1	100 + 47
3.3	1.2	1	100
3.3	1.5	1	100
3.3	1.8	1	100
3.3	2.5	1	100
5	1.0	1	100 + 47
5	1.2	1	100
5	1.5	1	100
5	1.8	1	100
5	2.5	1	100
5	3.3	1	100

Table 6. Recommended L and C_{OUT} Value at f_S = 600 kHz

V_{IN} (V)	V_{OUT} (V)	L (µH)	C_{OUT} (µF)
3.3	1.0	1.5	100 + 47
3.3	1.2	1.5	100
3.3	1.5	1.5	100
3.3	1.8	1.5	100
3.3	2.5	1.5	100
5	1.0	1.5	100 + 47
5	1.2	1.5	100
5	1.5	2.2	100
5	1.8	2.2	100
5	2.5	2.2	100
5	3.3	2.2	100

Higher or lower inductors and output capacitors can be used in the converter, but the system stability and load transient performance need to be checked.

The minimum output capacitor can be 47 µF. If f_S = 1.2 MHz, the inductor range is 0.8 µH to 3.3 µH. If f_S = 600 kHz, the inductor range is 1.5 µH to 3.3 µH.

Table 7. Recommended Inductors

Manufacturer	Part Number
Coilcraft	MSS1038, MSS1048, MSS1260
Sumida	CDRH103R, CDRH104R, CDRH105R

Table 8. Recommended Capacitors

Manufacturer	Part Number	Description
Murata	GRM32ER60J107ME20	100 µF, 6.3 V, X5R, 1210
Murata	GRM32ER60J476ME20	47 µF, 6.3 V, X5R, 1210
TDK	C3225X5R0J107M	100 µF, 6.3 V, X5R, 1210
TDK	C3225X5R0J476M	47 µF, 6.3 V, X5R, 1210

INPUT CAPACITOR SELECTION

The input capacitor reduces the input voltage ripple caused by the switch current on PVIN. Place the input capacitor as close as possible to the PVIN pin. A 22 µF or 47 µF ceramic capacitor is recommended. The rms current rating of the input capacitor should be larger than the following equation:

$$I_{RMS} = I_O \times \sqrt{D \times (1-D)}$$

VOLTAGE TRACKING

The ADP2118 includes a tracking feature that allows the ADP2118 output (slave voltage) to be configured to track an external voltage (master voltage), as shown in Figure 42.

A common application is coincident tracking, shown in Figure 43. Coincident tracking limits the slave output voltage to be the same as the master voltage until it reaches regulation. Connect the TRK pin to a resistor divider from the master voltage. For coincident tracking, set $R_{TRKT} = R_{TOP}$ and $R_{TRKB} = R_{BOT}$.

Ratiometric tracking is shown in Figure 44. The slave output is limited to a fraction of the master voltage. In this application, the slave and master voltages reach the final value at the same time. The ratio of the slave output voltage to the master voltage is a function of the two dividers.

$$\frac{V_{SLAVE}}{V_{MASTER}} = \frac{1+\frac{R_{TOP}}{R_{BOT}}}{1+\frac{R_{TRKT}}{R_{TRKB}}}$$

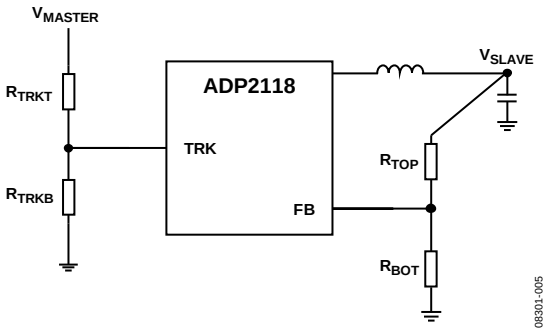


Figure 42. Voltage Tracking

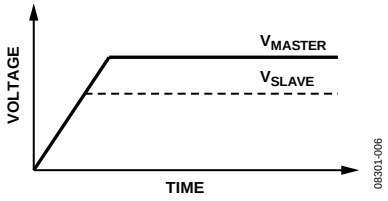


Figure 43. Coincident Tracking

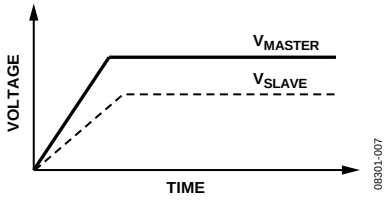


Figure 44. Ratiometric Tracking

TYPICAL APPLICATION CIRCUITS

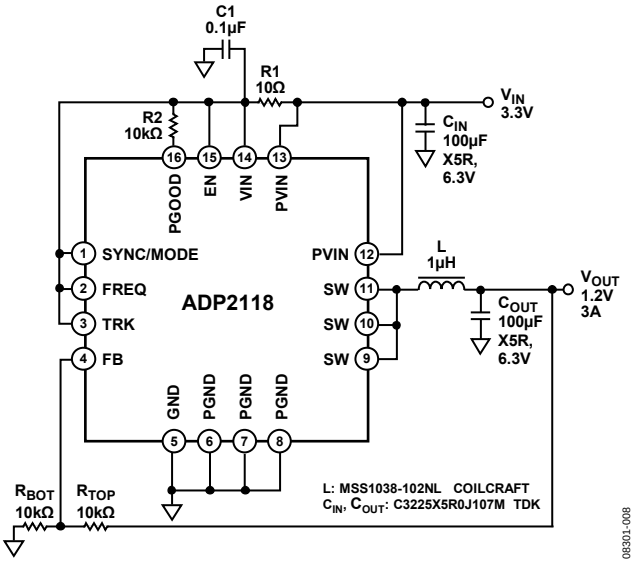


Figure 45. 1.2 V, 3 A, 1.2 MHz Step-Down Regulator, Force Continuous Conduction Mode

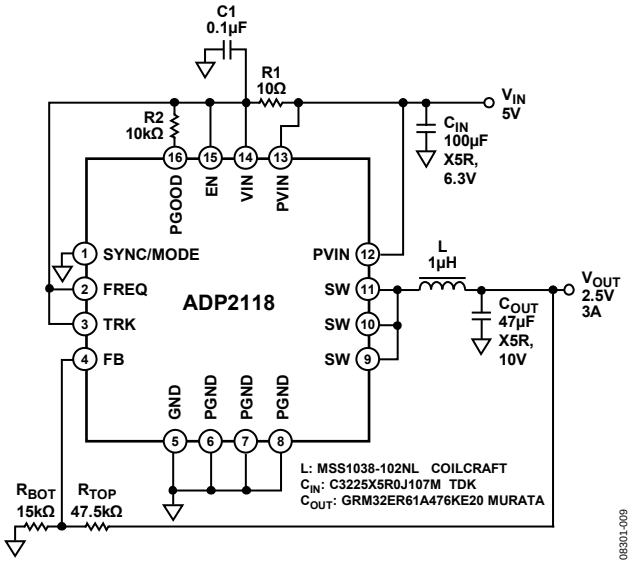


Figure 46. 2.5 V, 3 A, 1.2 MHz Step-Down Regulator, Enable PFM Mode

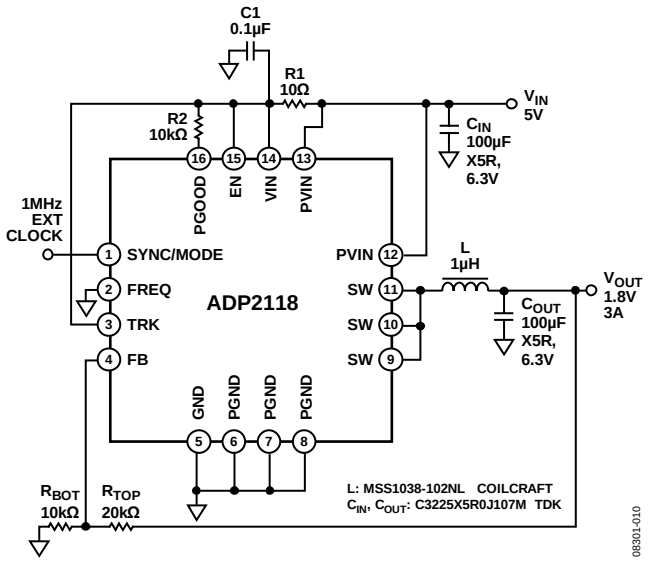


Figure 47. 1.8 V, 3 A Step-Down Regulator,
Synchronized to 1 MHz In Phase with the External Clock

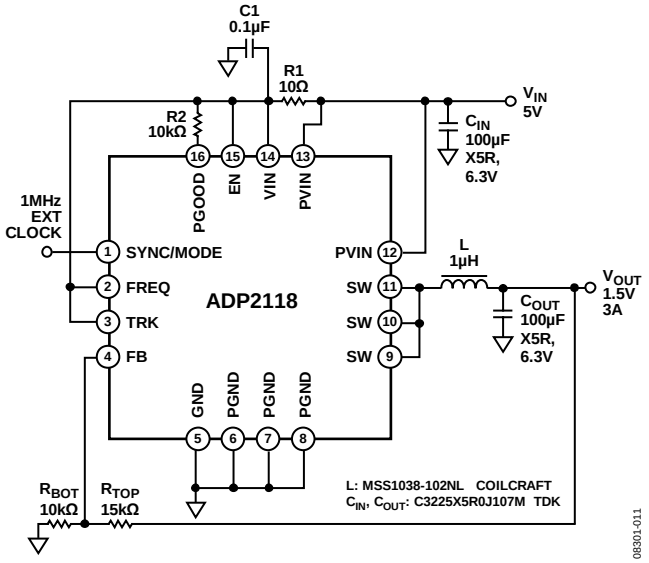


Figure 48. 1.5 V, 3 A Step-Down Regulator, Synchronized to 1 MHz,
180° Out of Phase with the External Clock

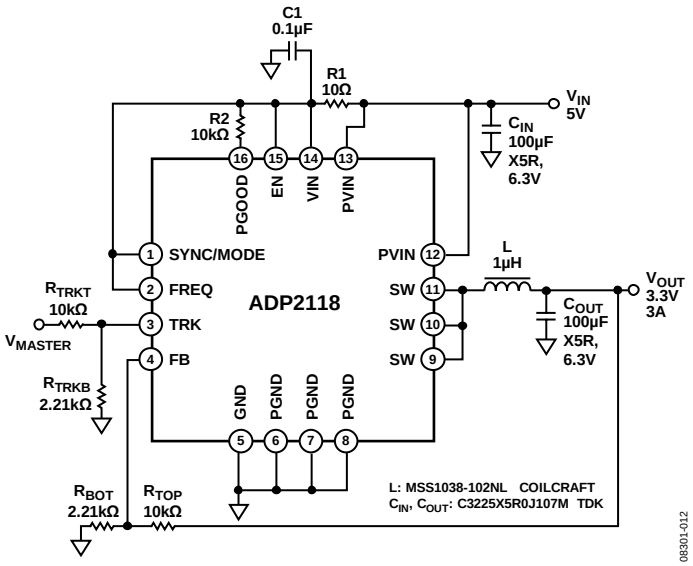
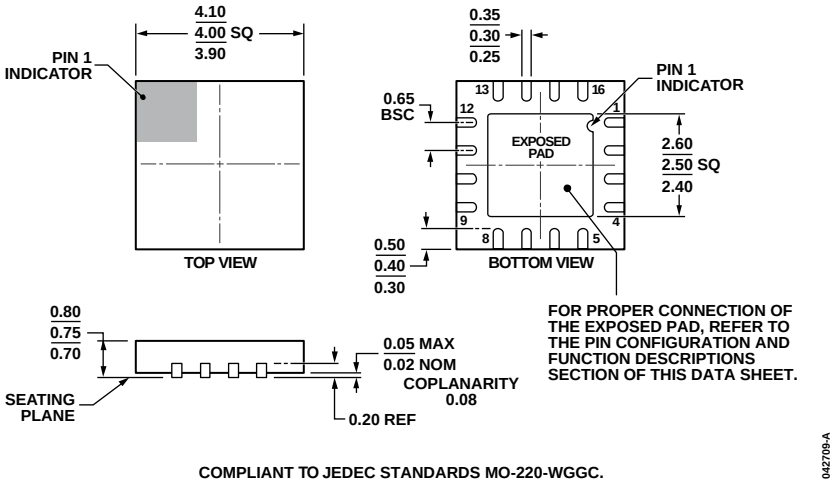


Figure 49. 3.3 V, 3 A, 1.2 MHz Step-Down Regulator, Tracking Mode

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WGGC.

Figure 50. 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Very Thin Quad
(CP-16-26)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Output Voltage	Package Description	Package Option
ADP2118ACPZ-R7[1]	−40°C to +125°C	Adjustable	16-Lead LFCSP_WQ	CP-16-26
ADP2118ACPZ-1.0-R7[1]	−40°C to +125°C	1.0 V	16-Lead LFCSP_WQ	CP-16-26
ADP2118ACPZ-1.2-R7[1]	−40°C to +125°C	1.2 V	16-Lead LFCSP_WQ	CP-16-26
ADP2118ACPZ-1.5-R7[1]	−40°C to +125°C	1.5 V	16-Lead LFCSP_WQ	CP-16-26
ADP2118ACPZ-1.8-R7[1]	−40°C to +125°C	1.8 V	16-Lead LFCSP_WQ	CP-16-26
ADP2118ACPZ-2.5-R7[1]	−40°C to +125°C	2.5 V	16-Lead LFCSP_WQ	CP-16-26
ADP2118ACPZ-3.3-R7[1]	−40°C to +125°C	3.3 V	16-Lead LFCSP_WQ	CP-16-26

[1] Z = RoHS Compliant Part.

NOTES

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