

Silicon NPN Power Transistors

BU102

DESCRIPTION

- With TO-3 package
- $V_{CEO(sus)}=150V$ (min)

APPLICATIONS

- Designed for horizontal deflection output stage of CTV receivers

PINNING(see fig.2)

PIN	DESCRIPTION
1	Base
2	Emitter
3	Collector

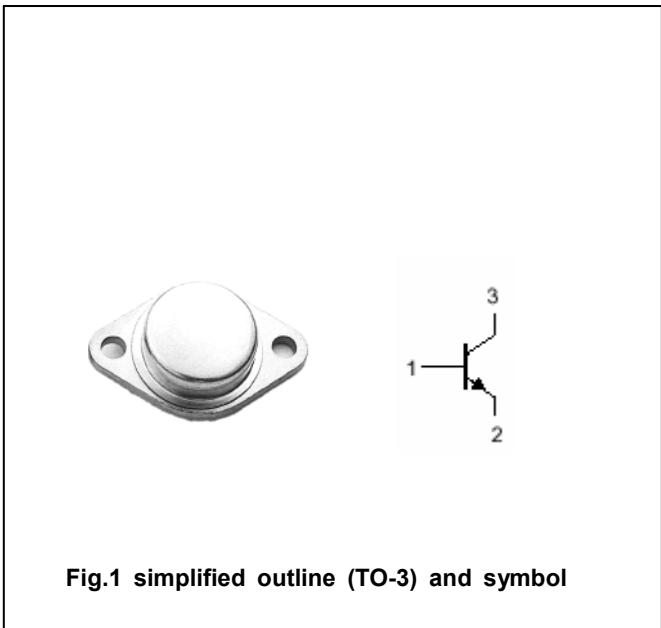


Fig.1 simplified outline (TO-3) and symbol

Absolute maximum ratings(Ta=□)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	400	V
V_{CEO}	Collector-emitter voltage	Open base	150	V
V_{EBO}	Emitter-base voltage	Open collector	6	V
I_C	Collector current		7	A
P_C	Collector power dissipation	$T_C=25□$	100	W
T_j	Junction temperature		150	□
T_{stg}	Storage temperature		-55~150	□

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CHARACTERISTICS

T_j=25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V _{CEO(SUS)}	Collector-emitter sustaining voltage	I _C =100mA; I _B =0	150			V
V _{(BR)EBO}	Emitter-base breakdown voltage	I _E =1mA; I _C =0	6			V
V _{(BR)CBO}	Collector-base breakdown voltage	I _C =1mA; I _E =0	400			V
V _{CEsat}	Collector-emitter saturation voltage	I _C =5 A; I _B =1.0 A			2.0	V
V _{BEsat}	Base-emitter saturation voltage	I _C =5 A; I _B =1.0 A			2.5	V
I _{CBO}	Collector cut-off current	V _{CB} =400V; I _E =0			0.1	mA
I _{CEO}	Collector cut-off current	V _{CE} =100V; I _E =0			1.0	mA
I _{EBO}	Emitter cut-off current	V _{EB} =5V; I _C =0			0.1	mA
h _{FE}	DC current gain	I _C =1A ; V _{CE} =5V	30		120	

PACKAGE OUTLINE

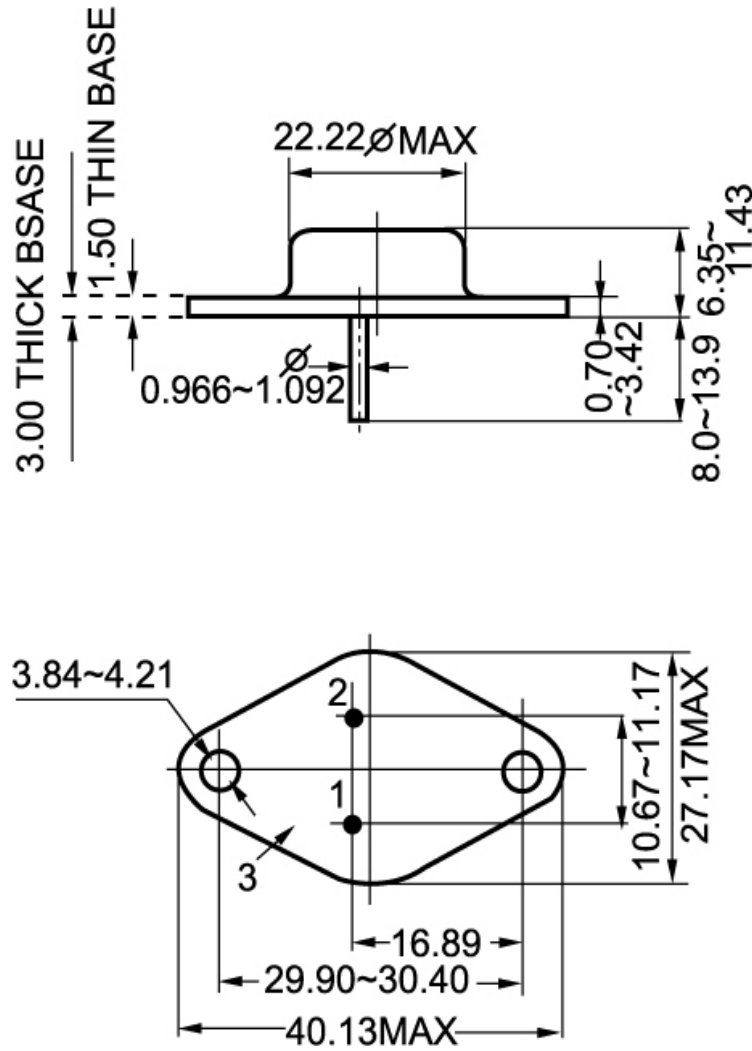


Fig.2 Outline dimensions