

CD4017BC • CD4022BC

Decade Counter/Divider with 10 Decoded Outputs • Divide-by-8 Counter/Divider with 8 Decoded Outputs

General Description

The CD4017BC is a 5-stage divide-by-10 Johnson counter with 10 decoded outputs and a carry out bit.

The CD4022BC is a 4-stage divide-by-8 Johnson counter with 8 decoded outputs and a carry out bit.

These counters are cleared to their zero count by a logical "1" on their reset line. These counters are advanced on the positive edge of the clock signal when the clock enable signal is in the logical "0" state.

The configuration of the CD4017BC and CD4022BC permits medium speed operation and assures a hazard free counting sequence. The 10/8 decoded outputs are normally in the logical "0" state and go to the logical "1" state only at their respective time slot. Each decoded output remains high for 1 full clock cycle. The carry-out signal completes a full cycle for every 10/8 clock input cycles and is used as a ripple carry signal to any succeeding stages.

Features

- Wide supply voltage range: 3.0V to 15V
- High noise immunity: $0.45 V_{DD}$ (typ.)
- Low power Fan out of 2 driving 74L TTL compatibility: or 1 driving 74LS
- Medium speed operation: 5.0 MHz (typ.) with $10V V_{DD}$
- Low power: 10 μ W (typ.)
- Fully static operation

Applications

- Automotive
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering

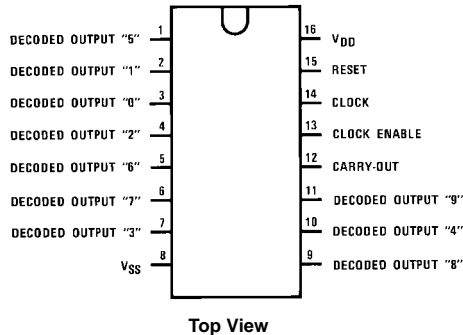
Ordering Code:

| Order Number | Package Number | Package Description |
|--------------|----------------|--|
| CD4017BCM | M16A | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| CD4017BCSJ | M16D | 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| CD4017BCN | N16E | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |
| CD4022BCM | M16A | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| CD4022BCN | N16E | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

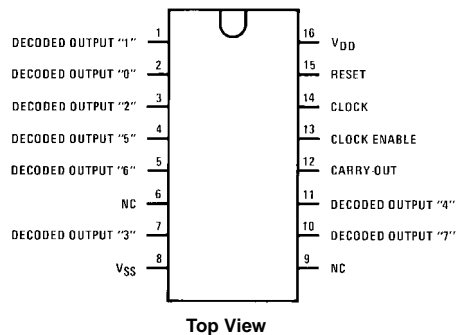
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagrams

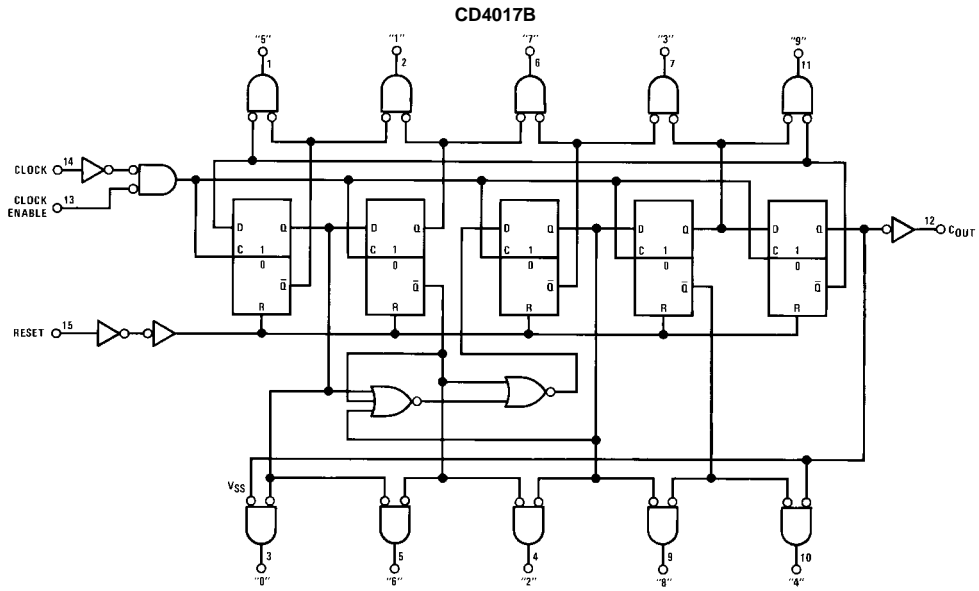
Pin Assignments for DIP, SOIC and SOP
CD4017B



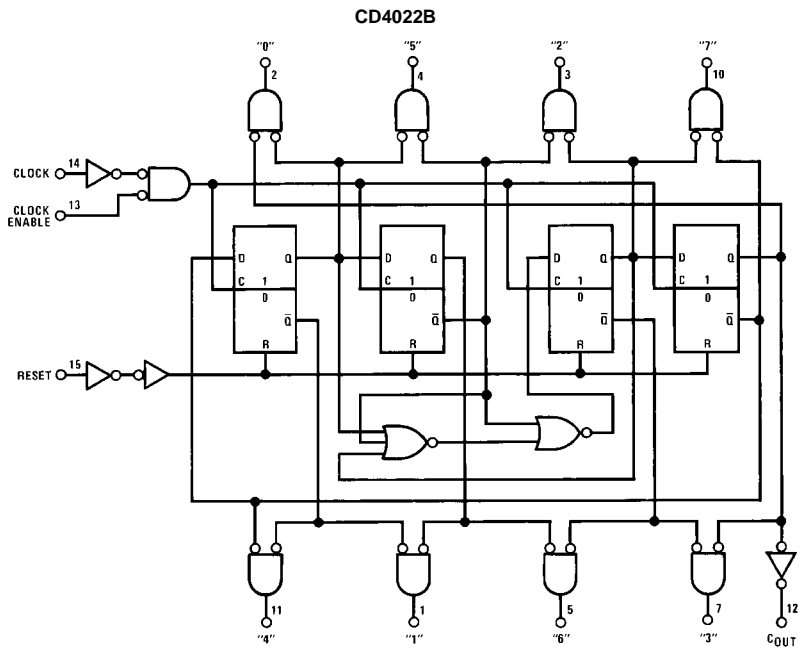
Pin Assignments for DIP and SOIC
CD4022B



Logic Diagrams



Terminal No. 8 = GND
 Terminal No. 16 = V_{DD}



Terminal No. 16 = V_{DD}
 Terminal No. 8 = GND

Absolute Maximum Ratings (Note 1)

(Note 2)

| | |
|--------------------------------|---|
| DC Supply Voltage (V_{DD}) | -0.5 V_{DC} to +18 V_{DC} |
| Input Voltage (V_{IN}) | -0.5 V_{DC} to V_{DD} +0.5 V_{DC} |
| Storage Temperature (T_S) | -65°C to +150°C |
| Power Dissipation (P_D) | |
| Dual-In-Line | 700 mW |
| Small Outline | 500 mW |
| Lead Temperature (T_L) | |
| (Soldering, 10 seconds) | 260°C |

Recommended Operating Conditions (Note 2)

| | |
|---------------------------------------|-----------------------------|
| DC Supply Voltage (V_{DD}) | +3 V_{DC} to +15 V_{DC} |
| Input Voltage (V_{IN}) | 0 to V_{DD} V_{DC} |
| Operating Temperature Range (T_A) | -40°C to +85°C |

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

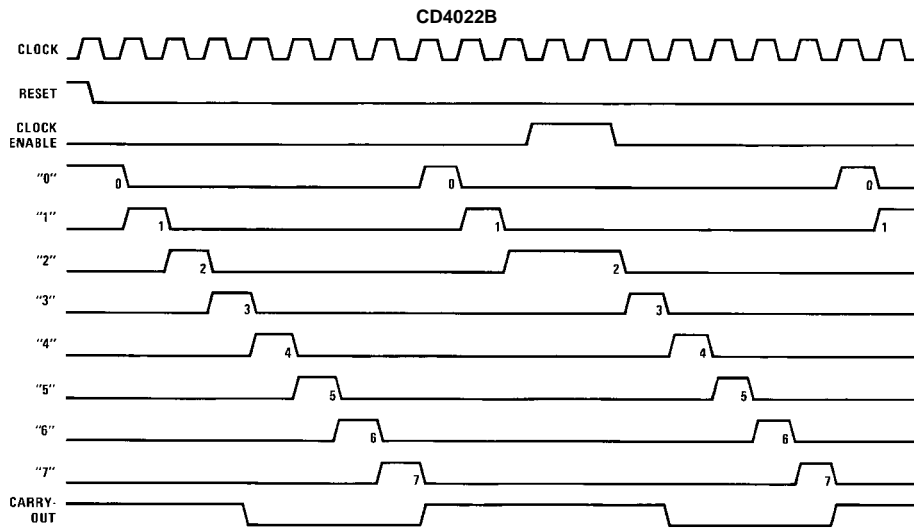
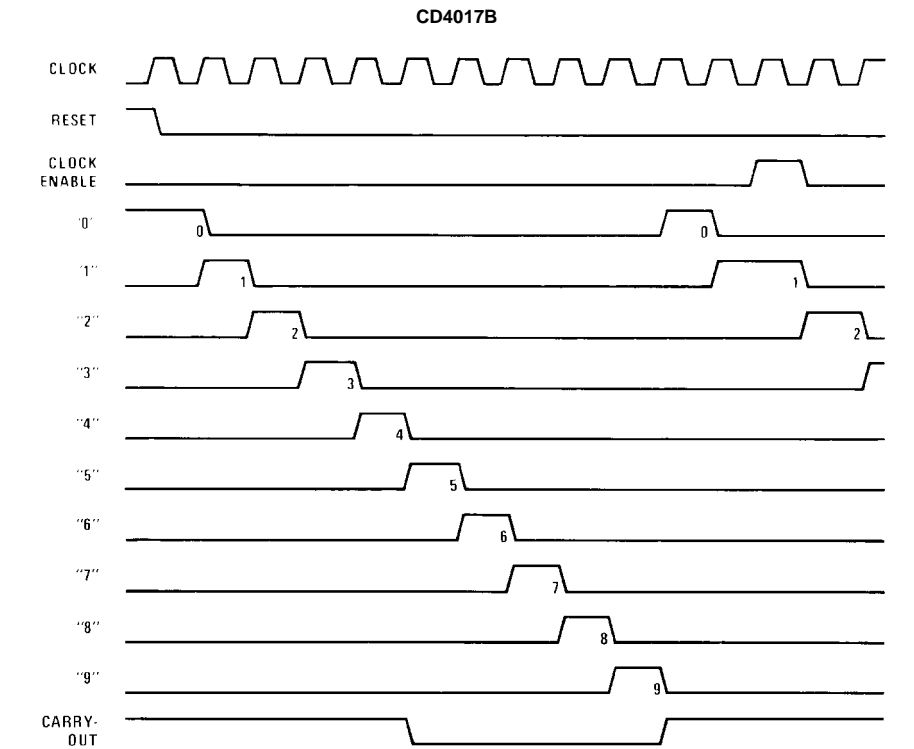
DC Electrical Characteristics (Note 2)

| Symbol | Parameter | Conditions | -40°C | | +25° | | | +85°C | | Units |
|----------|------------------------------------|---------------------------------------|-------|------|-------|------------|------|-------|------|---------|
| | | | Min | Max | Min | Typ | Max | Min | Max | |
| I_{DD} | Quiescent Device Current | $V_{DD} = 5V$ | | 20 | | 0.5 | 20 | | 150 | μA |
| | | $V_{DD} = 10V$ | | 40 | | 1.0 | 40 | | 300 | μA |
| | | $V_{DD} = 15V$ | | 80 | | 5.0 | 80 | | 600 | μA |
| V_{OL} | LOW Level Output Voltage | $ I_{OL} < 1.0 \mu A$ | | | | | | | | |
| | | $V_{DD} = 5V$ | | 0.05 | | 0 | 0.05 | | 0.05 | V |
| | | $V_{DD} = 10V$ | | 0.05 | | 0 | 0.05 | | 0.05 | V |
| | | $V_{DD} = 15V$ | | 0.05 | | 0 | 0.05 | | 0.05 | V |
| V_{OH} | HIGH Level Output Voltage | $ I_{OL} < 1.0 \mu A$ | | | | | | | | |
| | | $V_{DD} = 5V$ | 4.95 | | 4.95 | 5 | | 4.95 | | V |
| | | $V_{DD} = 10V$ | 9.95 | | 9.95 | 10 | | 9.95 | | V |
| | | $V_{DD} = 15V$ | 14.95 | | 14.95 | 15 | | 14.95 | | V |
| V_{IL} | LOW Level Input Voltage | $ I_{OL} < 1.0 \mu A$ | | | | | | | | |
| | | $V_{DD} = 5V, V_O = 0.5V$ or $4.5V$ | | 1.5 | | | 1.5 | | 1.5 | V |
| | | $V_{DD} = 10V, V_O = 1.0V$ or $9.0V$ | | 3.0 | | | 3.0 | | 3.0 | V |
| | | $V_{DD} = 15V, V_O = 1.5V$ or $13.5V$ | | 4.0 | | | 4.0 | | 4.0 | V |
| V_{IH} | HIGH Level Input Voltage | $ I_{OL} < 1.0 \mu A$ | | | | | | | | |
| | | $V_{DD} = 5V, V_O = 0.5V$ or $4.5V$ | 3.5 | | 3.5 | | | 3.5 | | V |
| | | $V_{DD} = 10V, V_O = 1.0V$ or $9.0V$ | 7.0 | | 7.0 | | | 7.0 | | V |
| | | $V_{DD} = 15V, V_O = 1.5V$ or $13.5V$ | 11.0 | | 11.0 | | | 11.0 | | V |
| I_{OL} | LOW Level Output Current (Note 3) | $V_{DD} = 5V, V_O = 0.4V$ | 0.52 | | 0.44 | 0.88 | | 0.36 | | mA |
| | | $V_{DD} = 10V, V_O = 0.5V$ | 1.3 | | 1.1 | 2.25 | | 0.9 | | mA |
| | | $V_{DD} = 15V, V_O = 1.5V$ | 3.6 | | 3.0 | 8.8 | | 2.4 | | mA |
| I_{OH} | HIGH Level Output Current (Note 3) | $V_{DD} = 5V, V_O = 4.6V$ | -0.2 | | -0.16 | -0.36 | | -0.12 | | mA |
| | | $V_{DD} = 10V, V_O = 9.5V$ | -0.5 | | -0.4 | -0.9 | | -0.3 | | mA |
| | | $V_{DD} = 15V, V_O = 13.5V$ | -1.4 | | -1.2 | -3.5 | | -1.0 | | mA |
| I_{IN} | Input Current | $V_{DD} = 15V, V_{IN} = 0V$ | | -0.3 | | -10^{-5} | -0.3 | | -1.0 | μA |
| | | $V_{DD} = 15V, V_{IN} = 15V$ | | 0.3 | | 10^{-5} | 0.3 | | 1.0 | μA |

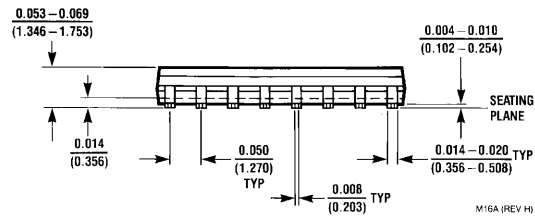
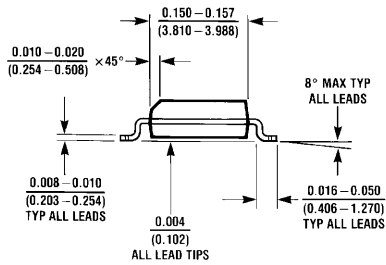
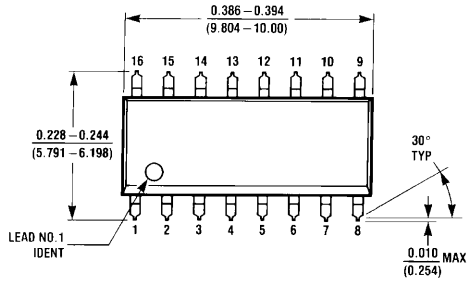
Note 3: I_{OL} and I_{OH} are tested one output at a time.

| AC Electrical Characteristics (Note 4) | | | | | | | |
|---|--|-----------------------|--|------|------|-------|-----|
| T _A = 25°C, C _L = 50 pF, R _L = 200k, t _{rCL} and t _{fCL} = 20 ns, unless otherwise specified | | | | | | | |
| Symbol | Parameter | Conditions | Min | Typ | Max | Units | |
| CLOCK OPERATION | | | | | | | |
| t _{PHL} , t _{PLH} | Propagation Delay Time Carry Out Line | V _{DD} = 5V | | 415 | 800 | ns | |
| | | V _{DD} = 10V | | 160 | 320 | ns | |
| | | V _{DD} = 15V | | 130 | 250 | ns | |
| | Carry Out Line | V _{DD} = 5V | C _L = 15 pF | 240 | 480 | ns | |
| | | V _{DD} = 10V | | 85 | 170 | ns | |
| | | V _{DD} = 15V | | 70 | 140 | ns | |
| | Decode Out Lines | V _{DD} = 5V | | 500 | 1000 | ns | |
| | | V _{DD} = 10V | | 200 | 400 | ns | |
| | | V _{DD} = 15V | | 160 | 320 | ns | |
| t _{TLH} , t _{THL} | Transition Time Carry Out and Decode Out Lines | t _{TLH} | V _{DD} = 5V | | 200 | 360 | ns |
| | | | V _{DD} = 10V | | 100 | 180 | ns |
| | | | V _{DD} = 15V | | 80 | 130 | ns |
| | | t _{THL} | V _{DD} = 5V | | 100 | 200 | ns |
| | | V _{DD} = 10V | | 50 | 100 | ns | |
| | | V _{DD} = 15V | | 40 | 80 | ns | |
| f _{CL} | Maximum Clock Frequency | V _{DD} = 5V | Measured with Respect to Carry Output Line | 1.0 | 2 | | MHz |
| | | V _{DD} = 10V | | 2.5 | 5 | | MHz |
| | | V _{DD} = 15V | | 3.0 | 6 | | MHz |
| t _{WL} , t _{WH} | Minimum Clock Pulse Width | V _{DD} = 5V | | 125 | 250 | ns | |
| | | V _{DD} = 10V | | 45 | 90 | ns | |
| | | V _{DD} = 15V | | 35 | 70 | ns | |
| t _{rCL} , t _{fCL} | Clock Rise and Fall Time | V _{DD} = 5V | | | 20 | μs | |
| | | V _{DD} = 10V | | | 15 | μs | |
| | | V _{DD} = 15V | | | 5 | μs | |
| t _{SU} | Minimum Clock Inhibit Data Setup Time | V _{DD} = 5V | | 120 | 240 | ns | |
| | | V _{DD} = 10V | | 40 | 80 | ns | |
| | | V _{DD} = 15V | | 32 | 65 | ns | |
| C _{IN} | Average Input Capacitance | | | 5 | 7.5 | pF | |
| Note 4: AC Parameters are guaranteed by DC correlated testing. | | | | | | | |
| AC Electrical Characteristics (Note 4) | | | | | | | |
| T _A = 25°C, C _L = 50 pF, R _L = 200k, t _{rCL} and t _{fCL} = 20 ns, unless otherwise specified | | | | | | | |
| Symbol | Parameter | Conditions | Min | Typ | Max | Units | |
| RESET OPERATION | | | | | | | |
| t _{PHL} , t _{PLH} | Propagation Delay Time Carry Out Line | V _{DD} = 5V | | 415 | 800 | ns | |
| | | V _{DD} = 10V | | 160 | 320 | ns | |
| | | V _{DD} = 15V | | 130 | 250 | ns | |
| | Carry Out Line | V _{DD} = 5V | C _L = 15 pF | 240 | 480 | ns | |
| | | V _{DD} = 10V | | 85 | 170 | ns | |
| | | V _{DD} = 15V | | 70 | 140 | ns | |
| Decode Out Lines | V _{DD} = 5V | | 500 | 1000 | ns | | |
| | V _{DD} = 10V | | 200 | 400 | ns | | |
| | V _{DD} = 15V | | 160 | 320 | ns | | |
| t _W | Minimum Reset Pulse Width | V _{DD} = 5V | | 200 | 400 | ns | |
| | | V _{DD} = 10V | | 70 | 140 | ns | |
| | | V _{DD} = 15V | | 55 | 110 | ns | |
| t _{REM} | Minimum Reset Removal Time | V _{DD} = 5V | | 75 | 150 | ns | |
| | | V _{DD} = 10V | | 30 | 60 | ns | |
| | | V _{DD} = 15V | | 25 | 50 | ns | |

Timing Diagrams

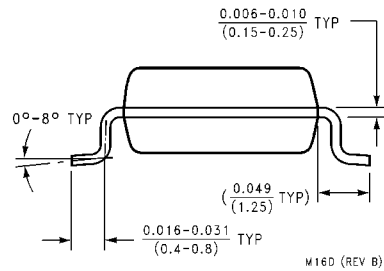
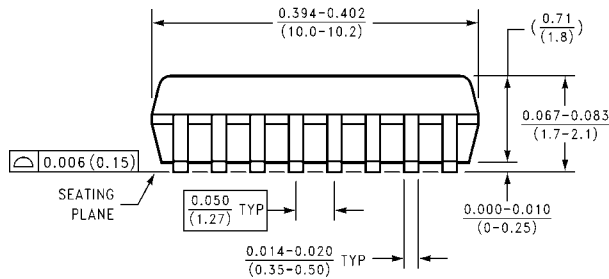
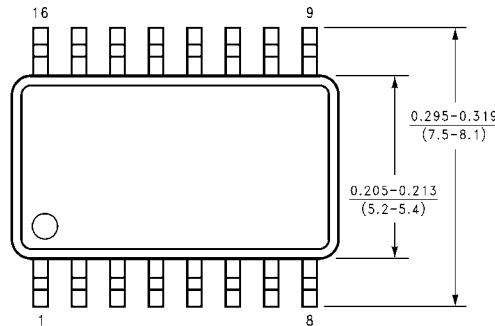


Physical Dimensions inches (millimeters) unless otherwise noted



M16A (REV H)

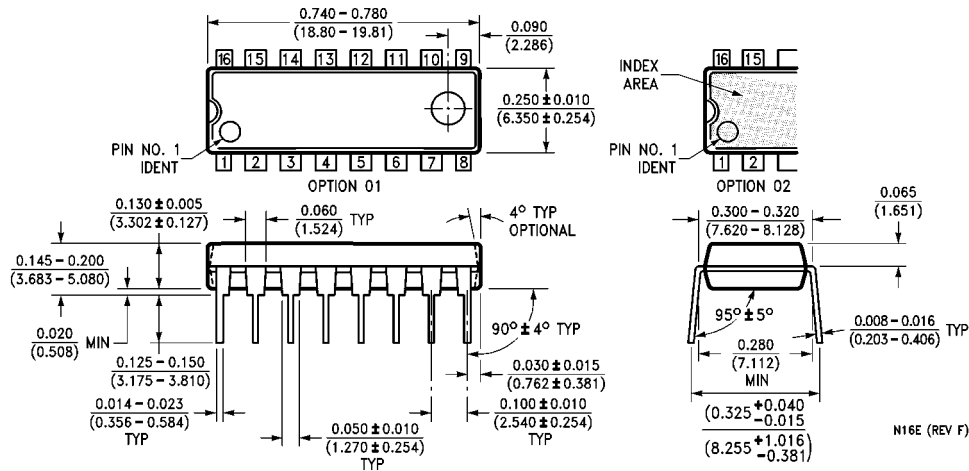
**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M16A**



M16D (REV B)

**16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-1, 0.300" Wide
Package Number N16E**

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