

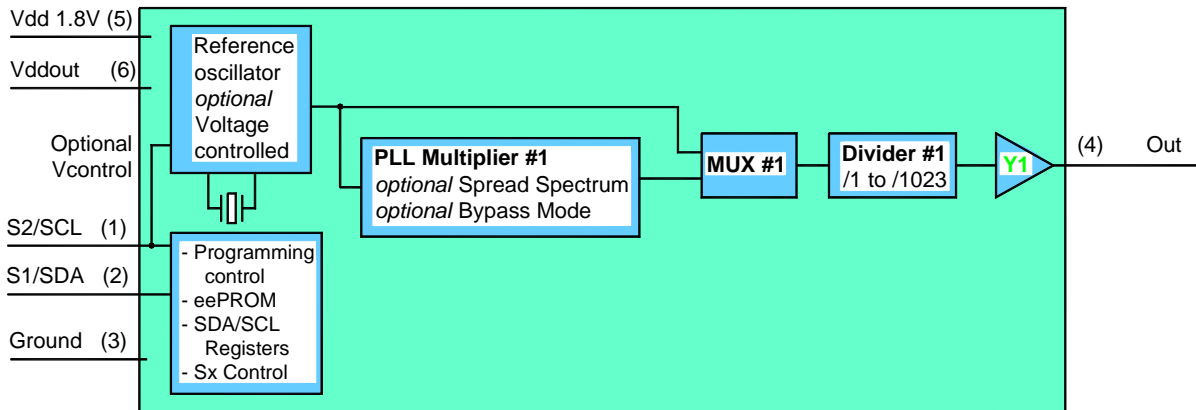
FD5T Series

FD51xxT-32.768KHz

CMOS Clock Oscillator

March 2009

- Pletronics' FD51T Series is a quartz crystal controlled precision square wave generator
- Output frequency 32.768KHz
- Selectable low jitter or spread spectrum output.
- Device characteristics may be either factory or field programmable
- Tape and Reel or cut tape packaging is available
- 3.2 x 5 mm LCC Ceramic Package
- Stability is much better than an XY cut watch crystal
- Very fast Start-up time, <10mS
- Low power
- 1.8V, 2.5 or 3.3V LVCMOS outputs
- Designed for high density SMD needs



Pletronics Inc. certifies this device is in accordance with the RoHS 6/6 (2002/95/EC) and WEEE (2002/96/EC) directives.

Pletronics Inc. guarantees the device does not contain the following:
 Cadmium, Hexavalent Chromium, Lead, Mercury, PBB's, PBDE's
 Weight of the Device: 0.09 grams
 Moisture Sensitivity Level: 1 As defined in J-STD-020C
 Second Level Interconnect code: e4

Absolute Maximum Ratings:

| Parameter | Unit |
|--------------------------------------|-----------------------------|
| V_{DD} | -0.5V to +2.5V |
| V_{DDOUT} | -0.5V to +4.6V |
| V_i Input Voltage | -0.5V to $V_{DD} + 0.5V$ |
| V_o Output Voltage | -0.5V to $V_{DDOUT} + 0.5V$ |
| I_o Continuous Output Current | ± 50 mA |
| T_j Maximum Junction Temperature | 125°C |
| Thermal Resistance, Junction to Case | 50°C/Watt |

Description:

The FD51xxT-32.768K is derived from the PLE FD51T series Programmable CMOS Clock Oscillator which is a modular PLL-based low cost, high-performance oscillator. The frequency output is set to 32.768KHz. The FD51xxT-32.768K base frequency is a 24.576MHz AT cut fundamental mode crystal.

The FD51T has a separate output supply pin, V_{DDOUT} , for either 1.8, 2.5 or 3.3V output logic levels. The device supply, V_{DD} which provides power to all the internal circuits, is nominally 1.8V.

The PLL is only utilized to support Spread Spectrum Clocking (SSC), in all other cases the PLL is disabled to reduce power. SSC may be programmed to be either center-spread or down-spread. This is an important technique to reduce electro-magnetic interference (EMI).

The device supports non-volatile eePROM programming for easy customization of the device. As shipped, the device is pre-programmed. However, the FD51xxT-32.768K may be reprogrammed to a different configuration. Reprogramming may be either prior to assembly, or in-circuit via a 2-wire SDA/SCL I²C bus. In-circuit programming is not allowed if the VCXO function is needed.

Two programmable control inputs, S1 and S2, may be used to control various aspects of FD51xxT-32.768K operation including selection of alternative frequency set(s), selection of SSC functionality, output tri-state and power-down.

Reference Oscillator

The VCXO input has a limited voltage range, the VCXO is associated with the internal 1.8V core. A resistor in series with the Vcontrol input will permit interfacing to 3.3V analog circuits, the voltage range that changes the frequency will still be limited but the larger voltages swings will not cause problems.

The VCXO function is only enabled (internally connected) if the part number indicates a VCXO specification. When the VCXO function is enabled the I²C programming mode will be disabled.

PLL Multiplier

The PLL Multiplier is enabled when tight tolerances are needed or when the spread spectrum function is needed.

Spread Spectrum

The PLL has its individual Spread Spectrum (SS) function that can be enabled. This permits the modulation of the output frequency by a user-set amount.

Divider Section

The dividers operate on the output of the PLL. The divider on the PLL can divide by 1 through 1023 and is set to 750 in this case. There is only 1 setting allowed per divider. These are not set by the Sx input state.

The dividers add very little jitter to the output signals.

Multiplexers

MUX #1 selects the input to the Divider #1, this can be the reference oscillator signal or the output from

PLL Multiplier #1.

The device can make only one of the setting of connections shown in the block diagram (only one pattern stored in eePROM).

Control Inputs

The two inputs, S1/SDA and S2/SCL can be configured in two ways.

- 1) Used as 2 user inputs to permit up to 4 states, Sx input setting.
- 2) The SDA and SCL become clock and data inputs to write to the FD5T internal setting memory. The interface follows the I²C protocol. If the SDA and SCL are not set then the internal eePROM sets the operation. (Not allowed if the VCXO function is specified.)

Standard Configuration

| S1 | S2 | Output | SS | PLL |
|------|------|-----------|--------------|---------|
| Low | Low | Tri State | --- | Disable |
| High | Low | 32.768KHz | ±1% centered | Enable |
| Low | High | 32.768KHz | ±2% centered | Enable |
| High | High | 32.768KHz | none | Disable |

PART NUMBER:

FD5 1 45 T L E -32.768K -YYY

| | |
|--|--|
| | Packaging code or blank T250 = 250 per Tape and Reel T500 = 500 per Tape and Reel T1K = 1000 per Tape and Reel |
| | Output Frequency - 32.768KHz |
| | Optional Enhanced Operating temperature Range Blank = Temp. range -20°C to +70°C E = Temp. range -40°C to +85°C |
| | Blank = V _{DDOUT} 3.3V, 2.5V and 1.8V device L = V _{DDOUT} 1.8V only - high output drive level device |
| | Series Model |
| | Frequency Stability for fixed frequency oscillator 45 = ± 50 ppm 15 = ± 15 ppm ¹ 44 = ± 25 ppm 10 = ± 10 ppm ¹ 20 = ± 20 ppm |
| | Frequency Pull Ability for VCXO option enabled 99 = ± 100 ppm Absolute Pull Range (APR) 75 = ± 25 ppm Absolute Pull Range (APR) 50 = ± 50 ppm Absolute Pull Range (APR) |
| | 1 = 1 output 1 PLL version |
| | Series Model |

¹In these cases the PLL will be enabled and the power dissipation will be higher.

Part Marking:

PLE FD51 Marking Legend: PLE = Pletronics
32.768K YMD = Date of Manufacture (year-month-day)
YMD All other marking is internal factory codes

Codes for Date Code YMD

| Code | 8 | 9 | 0 | 1 | 2 | Code | A | B | C | D | E | F | G | H | J | K | L | M |
|------|------|------|------|------|------|-------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Year | 2008 | 2009 | 2010 | 2011 | 2012 | Month | JAN | FEB | MAR | APR | MAY | JUN | JUL | AUG | SEP | OCT | NOV | DEC |

| Code | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F | G |
|------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Day | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
| Code | H | J | K | L | M | N | P | R | T | U | V | W | X | Y | Z | |
| Day | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | |

Electrical Specification over the specified temperature range.

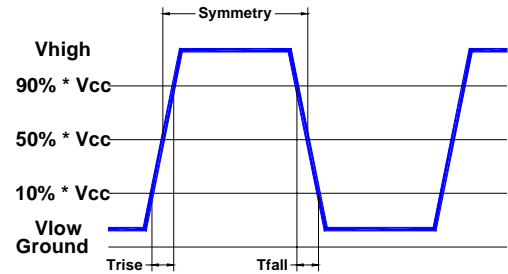
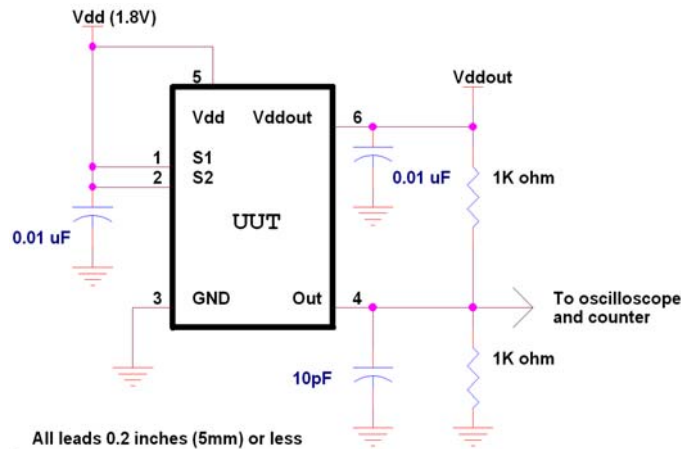
| Item | Min | Max | Unit | Condition | |
|---|------|-----|---------|--|--|
| Frequency Accuracy | "45" | -50 | +50 | ppm | For all supply voltages, load changes, aging for 1 year, shock, vibration and temperatures |
| | "44" | -25 | +25 | | |
| | "20" | -20 | +20 | | |
| | "15" | -15 | +15 | | |
| | "10" | -10 | +10 | | |
| Start-up Time | -- | 10 | mS | | |
| Recommended Operating Conditions | | | | | |
| Device Supply Voltage V_{DD} | 1.7 | 1.9 | V | | |
| Output Supply Voltage V_{DDOUT} | 1.7 | 3.6 | V | | |
| Output Supply Voltage "L" V_{DDOUT} | 1.7 | 1.9 | V | | |
| Low Level Input voltage | -- | 30 | % | of V_{DD} | |
| High Level Input voltage | 70 | -- | % | of V_{DD} | |
| Input Voltage Range, S1, S2 | 0 | 3.6 | V | V_{TH} is $0.5 * V_{DD}$ | |
| Input current for: S1, S2 | 0 | 5 | μA | $V_{IN} = V_{DD}; V_{DD} = 1.9V$ | |
| | -4 | 0 | μA | $V_{IN} = 0.0V_D; V_{DD} = 1.9V$ | |
| Output Current, $V_{DDOUT} = 3.3V$ | -12 | +12 | mA | | |
| Output Current, $V_{DDOUT} = 2.5V$ | -10 | +10 | mA | | |
| Output Current, $V_{DDOUT} = 1.8V$ | -5 | +5 | mA | | |
| Output Current "L", $V_{DDOUT} = 1.8V$ | -8 | +8 | mA | | |
| Output Load, LVCMOS | -- | 10 | pf | Higher loads can be used | |
| LVCMOS Output Parameters for $V_{DDOUT} = 3.3v$ | | | | | |
| Output High, $V_{DDOUT} = 3.3V$ | 2.9 | -- | V | $I_{OH} = -0.1 mA$ | |
| | 2.4 | -- | V | $I_{OH} = -8.0 mA$ | |
| | 2.2 | -- | V | $I_{OH} = -12.0 mA$ | |
| Output Low, $V_{DDOUT} = 3.3V$ | -- | 0.1 | V | $I_{OH} = +0.1 mA$ | |
| | -- | 0.5 | V | $I_{OH} = +8.0 mA$ | |
| | -- | 0.8 | V | $I_{OH} = +12.0 mA$ | |
| Rise & Fall Time | -- | 0.6 | nS | $V_{DDOUT} = 3.3v, 20 - 80\%, 10pF Load$ | |
| I_{DD} (no PLL enabled) | -- | 2.5 | mA | | |
| I_{DD} (PLL enabled) | -- | 9 | mA | SS option or 15ppm or 10 ppm stability | |
| I_{DDOUT} | -- | 5 | μA | 10pF Load | |
| Output Symmetry | 45 | 55 | % | at 50% point of V_{DDOUT} | |
| Peak-to-Peak Jitter ⁽¹⁾ | -- | 10 | pS | (No SS and PLL disabled) | |

| Item | Min | Max | Unit | Condition |
|--|-----|-----|------|--|
| LVC MOS Output Parameters for $V_{DDOUT} = 2.5V$ | | | | |
| Output High, $V_{DDOUT} = 2.5V$ | 2.2 | -- | V | $I_{OH} = -0.1$ mA |
| | 1.7 | -- | V | $I_{OH} = -6.0$ mA |
| | 1.6 | -- | V | $I_{OH} = -10.0$ mA |
| Output Low, $V_{DDOUT} = 2.5V$ | -- | 0.1 | V | $I_{OH} = +0.1$ mA |
| | -- | 0.5 | V | $I_{OH} = +6.0$ mA |
| | -- | 0.7 | V | $I_{OH} = +10.0$ mA |
| Rise & Fall Time | -- | 0.6 | nS | $V_{DDOUT} = 2.5V$, 20 - 80%, 10pF Load |
| Output Symmetry | 45 | 55 | % | at 50% point of V_{DDOUT} |
| I_{DD} (no PLL enabled) | -- | 2.5 | mA | |
| I_{DD} (PLL enabled) | -- | 9 | mA | SS option or 15ppm or 10 ppm stability |
| I_{DDOUT} | -- | 4 | uA | 10pF Load |
| Peak-to-Peak Jitter ⁽¹⁾ | -- | 10 | pS | (No SS and PLL disabled) |
| LVC MOS Output Parameters for $V_{DDOUT} = 1.8V$ | | | | |
| Output High, $V_{DDOUT} = 1.8V$ | 1.6 | -- | V | $I_{OH} = -0.1$ mA |
| | 1.4 | -- | V | $I_{OH} = -3.0$ mA |
| | 1.1 | -- | V | $I_{OH} = -6.0$ mA |
| Output Low, $V_{DDOUT} = 1.8V$ | -- | 0.1 | V | $I_{OH} = +0.1$ mA |
| | -- | 0.3 | V | $I_{OH} = +3.0$ mA |
| | -- | 0.6 | V | $I_{OH} = +6.0$ mA |
| Rise & Fall Time | -- | 0.9 | nS | $V_{DDOUT} = 1.8V$, 20 - 80%, 10pF Load |
| Output Symmetry | 45 | 55 | % | at 50% point of V_{DDOUT} |
| I_{DD} (no PLL enabled) | -- | 2.5 | mA | |
| I_{DD} (PLL enabled) | -- | 9 | mA | SS option or 15ppm or 10 ppm stability |
| I_{DDOUT} | -- | 2.5 | uA | 10pF Load |
| Peak-to-Peak Jitter ⁽¹⁾ | -- | 10 | pS | (No SS and PLL disabled) |
| LVC MOS Output Parameters for $V_{DDOUT} = 1.8V$ "L" Version | | | | |
| Output High, $V_{DDOUT} = 1.8V$ | 1.6 | -- | V | $I_{OH} = -0.1$ mA |
| | 1.4 | -- | V | $I_{OH} = -4.0$ mA |
| | 1.1 | -- | V | $I_{OH} = -8.0$ mA |
| Output Low, $V_{DDOUT} = 1.8V$ | -- | 0.1 | V | $I_{OH} = +0.1$ mA |
| | -- | 0.3 | V | $I_{OH} = +4.0$ mA |
| | -- | 0.6 | V | $I_{OH} = +8.0$ mA |
| Rise & Fall Time | | 0.7 | nS | $V_{DDOUT} = 1.8V$, 20 - 80%, 10pF Load |

| Item | Min | Max | Unit | Condition |
|--|-------------|-----------------|------|--|
| Output Symmetry | 45 | 55 | % | at 50% point of V_{DDOUT} |
| I_{DD} (no PLL enabled) | -- | 2.5 | mA | |
| I_{DD} (PLL enabled) | -- | 9 | mA | SS option or 15ppm or 10 ppm stability |
| I_{DDOUT} | -- | 3 | uA | 10pF Load |
| Peak-to-Peak Jitter ⁽¹⁾ | -- | 10 | pS | (No SS and PLL disabled) |
| VCXO Function | | | | |
| Vcontrol Input Range Usable | 0.5 | $V_{DD} - 0.5V$ | V | The slope is positive |
| Vcontrol Input Range Allowed - Direct connect to Vcontrol - Limit current to $\pm 3mA$ | 0.0 -1.0 | V_{DD} 4.0 | V | The slope is positive Recommend $\geq 1K$ ohm to Vcontrol |
| Pull Ability specified in the P.N. | -- | -- | | |
| Linearity | -10 | +10 | % | |

(1) 10,000 cycles

Load Circuit and Test Waveform



Reliability: Environmental Compliance

| Parameter | Condition |
|------------------|--------------------------------------|
| Mechanical Shock | MIL-STD-883 Method 2002, Condition B |
| Vibration | MIL-STD-883 Method 2007, Condition A |
| Solderability | MIL-STD-883 Method 2003 |
| Thermal Shock | MIL-STD-883 Method 1011, Condition A |

ESD Rating

| Model | Minimum Voltage | Conditions |
|----------------------|-----------------|-------------------------|
| Human Body Model | 1500 | MIL-STD-883 Method 3115 |
| Charged Device Model | 1000 | JESD 22-C101 |

Package Labeling

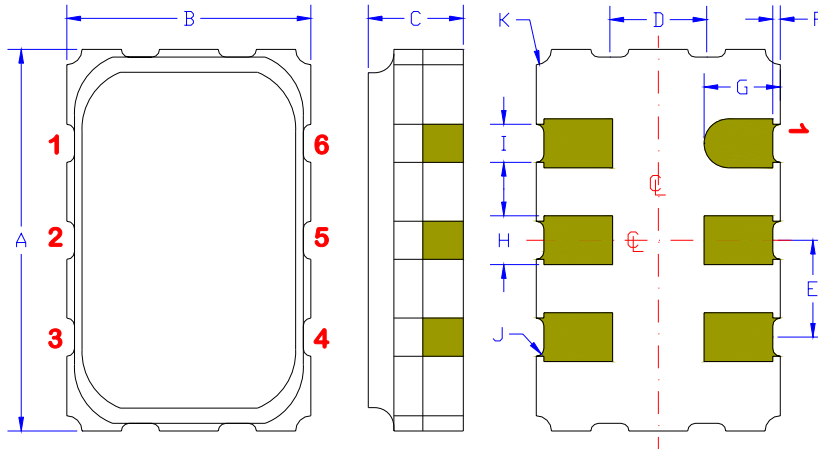
Label is 1" x 2.6" (25.4mm x 66.7mm)
Font is Courier New
Bar code is 39-Full ASCII
(Label will show FD51xxT-32.768K)

Label is 1" x 2.6" (25.4mm x 66.7mm)
Font is Arial

| | |
|---------------|-----|
| P/N: | |
| Customer P/N: | |
| Qty: | D/C |

| |
|-----------------------------------|
| RoHS Compliant |
| 2nd LVL Interconnect |
| Category=e4 |
| Max Safe Temp=260C for 10s 2X Max |

Mechanical:



Contacts:
Gold 11.8 μ mches 0.3 μ m minimum over
Nickel 50 to 350 μ mches 1.27 to 8.89 μ m

¹ Typical dimensions

Not to Scale

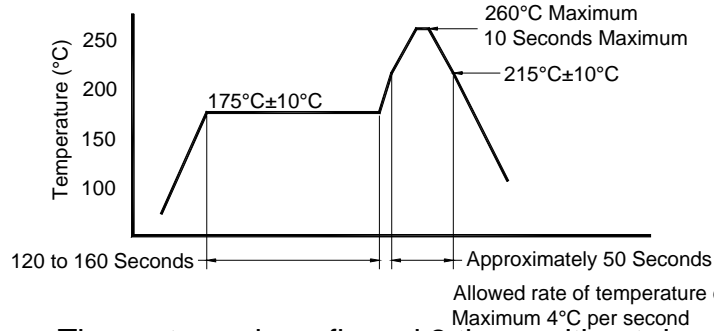
| | Inches | mm |
|----------------|-------------------|-----------------|
| A | 0.197 \pm 0.006 | 5.00 \pm 0.15 |
| B | 0.125 \pm 0.006 | 3.20 \pm 0.15 |
| C | 0.053 max | 1.35 max |
| D ¹ | 0.050 | 1.27 |
| E ¹ | 0.050 | 1.27 |
| F ¹ | 0.004 | 0.10 |
| G ¹ | 0.039 | 1.00 |
| H ¹ | 0.025 | 0.63 |
| I ¹ | 0.020 | 0.50 |
| J ¹ | 0.004R | 0.10R |
| K ¹ | 0.008R | 0.20R |

Pad Functions:

| Pad | Function | Note |
|-----|--------------------|---|
| 1 | S1/SDA | Serial Data Clock (optional V control - VCXO) |
| 2 | S2/SCL | Serial Data |
| 3 | Ground (GND) | |
| 4 | Out (Y3) | Crystal reference frequency divided by 1 through 1023 PLL1 frequency divided by 1 through 1023 |
| 5 | V _{DD} | 1.8V, powers internal circuitry of the oscillator. Bypass capacitor required near the package pin. |
| 6 | V _{DDOUT} | 1.8V, 2.5V or 3.3V supply for the output buffers. Sets CMOS output level. Bypass capacitor required near the package pin. |

All unused inputs should be pulled high.

Reflow Cycle (typical for lead free-processing)



The part may be reflowed 2 times without degradation.

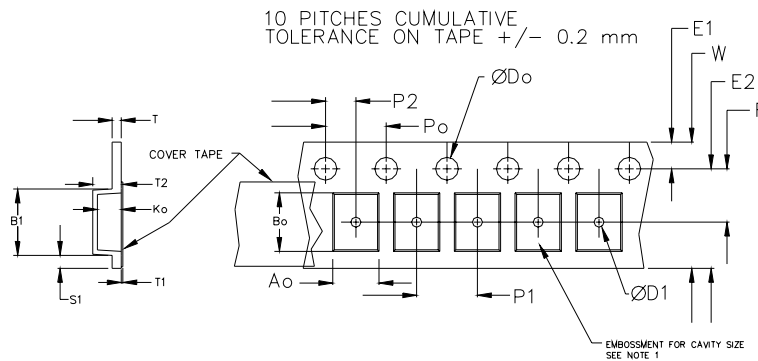
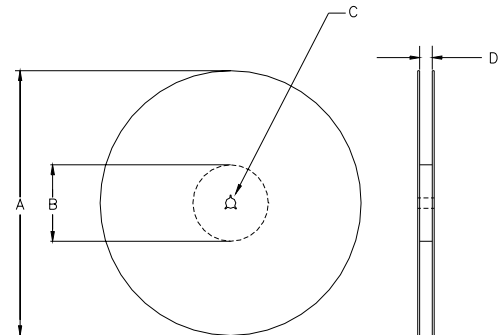
Tape and Reel: available for quantities of 250 to 1000 per reel, cut tape for < 250

| Constant Dimensions Table 1 | | | | | | | | |
|-----------------------------|-----|-----------|------------|-----------|------------|--------|-------|--------|
| Tape Size | D0 | D1 Min | E1 | P0 | P2 | S1 Min | T Max | T1 Max |
| 8mm | 1.5 | 1.0 | 1.75 ± 0.1 | 4.0 ± 0.1 | 2.0 ± 0.05 | 0.6 | 0.6 | 0.1 |
| 12mm | | 1.5 | | | 2.0 ± 0.1 | | | |
| 16mm | | +0.1 -0.0 | | | 1.5 | | | |
| 24mm | | 1.5 | | | 1.5 | | | |

| Variable Dimensions Table 2 | | | | | | | |
|-----------------------------|--------|--------|-----------|-----------|--------|-------|-------------|
| Tape Size | B1 Max | E2 Min | F | P1 | T2 Max | W Max | Ao, Bo & Ko |
| 16 mm | 12.1 | 14.25 | 7.5 ± 0.1 | 8.0 ± 0.1 | 8.0 | 16.3 | Note 1 |

Note 1: Embossed cavity to conform to EIA-481-B

Not to scale



| | | REEL DIMENSIONS | | | |
|---|--------|------------------|----------------|----------------|------------|
| A | inches | 7.0 | 10.0 | 13.0 | Tape Width |
| | mm | 177.8 | 254.0 | 330.2 | |
| B | inches | 2.50 | 4.00 | 3.75 | Tape Width |
| | mm | 63.5 | 101.6 | 95.3 | |
| C | mm | 13.0 +0.5 / -0.2 | | | Tape Width |
| D | mm | 16.4 +2.0 -0.0 | 16.4 +2.0 -0.0 | 16.4 +2.0 -0.0 | |

USER DIRECTION OF UNREELING →

Reel dimensions may vary from the above

IMPORTANT NOTICE

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