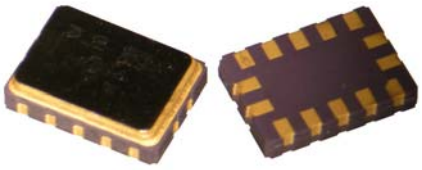
PLETRONICS
www.pletronics.com 425-776-1880



# FD7T Series
## Multi-Output CMOS Clock Oscillator

May 2008

- Pletronics' FD7T Series is a quartz crystal controlled precision square wave generator with multiple independent CMOS outputs
- Output frequencies from 12 KHz to 230 MHZ
- Selectable low jitter or spread spectrum outputs.
- Device characteristics may be either factory or field programmable
- 1.8V, 2.5 or 3.3V LVCMOS outputs
- 5 x 7 mm LCC Ceramic Package
- Low power
- This is a low cost, mass produced oscillator.
- Tape and Reel or cut tape packaging is available.
- The package is designed for high density surface mount designs

| Model Number | PLLs | Outputs |
|---|---|---|
| FD77xxT | 4 | 7 |
| FD75xxT | 3 | 5 |
| FD74xxT | 2 | 4 |
| FD73xxT | 1 | 3 |

**Pletronics Inc. certifies this device is in accordance with the RoHS 6/6 (2002/95/EC) and WEEE (2002/96/EC) directives.**

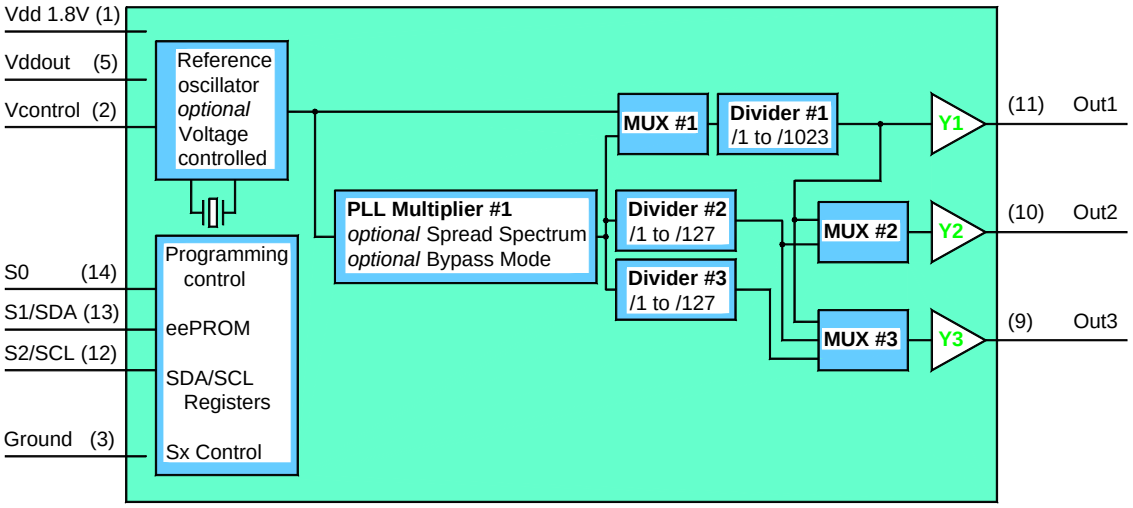
Pletronics Inc. guarantees the device does not contain the following:
Cadmium, Hexavalent Chromium, Lead, Mercury, PBB's, PBDE's
Weight of the Device: 0.17 grams
Moisture Sensitivity Level: 1 As defined in J-STD-020C
Second Level Interconnect code: e4

### Absolute Maximum Ratings:

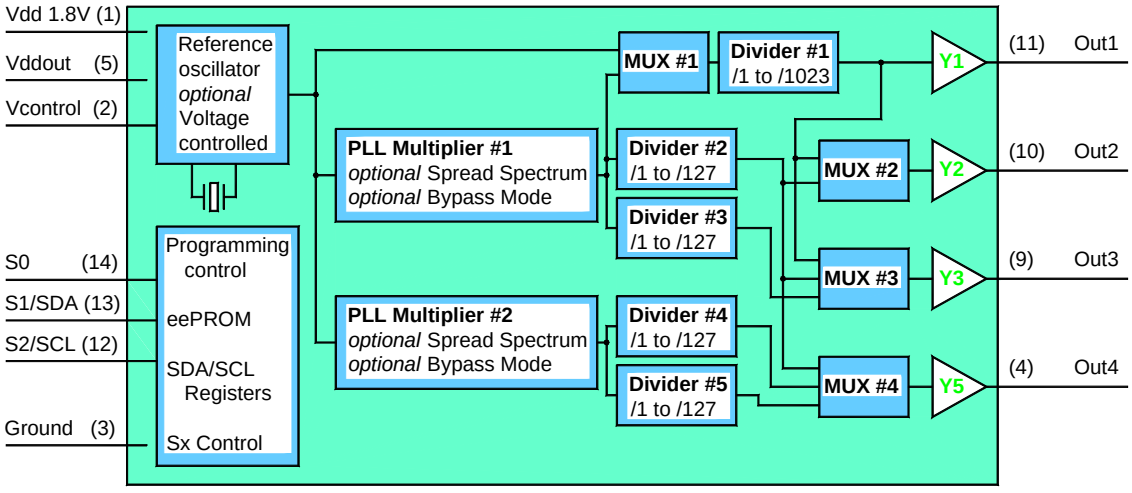
| Parameter | Unit |
|---|---|
| $V_{DD}$ | -0.5V to +2.5V |
| $V_{DDOUT}$ | -0.5V to +4.6V |
| Vi Input Voltage | -0.5V to $V_{DD}$+ 0.5V |
| Vo Output Voltage | -0.5V to $V_{DDOUT}$ + 0.5V |
| Io Continuous Output Current | $\pm$ 50 mA |
| Tj Maximum Junction Temperature | 125°C |
| Thermal Resistance, Junction to Case | 50°C/Watt |

## BLOCK DIAGRAMS OF THE FD7T SERIES

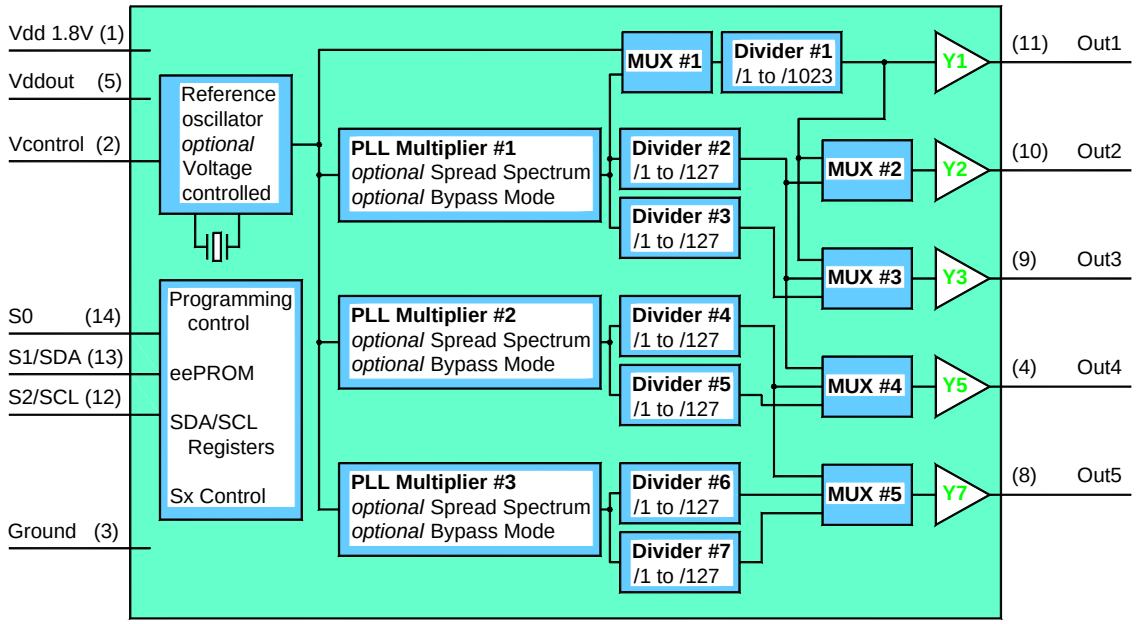
### FD73xxT



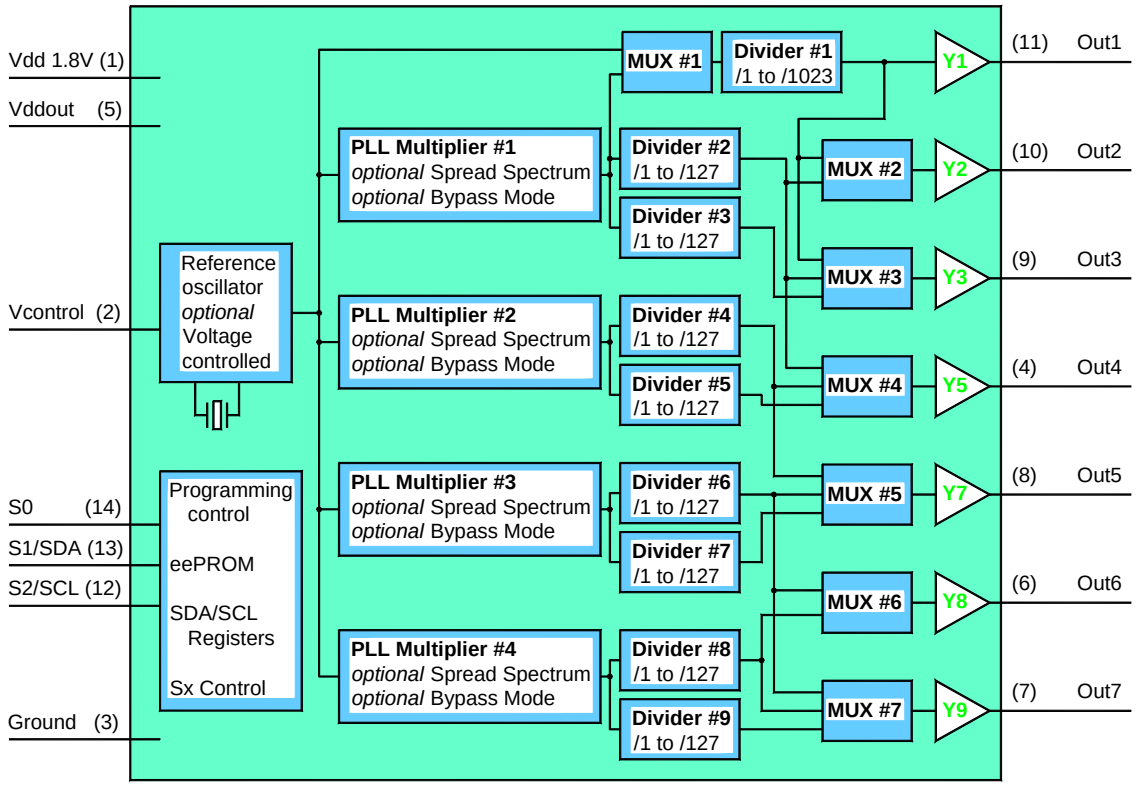

### FD74xxT



## FD75xxT




## FD77xxT



## Description:

The FD7T series Multi-Output CMOS Clock Oscillator is a modular PLL-based low cost, high-performance, programmable oscillator. The FD7T generates up to seven output frequencies, OUT1 through OUT7. Frequencies are mutually independent and may be programmed to any frequency from 100KHz to 230-MHZ and one output can be as low as 12KHz. There are versions including 1 to 4 PLLs, the number of PLLs impacts the cost.

The FD7T base frequency, as noted in the device part number, is established during manufacture and is permanently fixed. For convenience, the divider for output OUT1 and the remaining seven output frequencies, and their characteristics may be pre-programmed at the factory, or field programmed.

The FD7T has a separate output supply pin, $V_{DDOUT}$, for either 1.8, 2.5 or 3.3V output logic levels. The device supply, $V_{DD}$ which provides power to all the internal circuits, is nominally 1.8V.

The FD7xxxTL version has increased output drive for then 1.8V output levels. This version can be used at 1.8V $V_{DDOUT}$ only.

The deep M/N PLL divider ratio allows the generation of zero-ppm clocks for applications such as WLAN, BlueTooth, Ethernet, GPS, USB, IEEE1394, etc. from the base frequency.

Each of the independent PLLs supports Spread Spectrum Clocking (SSC). SSC may be programmed to be either center-spread or down-spread. This is an important technique to reduce electro-magnetic interference (EMI).

The device supports non-volatile eePROM programming for easy customization of the device. As shipped, the device is pre-programmed. Standard combinations are denoted by three characters in the device part number. However, the FD7T may be reprogrammed to a different configuration. Reprogramming may be either prior to assembly, or in-circuit via a 2-wire SDA/SCL $I^2C$ bus.

Three programmable control inputs, S0, S1 and S2, may be used to control various aspects of FD7T operation including selection of alternative frequency set(s), selection of SSC functionality, output tri-state and power-down.

### Reference Oscillator

The Reference Oscillator is an AT cut quartz crystal based oscillator. This oscillator is very similar to the Pletronics SM77xxH product oscillator. This signal is the lowest jitter and can be an output on Out1, Out2 or Out3 and can be divided down by the Divider #1. The user may specify any frequency between 12MHz and 32MHz for this reference. All output frequencies are derived from (referenced to) this Reference Oscillator.

### Reference Oscillator - VCXO

The reference oscillator frequency can be modulated by the Vcontrol input, if the VCXO option is selected. As this Reference Signal is the reference for all other parts of this circuit, all PLLs will be modulated also.

The VCXO input has a limited voltage range, the VCXO is associated with the internal 1.8V core. A resistor in series with the Vcontrol input will permit interfacing to 3.3V analog circuits, the voltage range that changes the frequency will still be limited but the larger voltages swings will not cause problems.

### PLL Multipliers

There are up to 4 each independent PLL Multipliers and these can multiply the Reference Oscillator frequency from 1 (bypass mode) to any value that is <=230MHz (the lowest frequency is the Reference Oscillator frequency).

Each of the PLL Multipliers can have two setup options, 0 or 1, depending on which option is chosen and set by the Sx control signals and the user's definitions are stored in eePROM.

### Spread Spectrum

Each PLL has its individual Spread Spectrum (SS) function that can be enabled. This permits the modulation of the output frequency by a user-set amount. The modulation can be centered on the output frequency or down side only. Which of the 1 of 8 SS settings is being used is set by the Sx input and the user definition. The value is a percentage of the output frequency that will be modulated.

| SS Option | Down Side Modulation | Centered Modulation |
|---|---|---|
| 0 | No SS | No SS |
| 1 | -0.25% | ±0.25% |
| 2 | -0.50% | ±0.50% |
| 3 | -0.75% | ±0.75% |
| 4 | -1.00% | ±1.00% |
| 5 | -1.25% | ±1.25% |
| 6 | -1.50% | ±1.50% |
| 7 | -2.00% | ±2.00% |

### Divider Section

The dividers operate on the output of the PLLs. There are two dividers on each PLL that divide by 1 through 127, the value is user defined. There is only 1 setting allowed per divider. These are not set by the Sx input state.

The dividers add very little jitter to the output signals.

### Multiplexers

MUX #1 selects the input to the Divider #1, this can be the reference oscillator signal or the output from PLL Multiplier #1. MUX #2 through MUX #7 connect various divider outputs to the output buffers.

The device can make only one of the setting of connections shown in the block diagram (only one pattern stored in eePROM).

### Output Buffers

Each output buffer can have 3 modes of operation:
1) Tri State 2) Active Low 3) The signal output of the Multiplexer
The output buffers for Out2 and Out3 and the output buffers Out6 and Out7 function as pairs. When selecting on the function both outputs in the pair function the same.

There can be two options stored for the Output Buffers, State 0 and State 1. The eight Sx input settings can have assigned one of the two Output Buffer states for each of Output Buffer sets.

This permits wired 'OR' of tri-state outputs, this permits setting total enable and disable functions of all outputs.

### Control Inputs

The three inputs, S0, S1/SDA and S2/SCL can be configured in two ways.
1) Used as 3 user inputs to permit up to 8 states, Sx input setting.
2) S0 used as an input to permit up to 2 states, S0 input setting. The SDA and SCL become clock and data inputs to write to the FD7T internal setting memory. The interface follows the $I^2C$ protocol. If the SDA and SCL are not set then the internal eePROM sets the operation.

The S0, S1 and S2 input signals control and variations states allowed:

| Inputs | | | PLL #1 | | PLL #2 | | PLL #3 | | PLL #4 | | Output | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| S2 | S1 | S0 | SS | PLL | SS | PLL | SS | PLL | SS | PLL | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 0 | 0 | 0 | 0/7 | 0/1 | 0/7 | 0/1 | 0/7 | 0/1 | 0/7 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 |
| 0 | 0 | 1 | 0/7 | 0/1 | 0/7 | 0/1 | 0/7 | 0/1 | 0/7 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 |
| 0 | 1 | 0 | 0/7 | 0/1 | 0/7 | 0/1 | 0/7 | 0/1 | 0/7 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 |
| 0 | 1 | 1 | 0/7 | 0/1 | 0/7 | 0/1 | 0/7 | 0/1 | 0/7 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 |
| 1 | 0 | 0 | 0/7 | 0/1 | 0/7 | 0/1 | 0/7 | 0/1 | 0/7 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 |
| 1 | 0 | 1 | 0/7 | 0/1 | 0/7 | 0/1 | 0/7 | 0/1 | 0/7 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 |
| 1 | 1 | 0 | 0/7 | 0/1 | 0/7 | 0/1 | 0/7 | 0/1 | 0/7 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 |
| 1 | 1 | 1 | 0/7 | 0/1 | 0/7 | 0/1 | 0/7 | 0/1 | 0/7 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 | 0/1 |

The MUX inputs are fixed independent of the Sx setting.
The Divider Values are fixed independent of the Sx setting

### Specifying The FD7T Device For A Specific Application

Pletronics provides an EXCEL spreadsheet based program that assists in defining the FD77T functions. The program only permits setting of parameters that will properly function. After defining the desired functions, this spreadsheet is sent to Pletronics and the Configuration Part Number will then be assigned. Pletronics uses the values in the spreadsheet to program the devices for shipment.

## PART NUMBER:

| FD7 | 7 | 45 | T | L | E | -25.0M | -YYY | -XX | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | Packaging code or blank<br>T250 = 250 per Tape and Reel<br>T500 = 500 per Tape and Reel<br>T1K = 1000 per Tape and Reel |
| | | | | | | | | | **Configuration Number**<br>This is a 3 character alpha-numeric code issued by Pletronics that defines the FD77T function (the output pin functions, the available frequencies and the pin number assignments). Each configuration is given a unique value. |
| | | | | | | | | | **Base Frequency (Crystal oscillator frequency) in MHZ** |
| | | | | | | | | | **Optional Enhanced Operating temperature Range**<br>Blank = Temp. range -20°C to +70°C<br>**E** = Temp. range -40°C to +85°C |
| | | | | | | | | | Blank = $V_{DDOUT}$ 3.3V, 2.5V and 1.8V device<br>**L** = $V_{DDOUT}$ 1.8V only high output drive level device |
| | | | | | | | | | **Series Model** |
| | | | | | | | | | **Frequency Stability for fixed frequency oscillator**<br>**45** = ± 50 ppm **15** = ± 15 ppm<br>**44** = ± 25 ppm **10** = ± 10 ppm<br>**20** = ± 20 ppm<br>**Frequency Pull Ability for VCXO option enabled**<br>**99** = ± 100 ppm Absolute Pull Range (APR)<br>**75** = ± 25 ppm Absolute Pull Range (APR)<br>**50** = ± 50 ppm Absolute Pull Range (APR) |
| | | | | | | | | | **7** = 7 outputs 4 PLL version<br>**5** = 5 outputs 3 PLL version<br>**4** = 4 outputs 2 PLL version<br>**3** = 3 outputs 1 PLL version |
| | | | | | | | | | **Series Model** |

## Part Marking:

**PLE FD7x**
**ZZZ**
**YMD**

Marking Legend: PLE = Pletronics; *ZZZ* = configuration; *X* = Model type; *YMD* = Date of Manufacture (year-month-day)

All other marking is internal factory codes

Codes for Date Code YMD

| Code | 8 | 9 | 0 | 1 | 2 | Code | A | B | C | D | E | F | G | H | J | K | L | M |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Year | 2008 | 2009 | 2010 | 2011 | 2012 | Month | JAN | FEB | MAR | APR | MAY | JUN | JUL | AUG | SEP | OCT | NOV | DEC |

| Code | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F | G |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Day | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
| Code | H | J | K | L | M | N | P | R | T | U | V | W | X | Y | Z | |
| Day | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | |

## Electrical Specification over the specified temperature range

| Item | Min | Max | Unit | Condition |
|---|---|---|---|---|
| Base Frequency | 12 | 32 | MHZ | |
| Frequency Range OUT1 | 0.0117 | 230 | MHZ | Base Frequency / (1 to 1023) -or- PLL1 |
| Frequency Range OUT2 - 7 | 0.0945 | 230 | MHZ | |
| Frequency Accuracy "**45**" | -50 | +50 | ppm | For all supply voltages, load changes, aging for 1 year, shock, vibration and temperatures |
| "**44**" | -25 | +25 | | |
| "**20**" | -20 | +20 | | |
| **Recommended Operating Conditions** | | | | |
| Device Supply Voltage $V_{DD}$ | 1.7 | 1.9 | V | |
| Output Supply Voltage $V_{DDOUT}$ | 1.7 | 3.6 | V | |
| Output Supply Voltage "L" $V_{DDOUT}$ | 1.7 | 1.9 | V | |
| Low Level Input voltage | -- | 30 | % | of $V_{DD}$ |
| High Level Input voltage | 70 | -- | % | of $V_{DD}$ |
| Input Voltage Range, S0<br>If 1K ohm in series with S0 pad | 0<br>-1 | 1.9<br>4.0 | V | $V_{TH}$ is 0.5 * $V_{DD}$ |
| Input Voltage Range, S1, S2 | 0 | 3.6 | V | $V_{TH}$ is 0.5 * $V_{DD}$ |
| Input current for:<br>S0 with 1K ohm in series | 0 | 3 | mA | $V_{IN}$ = 4V; $V_{DD}$ = 1.8V |
| S0, S1, S2 | 0 | 5 | µA | $V_{IN}$ = $V_{DD}$; $V_{DD}$ = 1.9V |
| | -4 | 0 | µA | $V_{IN}$ = 0.0$V_D$; $V_{DD}$ = 1.9V |
| Output Current, $V_{DDOUT}$ = 3.3V | -12 | +12 | mA | |
| Output Current, $V_{DDOUT}$ = 2.5V | -10 | +10 | mA | |
| Output Current, $V_{DDOUT}$ = 1.8V | -5 | +5 | mA | |
| Output Current "L", $V_{DDOUT}$ = 1.8V | -8 | +8 | mA | |
| Output Load, LVCMOS | -- | 10 | pf | Higher loads can be used |
| **LVCMOS Output Parameters for $V_{DDOUT}$ = 3.3v** | | | | |
| Output High, $V_{DDOUT}$ = 3.3V | 2.9 | -- | V | $I_{OH}$ = -0.1 mA |
| | 2.4 | -- | V | $I_{OH}$ = -8.0 mA |
| | 2.2 | -- | V | $I_{OH}$ = -12.0 mA |
| Output Low, $V_{DDOUT}$ = 3.3V | -- | 0.1 | V | $I_{OH}$ = +0.1 mA |
| | -- | 0.5 | V | $I_{OH}$ = +8.0 mA |
| | -- | 0.8 | V | $I_{OH}$ = +12.0 mA |
| Rise & Fall Time | -- | 0.6 | nS | $V_{DDOUT}$ = 3.3v, 20 - 80%, 10pF Load |
| Output Symmetry | 45 | 55 | % | at 50% point of $V_{DDOUT}$ |

| Item | Min | Max | Unit | Condition |
|---|---|---|---|---|
| Peak-to-Peak Jitter[1][2] | -- | 100 | pS | 1 PLL Switching |
| | -- | 180 | pS | 4 PLLs Switching |
| Cycle-to-Cycle Jitter[1][2] | -- | 90 | pS | 1 PLL Switching |
| | -- | 170 | pS | 4 PLLs Switching |
| Output Skew | -- | 60 | pS | OUT1 to OUT2 |
| | -- | 160 | pS | OUT3 to OUT7 |
| **LVCMOS Output Parameters for $V_{DDOUT}$ = 2.5v** | | | | |
| Output High, $V_{DDOUT}$ = 2.5V | 2.2 | -- | V | $I_{OH}$ = -0.1 mA |
| | 1.7 | -- | V | $I_{OH}$ = -6.0 mA |
| | 1.6 | -- | V | $I_{OH}$ = -10.0 mA |
| Output Low, $V_{DDOUT}$ = 2.5V | -- | 0.1 | V | $I_{OH}$ = +0.1 mA |
| | -- | 0.5 | V | $I_{OH}$ = +6.0 mA |
| | -- | 0.7 | V | $I_{OH}$ = +10.0 mA |
| Rise & Fall Time | -- | 0.6 | nS | $V_{DDOUT}$ = 2.5v, 20 - 80%, 10pF Load |
| Output Symmetry | 45 | 55 | % | at 50% point of $V_{DDOUT}$ |
| Peak-to-Peak Jitter[1][2] | -- | 100 | pS | 1 PLL Switching |
| | -- | 180 | pS | 4 PLLs Switching |
| Cycle-to-Cycle Jitter[1][2] | -- | 90 | pS | 1 PLL Switching |
| | -- | 170 | pS | 4 PLLs Switching |
| Output Skew | -- | 60 | pS | OUT1 to OUT2 |
| | -- | 160 | pS | OUT3 to OUT7 |
| **LVCMOS Output Parameters for $V_{DDOUT}$ = 1.8v** | | | | |
| Output High, $V_{DDOUT}$ = 1.8V | 1.6 | -- | V | $I_{OH}$ = -0.1 mA |
| | 1.4 | -- | V | $I_{OH}$ = -3.0 mA |
| | 1.1 | -- | V | $I_{OH}$ = -6.0 mA |
| Output Low, $V_{DDOUT}$ = 1.8V | -- | 0.1 | V | $I_{OH}$ = +0.1 mA |
| | -- | 0.3 | V | $I_{OH}$ = +3.0 mA |
| | -- | 0.6 | V | $I_{OH}$ = +6.0 mA |
| Rise & Fall Time | -- | 0.9 | nS | $V_{DDOUT}$ = 1.8v, 20 - 80%, 10pF Load |
| Output Symmetry | 45 | 55 | % | at 50% point of $V_{DDOUT}$ |
| Peak-to-Peak Jitter[1][2] | -- | 140 | pS | 1 PLL Switching |
| | -- | 190 | pS | 4 PLLs Switching |
| Cycle-to-Cycle Jitter[1][2] | -- | 120 | pS | 1 PLL Switching |
| | -- | 170 | pS | 4 PLLs Switching |

| Item | Min | Max | Unit | Condition |
|---|---|---|---|---|
| Output Skew | -- | 60 | pS | OUT1 to OUT2 |
| | -- | 160 | pS | OUT3 to OUT7 |
| **LVCMOS Output Parameters for $V_{DDOUT}$ = 1.8v "L" Version** | | | | |
| Output High, $V_{DDOUT}$ = 1.8V | 1.6 | -- | V | $I_{OH}$ = -0.1 mA |
| | 1.4 | -- | V | $I_{OH}$ = -4.0 mA |
| | 1.1 | -- | V | $I_{OH}$ = -8.0 mA |
| Output Low, $V_{DDOUT}$ = 1.8V | -- | 0.1 | V | $I_{OH}$ = +0.1 mA |
| | -- | 0.3 | V | $I_{OH}$ = +4.0 mA |
| | -- | 0.6 | V | $I_{OH}$ = +8.0 mA |
| Rise & Fall Time | | 0.7 | nS | $V_{DDOUT}$ = 1.8v, 20 - 80%, 10pF Load |
| Output Symmetry | 45 | 55 | % | at 50% point of $V_{DDOUT}$ |
| Peak-to-Peak Jitter(1)(2) | -- | 140 | pS | 1 PLL Switching |
| | -- | 190 | pS | 4 PLLs Switching |
| Cycle-to-Cycle Jitter(1)(2) | -- | 120 | pS | 1 PLL Switching |
| | -- | 170 | pS | 4 PLLs Switching |
| Output Skew | -- | 60 | pS | OUT1 to OUT2 |
| | -- | 160 | pS | OUT3 to OUT7 |
| **VCXO Function** | | | | |
| Vcontrol Input Range Usable | 0.5 | $V_{DD}$ - 0.5V | V | The slope is positive |
| Vcontrol Input Range Allowed<br>- Direct connect to Vcontrol<br>- Limit current to ± 3mA | <br>0.0<br>-1.0 | <br>$V_{DD}$<br>4.0 | V | <br>The slope is positive<br>Recommend >=1K ohm to Vcontrol |
| Pull Ability specified in the P.N. | | | | |
| Linearity | -10 | +10 | % | |

(1) 10,000 cycles
(2) Jitter depends on the device configuration. Data is taken under the following conditions: 1-PLL; 27MHz Crystal, Out2 and Out3 are 27MHz (measured at Out2). 4-PLL; 27MHz Crystal, Out2 and Out3 are 27MHz (measured at Out2). Out4 is 16.384MHz, Out5 is 74.25MHz, Out6 and Out7 are 48MHz.

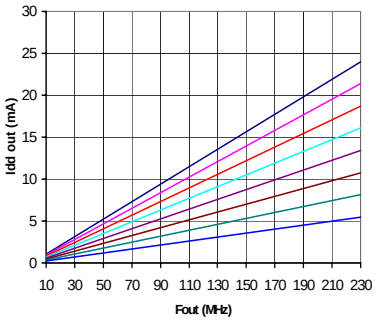
## Frequency Tolerance:

For the FD7x15T and the FD7x10T devices, Pletronics recommends that the tight tolerance be required on the PLL outputs only. In this case the reference frequency output would only achieve ±25ppm tolerance. This will reduce the cost of the device.

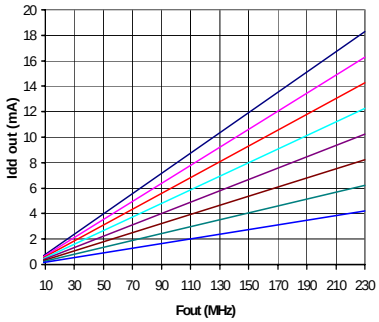
## FD7xxxT $I_{DDOUT}$ Current for Various Number of Outputs On

No Load VDD=1.8V

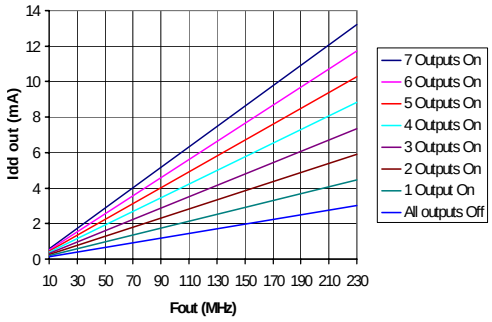
$V_{DDOUT}$=3.3V




$V_{DDOUT}$=2.5V

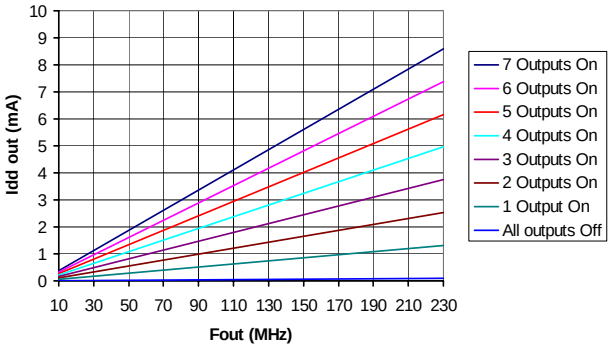



$V_{DDOUT}$=1.8V



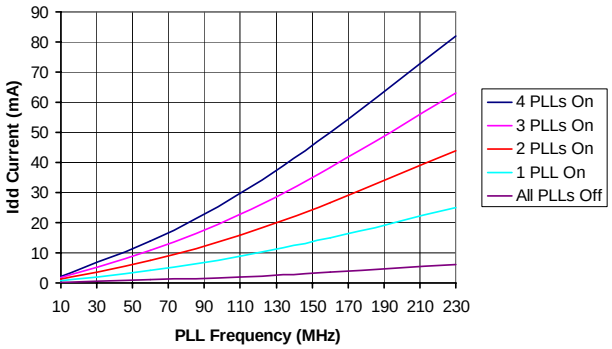

## FD7xxxTL $V_{DD}$ = $V_{DDOUT}$=1.8V

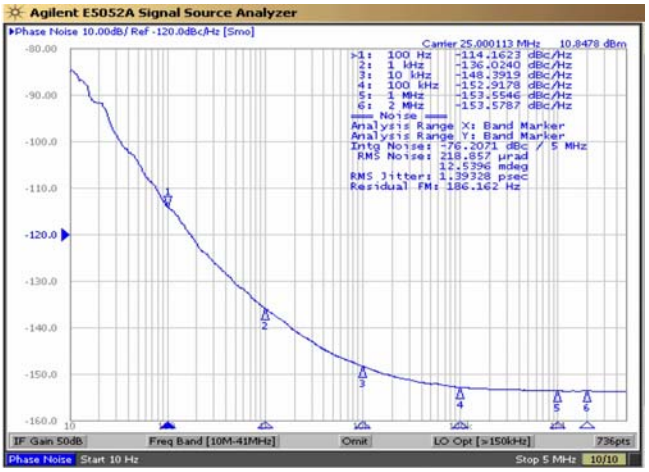
No Load




## FD7 Series $I_{DD}$ versus PLLs Used

$V_{DD}$=1.8V

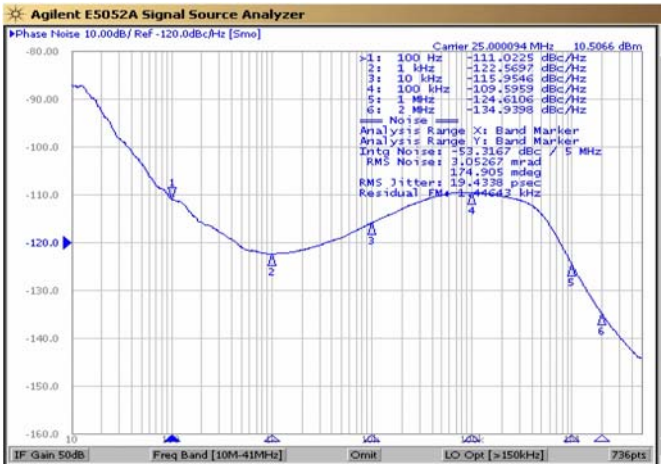


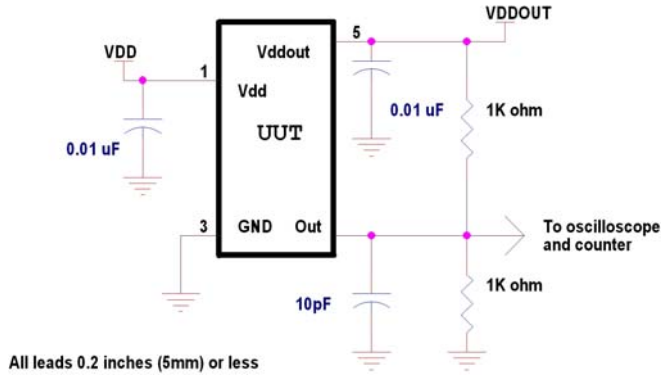

Phase noise of the reference signal, Out1.
25MHz Reference Frequency

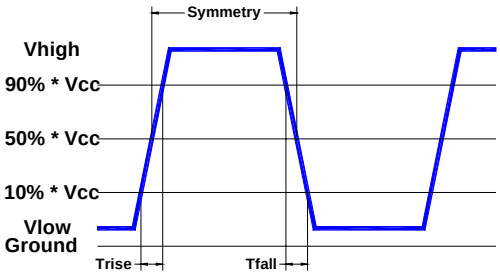
RMS jitter is 1.4pS from 10Hz to 2MHz

Example of the PLL synthesizing a frequency.
25MHz Reference Frequency
Multiply by 8 to 200MHz
Divide the 200MHz PLL output by 8
Phase noise plot of the resulting 25MHz on Out 2



## Load Circuit and Test Waveform



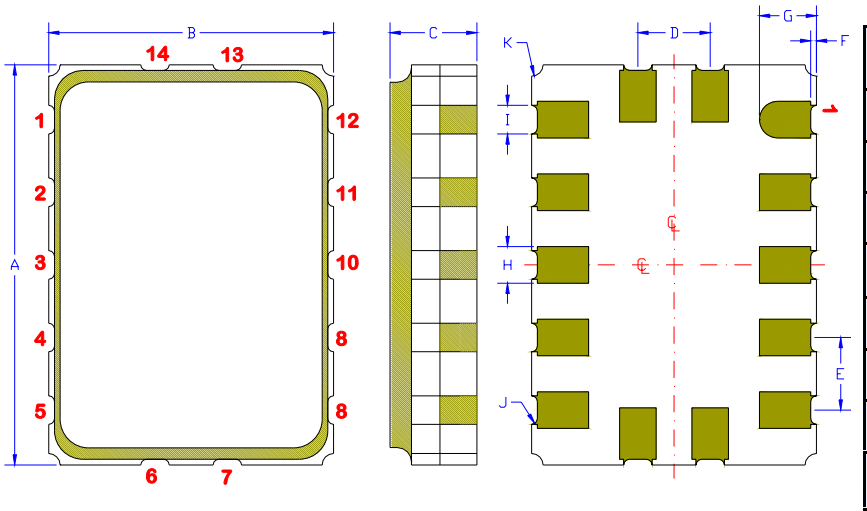

## Reliability: Environmental Compliance

| Parameter | Condition |
|---|---|
| Mechanical Shock | MIL-STD-883 Method 2002, Condition B |
| Vibration | MIL-STD-883 Method 2007, Condition A |
| Solderability | MIL-STD-883 Method 2003 |
| Thermal Shock | MIL-STD-883 Method 1011, Condition A |

## ESD Rating

| Model | Minimum Voltage | Conditions |
|---|---|---|
| Human Body Model | 1500 | MIL-STD-883 Method 3115 |
| Charged Device Model | 1000 | JESD 22-C101 |

## Mechanical:




| | Inches | mm |
|---|---|---|
| A | 0.276 ±0.006 | 7.00 ±0.15 |
| B | 0.197 ±0.006 | 5.00 ±0.15 |
| C | 0.067 max | 1.70 max |
| D[1] | 0.050 | 1.27 |
| E[1] | 0.050 | 1.27 |
| F[1] | 0.004 | 0.10 |
| G[1] | 0.039 | 1.00 |
| H[1] | 0.025 | 0.63 |
| I[1] | 0.020 | 0.50 |
| J[1] | 0.004r | 0.10r |
| K[1] | 0.008r | 0.20r |

Contacts:
Gold 11.8 µinches 0.3 µm minimum over
Nickel 50 to 350 µinches 1.27 to 8.89 µm

[1] Typical dimensions

Not to Scale

## Package Labeling

Label is 1" x 2.6" (25.4mm x 66.7mm)
Font is Courier New
Bar code is 39-Full ASCII

P/N: FD7745-25.0M-123
Customer P/N: 12345678
Qty: 500 D/C 6MC5P

Label is 1" x 2.6" (25.4mm x 66.7mm)
Font is Arial

RoHS Compliant
2nd LvL Interconnect
Category=e4
Max Safe Temp=260C for 10s 2X Max

## Pad Functions FD73xxT:

| Pad | Function | Note | | | Output Function | | |
|---|---|---|---|---|---|---|---|
| | | | | | Other | SSC | SSD |
| 1 | Vsupply1 | 1.8V, powers internal circuitry of the oscillator. Bypass capacitor required near the package pin. | | | | | |
| 2 | Vcontrol | Frequency control input when the VCXO function is enabled | | | | | |
| 3 | Ground (GND) | | | | | | |
| 4 | n.c. | No connection or connect to ground (do not connect to a signal lead) | | | | | |
| 5 | Vsupply2 | 1.8V, 2.5V or 3.3V supply for the output buffers. Sets CMOS output level. Bypass capacitor required near the package pin. | | | | | |
| 6 | n.c. | No connection or connect to ground (do not connect to a signal lead) | | | | | |
| 7 | n.c. | No connection or connect to ground (do not connect to a signal lead) | | | | | |
| 8 | n.c. | No connection or connect to ground (do not connect to a signal lead) | | | | | |
| 9 | Out3 (Y3) | Crystal reference frequency divider 1 and divided by 1 through 1023 | | | X | X | X |
| | | PLL1 frequency divider 2 and divided by 1 through 127 | | | X | X | X |
| | | PLL1 frequency divider 3 and divided by 1 through 127 | | | X | X | X |
| 10 | Out2 (Y2) | Crystal reference frequency divider 1 and divided by 1 through 1023 | | | X | | |
| | | PLL1 frequency divider 2 and divided by 1 through 127 | | | X | X | X |
| 11 | Out1 (Y1) | Crystal reference frequency divider 1 and divided by 1 through 1023 | | | X | | |
| | | PLL1 frequency divider 1 and divided by 1 through 1023 | | | X | X | X |
| 12 | S2 / SCL | Serial Data Clock | S2 | Input to select 1 of 8 preprogrammed functions of the outputs | | | |
| 13 | S1 / SDA | Serial Data | S1 | | | | |
| 14 | S0 | | S0 | | | | |

Other Logic “0" or tri-stated (off)
SSC The output can have a spread spectrum centered about the output frequency.
SSD The output can have a spread spectrum from the output frequency downward.
All unused inputs should be pulled high.

## Pad Functions FD74xxT:

| Pad | Function | Note | | | Output Function | | |
|---|---|---|---|---|---|---|---|
| | | | | | Other | SSC | SSD |
| 1 | Vsupply1 | 1.8V, powers internal circuitry of the oscillator. Bypass capacitor required near the package pin. | | | | | |
| 2 | Vcontrol | Frequency control input when the VCXO function is enabled | | | | | |
| 3 | Ground (GND) | | | | | | |
| 4 | Out4 (Y5) | PLL1 frequency divider 2 and divided by 1 through 127 | | | X | X | X |
| | | PLL2 frequency divider 4 and divided by 1 through 127 | | | | | |
| | | PLL2 frequency divider 5 and divided by 1 through 127 | | | | | |
| 5 | Vsupply2 | 1.8V, 2.5V or 3.3V supply for the output buffers. Sets CMOS output level. Bypass capacitor required near the package pin. | | | | | |
| 6 | n.c. | No connection or connect to ground (do not connect to a signal lead) | | | | | |
| 7 | n.c. | No connection or connect to ground (do not connect to a signal lead) | | | | | |
| 8 | n.c. | No connection or connect to ground (do not connect to a signal lead) | | | | | |
| 9 | Out3 (Y3) | Crystal reference frequency divider 1 and divided by 1 through 1023 | | | X | X | X |
| | | PLL1 frequency divider 2 and divided by 1 through 127 | | | X | X | X |
| | | PLL1 frequency divider 3 and divided by 1 through 127 | | | X | X | X |
| 10 | Out2 (Y2) | Crystal reference frequency divider 1 and divided by 1 through 1023 | | | X | | |
| | | PLL1 frequency divider 2 and divided by 1 through 127 | | | X | X | X |
| 11 | Out1 (Y1) | Crystal reference frequency divider 1 and divided by 1 through 1023 | | | X | | |
| | | PLL1 frequency divider 1 and divided by 1 through 1023 | | | X | X | X |
| 12 | S2 / SCL | Serial Data Clock | S2 | Input to select 1 of 8 preprogrammed functions of the outputs | | | |
| 13 | S1 / SDA | Serial Data | S1 | | | | |
| 14 | S0 | | S0 | | | | |

Other Logic “0" or tri-stated (off)
SSC The output can have a spread spectrum centered about the output frequency.
SSD The output can have a spread spectrum from the output frequency downward.
All unused inputs should be pulled high.

## Pad Functions FD75xxT:

| Pad | Function | Note | | | Output Function | | |
|---|---|---|---|---|---|---|---|
| | | | | | Other | SSC | SSD |
| 1 | Vsupply1 | 1.8V, powers internal circuitry of the oscillator. Bypass capacitor required near the package pin. | | | | | |
| 2 | Vcontrol | Frequency control input when the VCXO function is enabled | | | | | |
| 3 | Ground (GND) | | | | | | |
| 4 | Out4 (Y5) | PLL1 frequency divider 2 and divided by 1 through 127 | | | X | X | X |
| | | PLL2 frequency divider 4 and divided by 1 through 127 | | | | | |
| | | PLL2 frequency divider 5 and divided by 1 through 127 | | | | | |
| 5 | Vsupply2 | 1.8V, 2.5V or 3.3V supply for the output buffers. Sets CMOS output level. Bypass capacitor required near the package pin. | | | | | |
| 6 | n.c. | No connection or connect to ground (do not connect to a signal lead) | | | | | |
| 7 | n.c. | No connection or connect to ground (do not connect to a signal lead) | | | | | |
| 8 | Out5 (Y7) | PLL2 frequency divider 4 and divided by 1 through 127 | | | X | X | X |
| | | PLL3 frequency divider 6 and divided by 1 through 127 | | | X | X | X |
| | | PLL3 frequency divider 7 and divided by 1 through 127 | | | X | X | X |
| 9 | Out3 (Y3) | Crystal reference frequency divider 1 and divided by 1 through 1023 | | | X | X | X |
| | | PLL1 frequency divider 2 and divided by 1 through 127 | | | X | X | X |
| | | PLL1 frequency divider 3 and divided by 1 through 127 | | | X | X | X |
| 10 | Out2 (Y2) | Crystal reference frequency divider 1 and divided by 1 through 1023 | | | X | | |
| | | PLL1 frequency divider 2 and divided by 1 through 127 | | | X | X | X |
| 11 | Out1 (Y1) | Crystal reference frequency divider 1 and divided by 1 through 1023 | | | X | | |
| | | PLL1 frequency divider 1 and divided by 1 through 1023 | | | X | X | X |
| 12 | S2 / SCL | Serial Data Clock | S2 | Input to select 1 of 8 preprogrammed functions of the outputs | | | |
| 13 | S1 / SDA | Serial Data | S1 | | | | |
| 14 | S0 | | S0 | | | | |

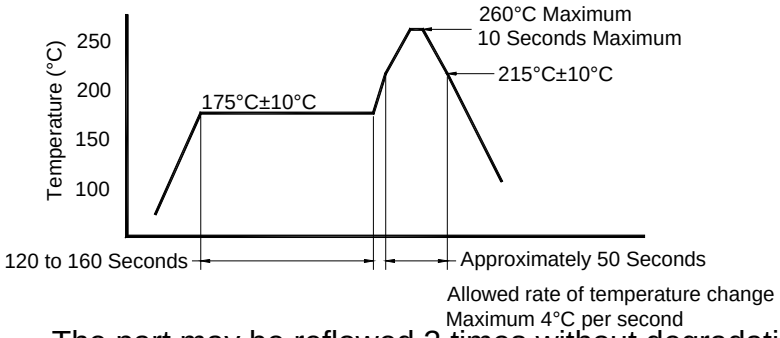
Other Logic “0" or tri-stated (off)
SSC The output can have a spread spectrum centered about the output frequency.
SSD The output can have a spread spectrum from the output frequency downward.
All unused inputs should be pulled high.

## Pad Functions FD77xxT:

| Pad | Function | Note | | | Output Function | | |
|---|---|---|---|---|---|---|---|
| | | | | | Other | SSC | SSD |
| 1 | Vsupply1 | 1.8V, powers internal circuitry of the oscillator. Bypass capacitor required near the package pin. | | | | | |
| 2 | Vcontrol | Frequency control input when the VCXO function is enabled | | | | | |
| 3 | Ground (GND) | | | | | | |
| 4 | Out4 (Y5) | PLL1 frequency divider 2 and divided by 1 through 127 | | | X | X | X |
| | | PLL2 frequency divider 4 and divided by 1 through 127 | | | | | |
| | | PLL2 frequency divider 5 and divided by 1 through 127 | | | | | |
| 5 | Vsupply2 | 1.8V, 2.5V or 3.3V supply for the output buffers. Sets CMOS output level. Bypass capacitor required near the package pin. | | | | | |
| 6 | Out6 (Y8) | PLL3 frequency divider 6 and divided by 1 through 127 | | | X | X | X |
| | | PLL4 frequency divider 8 and divided by 1 through 127 | | | X | X | X |
| 7 | Out7 (Y9) | PLL3 frequency divider 6 and divided by 1 through 127 | | | X | X | X |
| | | PLL4 frequency divider 8 and divided by 1 through 127 | | | X | X | X |
| | | PLL4 frequency divider 9 and divided by 1 through 127 | | | X | X | X |
| 8 | Out5 (Y7) | PLL2 frequency divider 4 and divided by 1 through 127 | | | X | X | X |
| | | PLL3 frequency divider 6 and divided by 1 through 127 | | | X | X | X |
| | | PLL3 frequency divider 7 and divided by 1 through 127 | | | X | X | X |
| 9 | Out3 (Y3) | Crystal reference frequency divider 1 and divided by 1 through 1023 | | | X | X | X |
| | | PLL1 frequency divider 2 and divided by 1 through 127 | | | X | X | X |
| | | PLL1 frequency divider 3 and divided by 1 through 127 | | | X | X | X |
| 10 | Out2 (Y2) | Crystal reference frequency divider 1 and divided by 1 through 1023 | | | X | | |
| | | PLL1 frequency divider 2 and divided by 1 through 127 | | | X | X | X |
| 11 | Out1 (Y1) | Crystal reference frequency divider 1 and divided by 1 through 1023 | | | X | | |
| | | PLL1 frequency divider 1 and divided by 1 through 1023 | | | X | X | X |
| 12 | S2 / SCL | Serial Data Clock | S2 | Input to select 1 of 8 preprogrammed functions of the outputs | | | |
| 13 | S1 / SDA | Serial Data | S1 | | | | |
| 14 | S0 | | S0 | | | | |

Other Logic “0" or tri-stated (off)
SSC The output can have a spread spectrum centered about the output frequency.
SSD The output can have a spread spectrum from the output frequency downward.
All unused inputs should be pulled high.

## Reflow Cycle (typical for lead free-processing)




The part may be reflowed 2 times without degradation.

## Tape and Reel: available for quantities of 250 to 1000 per reel, cut tape for < 250

Constant Dimensions Table 1

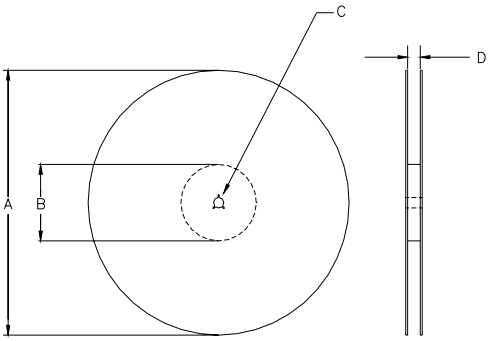
| Tape Size | D0 | D1 Min | E1 | P0 | P2 | S1 Min | T Max | T1 Max |
|---|---|---|---|---|---|---|---|---|
| 8mm | 1.5 +0.1 -0.0 | 1.0 | 1.75 ±0.1 | 4.0 ±0.1 | 2.0 ±0.05 | 0.6 | 0.6 | 0.1 |
| 12mm | | 1.5 | | | | | | |
| 16mm | | 1.5 | | | 2.0 ±0.1 | | | |
| 24mm | | 1.5 | | | | | | |

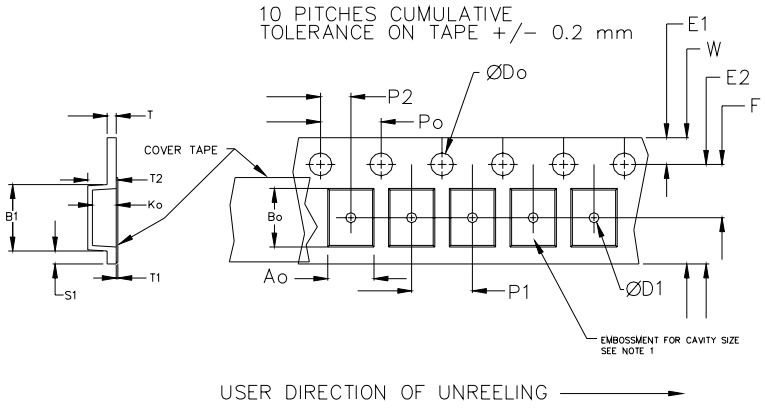
Variable Dimensions Table 2

| Tape Size | B1 Max | E2 Min | F | P1 | T2 Max | W Max | Ao, Bo & Ko |
|---|---|---|---|---|---|---|---|
| 16 mm | 12.1 | 14.25 | 7.5 ±0.1 | 8.0 ±0.1 | 8.0 | 16.3 | Note 1 |

Note 1: Embossed cavity to conform to EIA-481-B

Not to scale




| | | REEL DIMENSIONS | | | |
|---|---|---|---|---|---|
| A | inches | 7.0 | 10.0 | 13.0 | |
| | mm | 177.8 | 254.0 | 330.2 | |
| B | inches | 2.50 | 4.00 | 3.75 | |
| | mm | 63.5 | 101.6 | 95.3 | Tape Width |
| C | mm | 13.0 +0.5 / -0.2 | | | |
| D | mm | 16.4 +2.0 -0.0 | 16.4 +2.0 -0.0 | 16.4 +2.0 -0.0 | 16.0 |

Reel dimensions may vary from the above

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