
HM62W16255HCI Series

Wide Temperature Range Version
4M High Speed SRAM (256-kword × 16-bit)

HITACHI

ADE-203-1263A (Z)

Rev. 1.0
Nov. 1, 2001

Description

The HM62W16255HCI is a 4-Mbit high speed static RAM organized 256-kword × 16-bit. It has realized high speed access time by employing CMOS process (6-transistor memory cell) and high speed circuit designing technology. It is most appropriate for the application which requires high speed, high density memory and wide bit width configuration, such as cache and buffer memory in system. The HM62W16255HCI is packaged in 400-mil 44-pin SOJ and 400-mil 44-pin plastic TSOPII for high density surface mounting.

Features

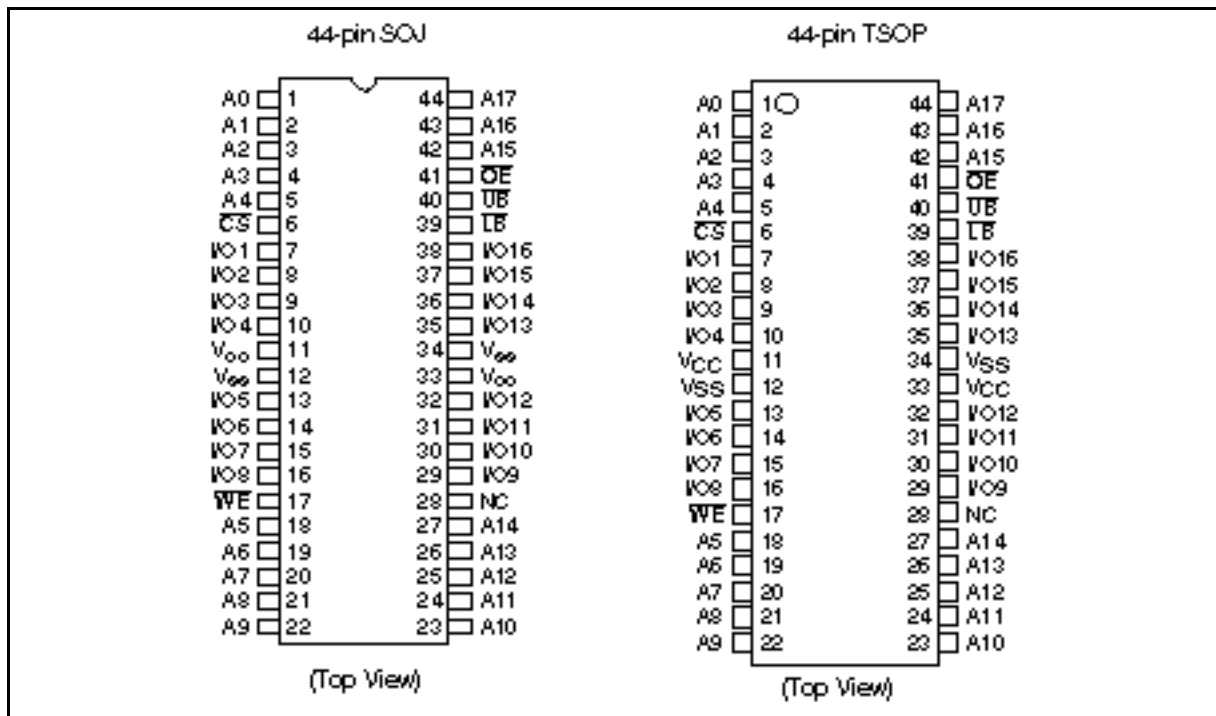
- Single 3.3 V supply: 3.3 V ± 0.3 V
- Access time: 12 ns (max)
- Completely static memory
 - No clock or timing strobe required
- Equal access and cycle times
- Directly TTL compatible
 - All inputs and outputs
- Operating current: 130 mA (max)
- TTL standby current: 40 mA (max)
- CMOS standby current: 5 mA (max)
- Center V_{CC} and V_{SS} type pinout
- Temperature range: -40 to +85°C

HM62W16255HCI Series

Ordering Information

Type No.	Access time	Device marking	Package
HM62W16255HCJPI-12	12 ns	HM62W16255CJPI12	400-mil 44-pin plastic SOJ (CP-44D)
HM62W16255HCTTI-12	12 ns	HM62W16255CTTI12	400-mil 44-pin plastic TSOPII (TTP-44DE)

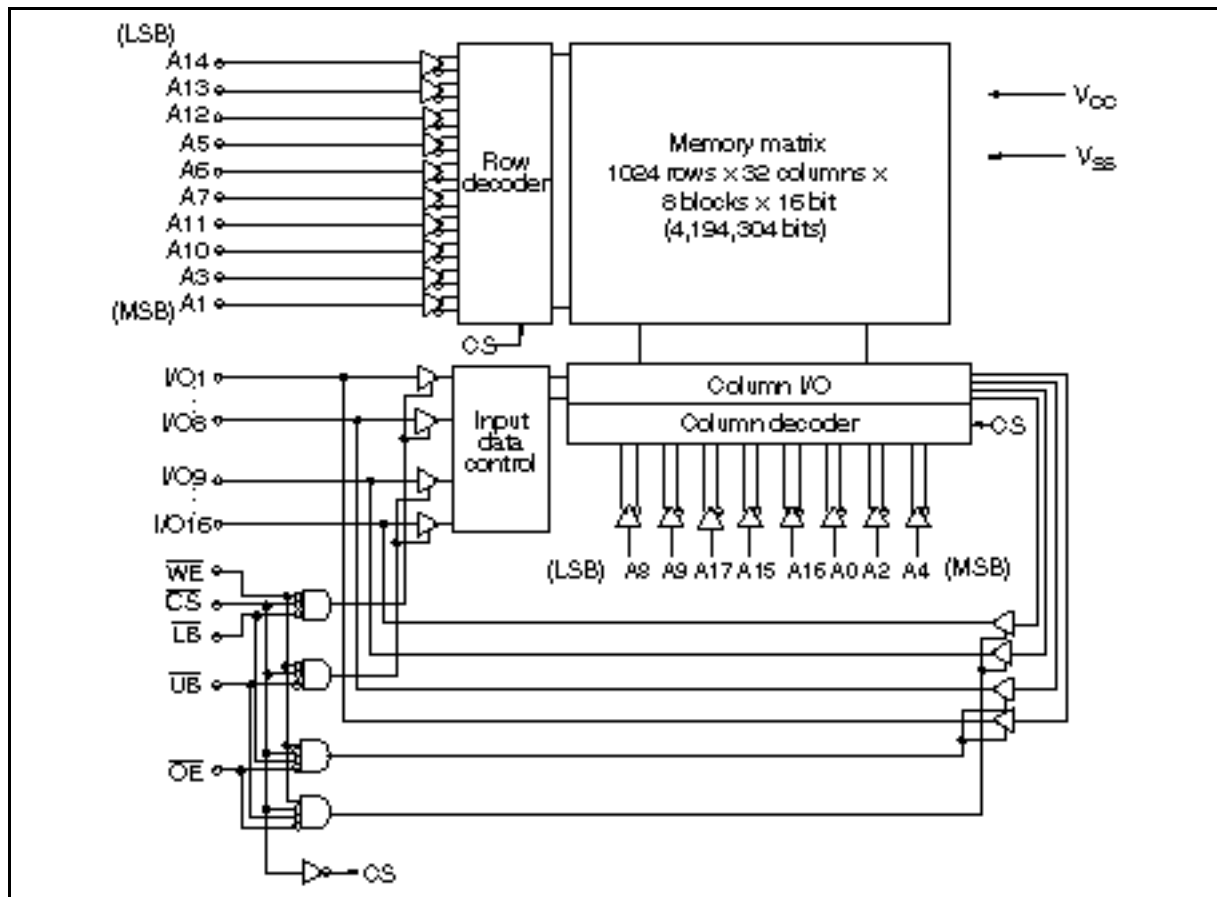
Pin Arrangement



Pin Description

Pin name	Function
A0 to A17	Address input
I/O1 to I/O16	Data input/output
CS	Chip select
OE	Output enable
WE	Write enable
UB	Upper byte select
LB	Lower byte select
V _{cc}	Power supply
V _{ss}	Ground
NC	No connection

Block Diagram



Operation Table

CS	OE	WE	LB	UB	Mode	V _{cc} current	I/O1–I/O8	I/O9–I/O16	Ref. cycle
H	×	×	×	×	Standby	I _{SB} , I _{SB1}	High-Z	High-Z	—
L	H	H	×	×	Output disable	I _{cc}	High-Z	High-Z	—
L	L	H	L	L	Read	I _{cc}	Output	Output	Read cycle
L	L	H	L	H	Lower byte read	I _{cc}	Output	High-Z	Read cycle
L	L	H	H	L	Upper byte read	I _{cc}	High-Z	Output	Read cycle
L	L	H	H	H	—	I _{cc}	High-Z	High-Z	—
L	×	L	L	L	Write	I _{cc}	Input	Input	Write cycle
L	×	L	L	H	Lower byte write	I _{cc}	Input	High-Z	Write cycle
L	×	L	H	L	Upper byte write	I _{cc}	High-Z	Input	Write cycle
L	×	L	H	H	—	I _{cc}	High-Z	High-Z	—

Note: H: V_{IH}, L: V_{IL}, ×: V_{IH} or V_{IL}

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage relative to V _{ss}	V _{cc}	–0.5 to +4.6	V
Voltage on any pin relative to V _{ss}	V _T	–0.5* ¹ to V _{cc} + 0.5* ²	V
Power dissipation	P _T	1.0	W
Operating temperature	T _{opr}	–40 to +85	°C
Storage temperature	T _{stg}	–55 to +125	°C
Storage temperature under bias	T _{bias}	–40 to +85	°C

- Notes: 1. V_T (min) = –2.0 V for pulse width (under shoot) ≤ 6 ns
 2. V_T (max) = V_{cc} + 2.0 V for pulse width (over shoot) ≤ 6 ns

HM62W16255HCI Series

Recommended DC Operating Conditions

($T_a = -40$ to $+85^\circ\text{C}$)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}^{*3}	3.0	3.3	3.6	V
	V_{SS}^{*4}	0	0	0	V
Input voltage	V_{IH}	2.0	—	$V_{CC} + 0.5^{*2}$	V
	V_{IL}	-0.5^{*1}	—	0.8	V

- Notes: 1. V_{IL} (min) = -2.0 V for pulse width (under shoot) ≤ 6 ns
 2. V_{IH} (max) = $V_{CC} + 2.0$ V for pulse width (over shoot) ≤ 6 ns
 3. The supply voltage with all V_{CC} pins must be on the same level.
 4. The supply voltage with all V_{SS} pins must be on the same level.

DC Characteristics

($T_a = -40$ to $+85^\circ\text{C}$, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $V_{SS} = 0 \text{ V}$)

Parameter	Symbol	Min	Typ ^{*1}	Max	Unit	Test conditions
Input leakage current	$ I_{UI} $	—	—	2	μA	$V_{in} = V_{SS}$ to V_{CC}
Output leakage current	$ I_{LO} $	—	—	2	μA	$V_{in} = V_{SS}$ to V_{CC}
Operating power supply current	I_{CC}	—	—	130	mA	Min cycle CS = V_{IL} , $I_{out} = 0$ mA Other inputs = V_{IH}/V_{IL}
Standby power supply current	I_{SB}	—	—	40	mA	Min cycle, CS = V_{IH} , Other inputs = V_{IH}/V_{IL}
	I_{SB1}	—	2.5	5	mA	f = 0 MHz $V_{CC} \geq CS \geq V_{CC} - 0.2 \text{ V}$, (1) $0 \text{ V} \leq V_{in} \leq 0.2 \text{ V}$ or (2) $V_{CC} \geq V_{in} \geq V_{CC} - 0.2 \text{ V}$
Output voltage	V_{OL}	—	—	0.4	V	$I_{OL} = 8$ mA
	V_{OH}	2.4	—	—	V	$I_{OH} = -4$ mA

Notes: 1. Typical values are at $V_{CC} = 3.3 \text{ V}$, $T_a = +25^\circ\text{C}$ and not guaranteed.

Capacitance

($T_a = +25^\circ\text{C}$, $f = 1.0\text{ MHz}$)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance* ¹	C_{in}	—	—	6	pF	$V_{in} = 0\text{ V}$
Input/output capacitance* ¹	$C_{i/o}$	—	—	8	pF	$V_{i/o} = 0\text{ V}$

Note: 1. This parameter is sampled and not 100% tested.

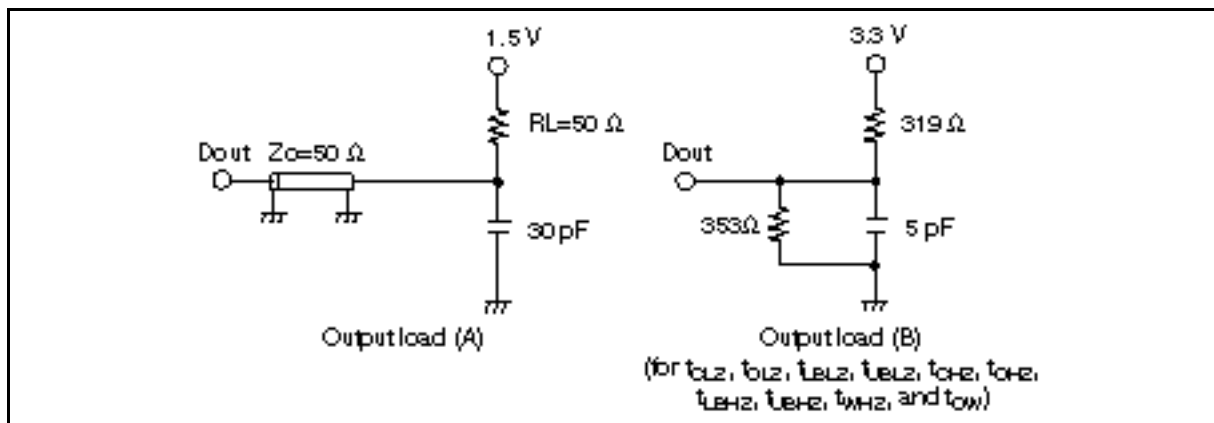
HM62W16255HCI Series

AC Characteristics

($T_a = -40$ to $+85^\circ\text{C}$, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$, unless otherwise noted.)

Test Conditions

- Input pulse levels: 3.0 V/0.0 V
- Input rise and fall time: 3 ns
- Input and output timing reference levels: 1.5 V
- Output load: See figures (Including scope and jig)



Read Cycle

Parameter	Symbol	HM62W16255HCI		Unit	Notes
		Min	Max		
Read cycle time	t_{RC}	12	—	ns	
Address access time	t_{AA}	—	12	ns	
Chip select access time	t_{ACS}	—	12	ns	
Output enable to output valid	t_{OE}	—	6	ns	
Byte select to output valid	t_{LB} , t_{UB}	—	6	ns	
Output hold from address change	t_{OH}	3	—	ns	
Chip select to output in low-Z	t_{CLZ}	3	—	ns	1
Output enable to output in low-Z	t_{OLZ}	0	—	ns	1
Byte select to output in low-Z	t_{LBLZ} , t_{UBLZ}	0	—	ns	1
Chip deselect to output in high-Z	t_{CHZ}	—	6	ns	1
Output disable to output in high-Z	t_{OHZ}	—	6	ns	1
Byte deselect to output in high-Z	t_{LBHZ} , t_{UBHZ}	—	6	ns	1

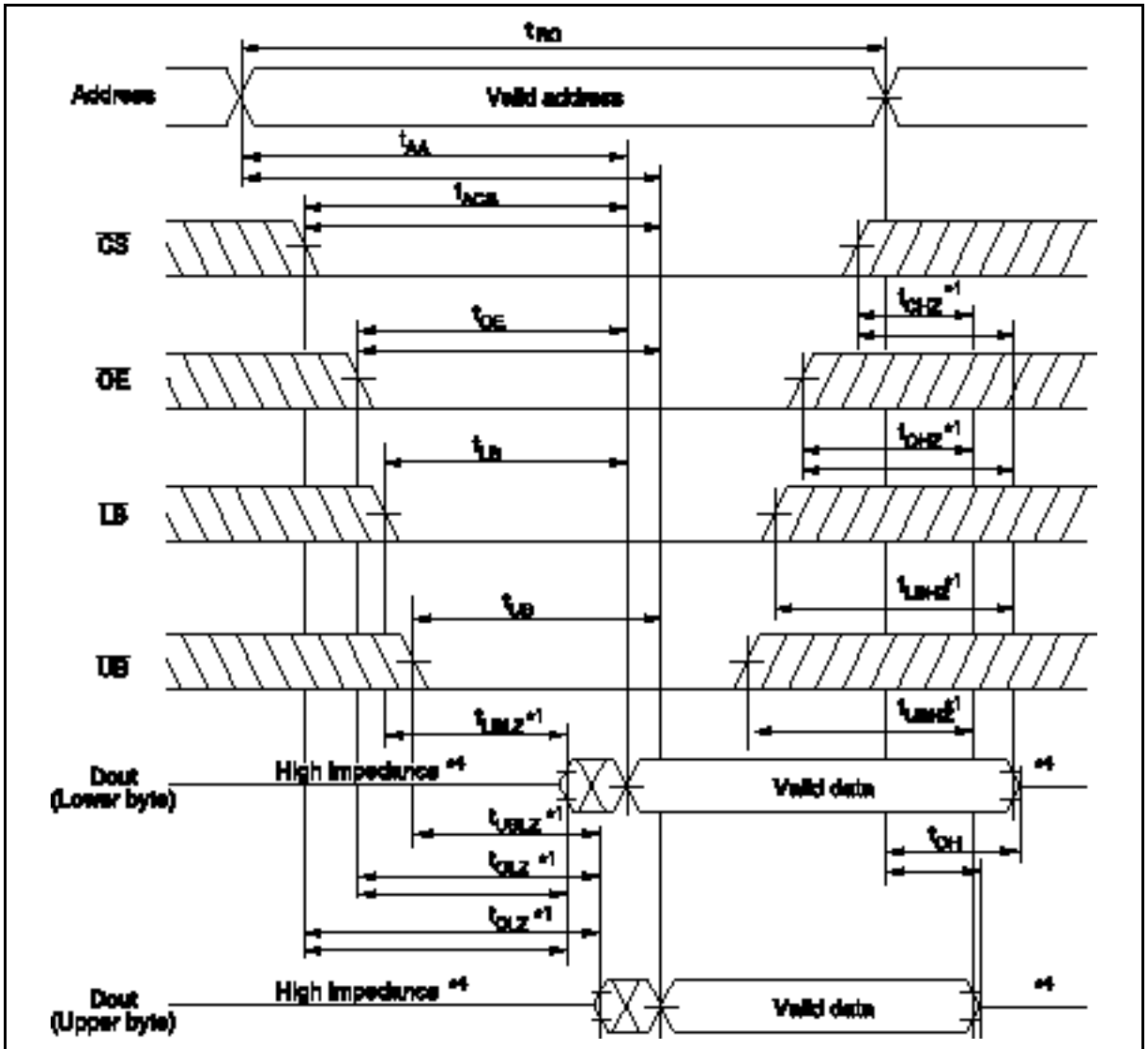
Write Cycle

Parameter	Symbol	HM62W16255HCI		Unit	Notes
		-12			
		Min	Max		
Write cycle time	t_{WC}	12	—	ns	
Address valid to end of write	t_{AW}	8	—	ns	
Chip select to end of write	t_{CW}	8	—	ns	8
Write pulse width	t_{WP}	8	—	ns	7
Byte select to end of write	t_{LBW}, t_{UBW}	8	—	ns	9, 10
Address setup time	t_{AS}	0	—	ns	5
Write recovery time	t_{WR}	0	—	ns	6
Data to write time overlap	t_{DW}	6	—	ns	
Data hold from write time	t_{DH}	0	—	ns	
Write disable to output in low-Z	t_{OW}	3	—	ns	1
Output disable to output in high-Z	t_{OHZ}	—	6	ns	1
Write enable to output in high-Z	t_{WHZ}	—	6	ns	1

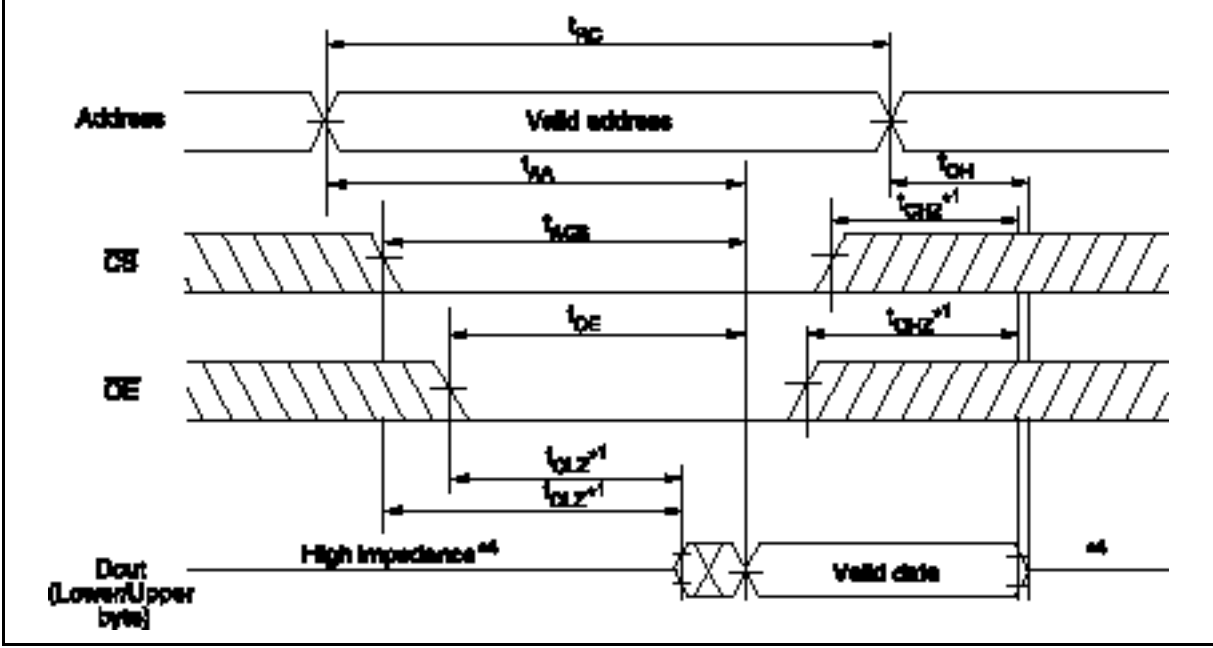
- Notes:
1. Transition is measured ± 200 mV from steady voltage with output load (B). This parameter is sampled and not 100% tested.
 2. If the CS or LB or UB low transition occurs simultaneously with the WE low transition or after the WE transition, output remains a high impedance state.
 3. WE and/or CS must be high during address transition time.
 4. If CS, OE, LB and UB are low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
 5. t_{AS} is measured from the latest address transition to the latest of CS, WE, LB or UB going low.
 6. t_{WR} is measured from the earliest of CS, WE, LB or UB going high to the first address transition.
 7. A write occurs during the overlap of low CS, low WE and low LB or low UB.
 8. t_{CW} is measured from the later of CS going low to the end of write.
 9. t_{LBW} is measured from the later of LB going low to the end of write.
 10. t_{UBW} is measured from the later of UB going low to the end of write.

Timing Waveforms

Read Timing Waveform (1) ($WE = V_{IH}$)

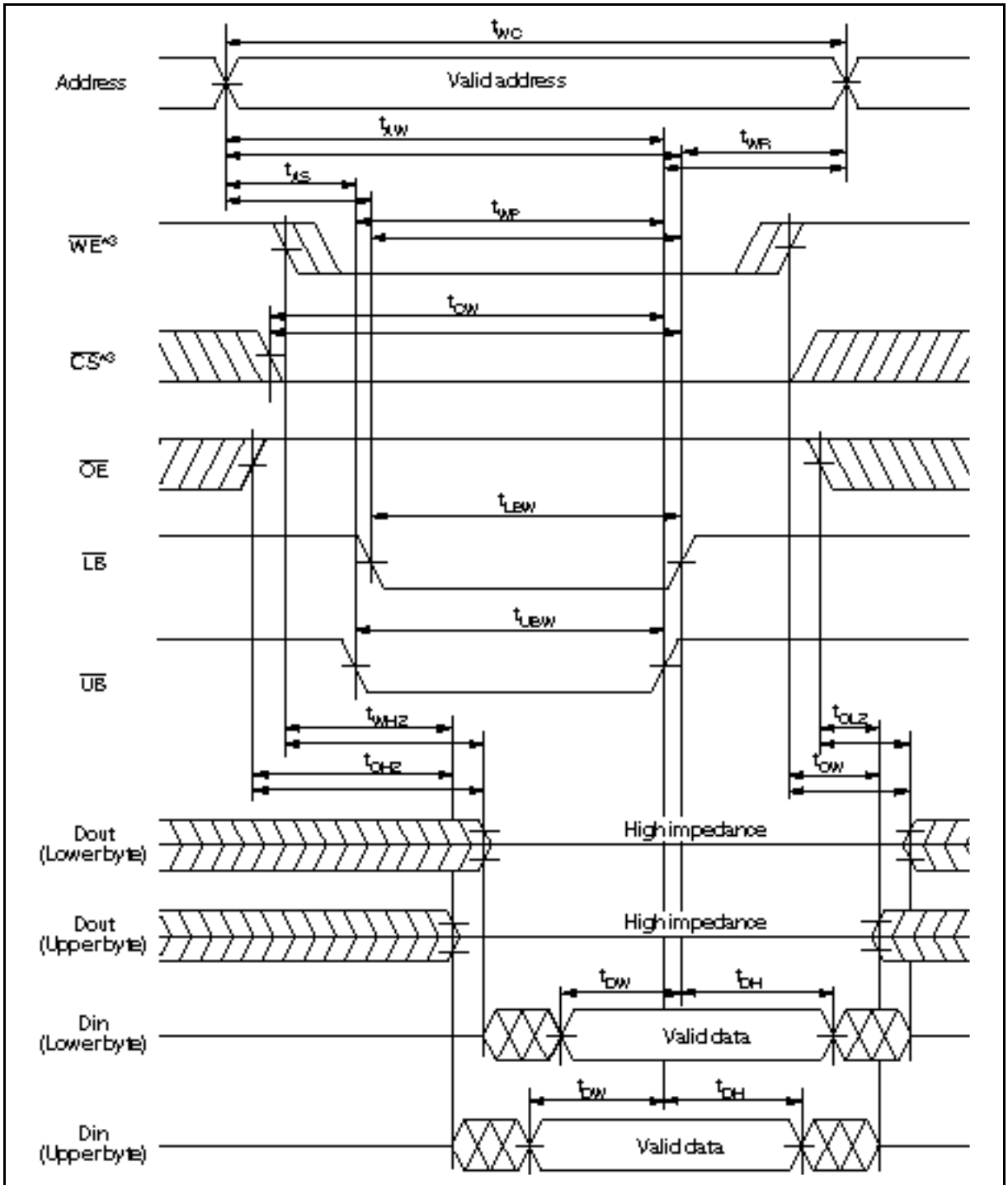


Read Timing Waveform (2) ($WE = V_{IH}$, $LB = V_{IL}$, $UB = V_{IL}$)



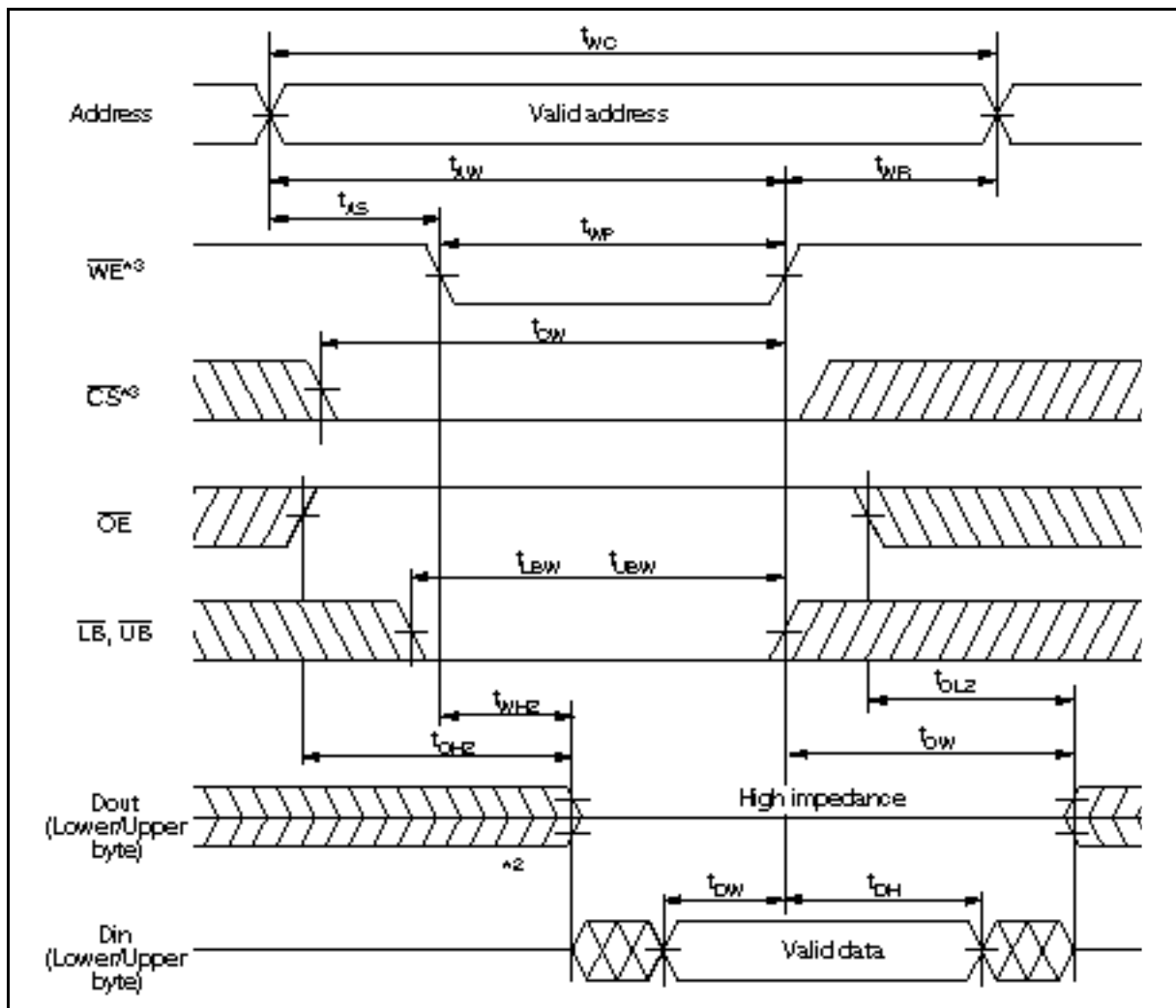
HM62W16255HCI Series

Write Timing Waveform (1) (LB, UB Controlled)



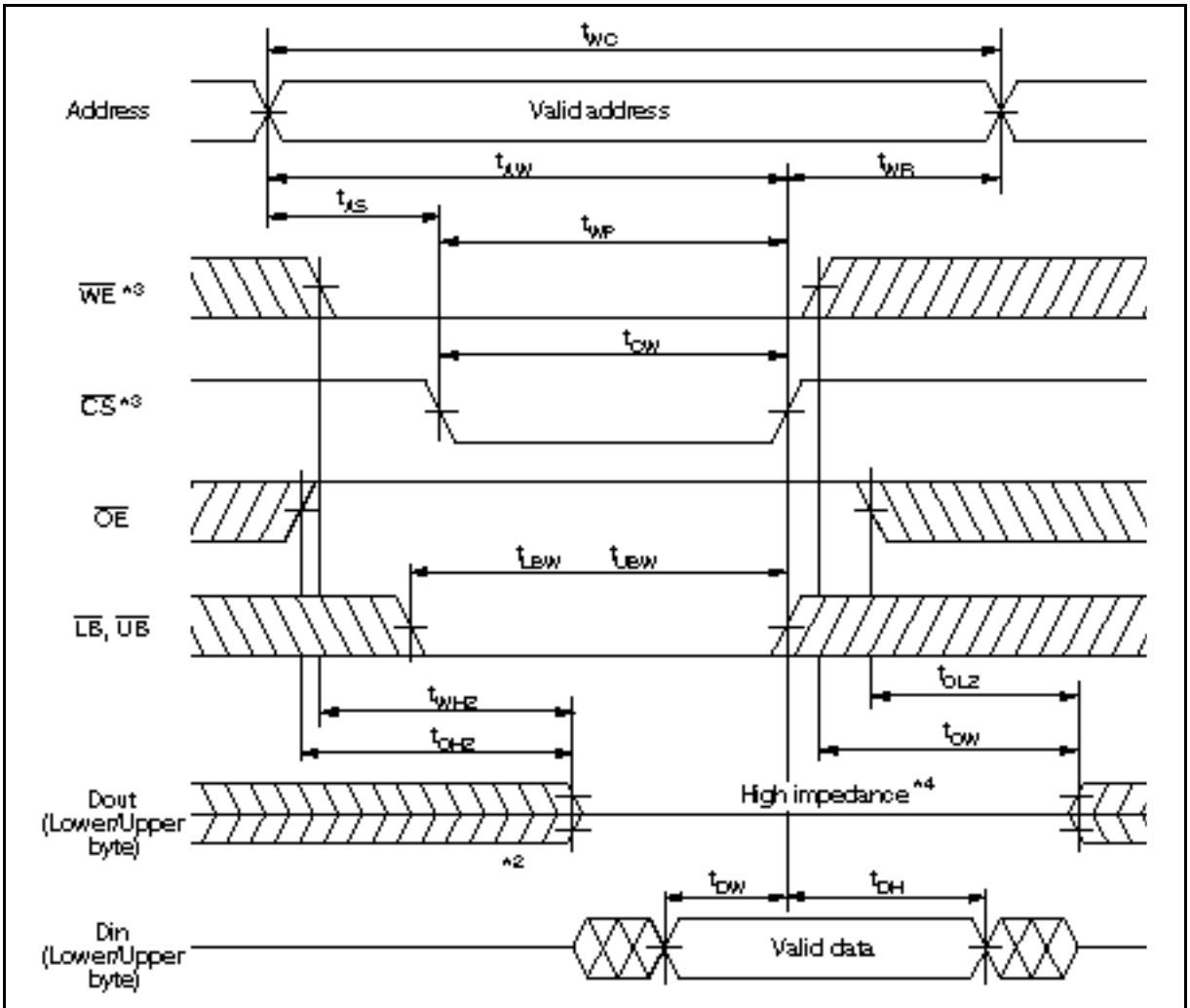
HITACHI

Write Timing Waveform (2) (WE Controlled)



HM62W16255HCI Series

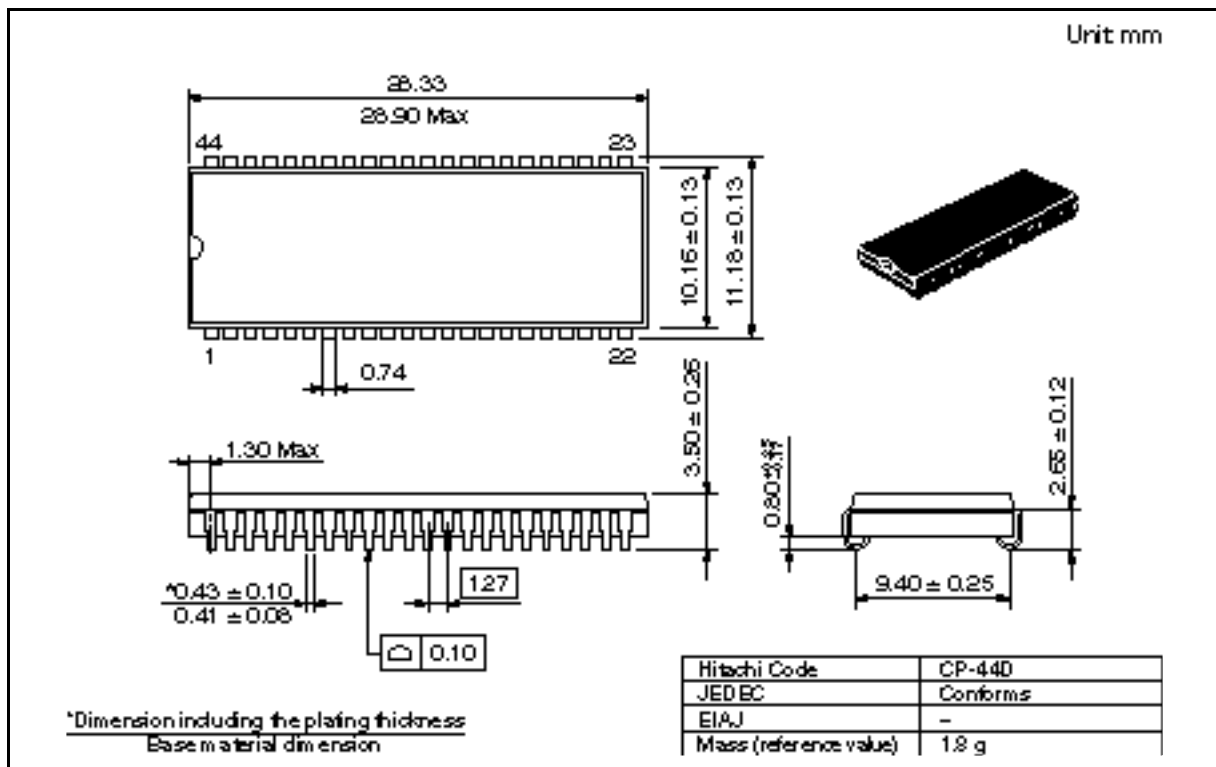
Write Timing Waveform (3) (CS Controlled)



HITACHI

Package Dimensions

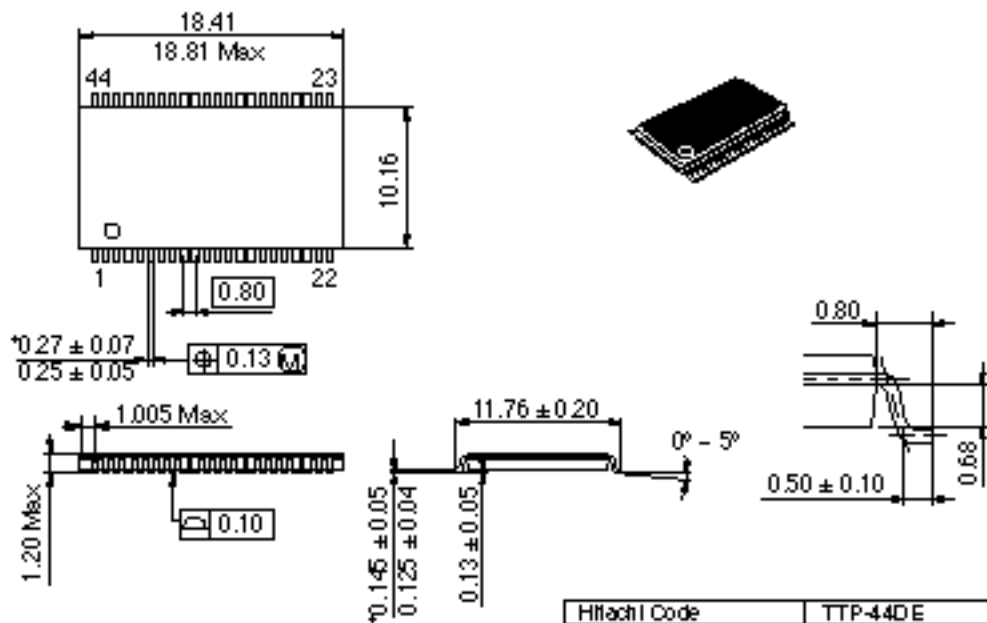
HM62W16255HCJPI Series (CP-44D)



HM62W16255HCI Series

HM62W16255HCTTI Series (TTP-44DE)

Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-44DE
JED BC	-
EIAJ	-
Mass (reference value)	0.43 g

HITACHI

Disclaimer

1. Hitachi neither warrants nor grants licenses of any rights of Hitachi's or any third party's patent, copyright, trademark, or other intellectual property rights for information contained in this document. Hitachi bears no responsibility for problems that may arise with third party's rights, including intellectual property rights, in connection with use of the information contained in this document.
2. Products and product specifications may be subject to change without notice. Confirm that you have received the latest product standards or specifications before final design, purchase or use.
3. Hitachi makes every attempt to ensure that its products are of high quality and reliability. However, contact Hitachi's sales office before using the product in an application that demands especially high quality and reliability or where its failure or malfunction may directly threaten human life or cause risk of bodily injury, such as aerospace, aeronautics, nuclear power, combustion control, transportation, traffic, safety equipment or medical equipment for life support.
4. Design your application so that the product is used within the ranges guaranteed by Hitachi particularly for maximum rating, operating supply voltage range, heat radiation characteristics, installation conditions and other characteristics. Hitachi bears no responsibility for failure or damage when used beyond the guaranteed ranges. Even within the guaranteed ranges, consider normally foreseeable failure rates or failure modes in semiconductor devices and employ systemic measures such as fail-safes, so that the equipment incorporating Hitachi product does not cause bodily injury, fire or other consequential damage due to operation of the Hitachi product.
5. This product is not designed to be radiation resistant.
6. No one is permitted to reproduce or duplicate, in any form, the whole or part of this document without written approval from Hitachi.
7. Contact Hitachi's sales office for any questions regarding this document or Hitachi semiconductor products.

Sales Offices

Title:
(adaddsem010416.EPS)
Creator:
Adobe Illustrator(TM) 5.5
Preview:
This EPS picture was not saved
with a preview included in it.
Comment:
This EPS picture will print to a
PostScript printer, but not to
other types of printers.