PRELIMINARY

Integrated Circuit Systems, Inc.

ICS840004

FEMTOCLOCKS™ CRYSTAL-TO-LVCMOS/LVTTL FREQUENCY SYNTHESIZER

GENERAL DESCRIPTION

The ICS840004 is a 4 output LVCMOS/LVTTL Synthesizer optimized to generate Ethernet reference clock frequencies and is a member of the HiPerClocks™ family of high performance clock solutions from ICS. Using a 26.5625MHz, 18pF parallel resonant crystal, the following frequencies can be generated based on the 2 frequency select pins (F_SEL1:0): 212.5MHz, 159.375MHz, 156.25MHz, 106.25MHz, and 53.125MHz. The ICS840004 uses ICS' 3rd generation low phase noise VCO technology and can achieve 1ps or lower typical random rms phase jitter, easily meeting Ethernet jitter requirements. The ICS840004 is packaged in a small 20-pin TSSOP package.

FEATURES

- Four LVCMOS/LVTTL outputs, 15Ω typical output impedance
- Selectable crystal oscillator interface or LVCMOS single-ended input
- Supports the following input frequencies: 212.5MHz, 159.375MHz, 156.25MHz, 106.25MHz and 53.125MHz
- RMS phase jitter @ 212.5MHz (637KHz - 10MHz): 0.98ps typical
- RMS phase noise at 212.5MHz, V_{DDO} = 3.3V

  Phase noise:

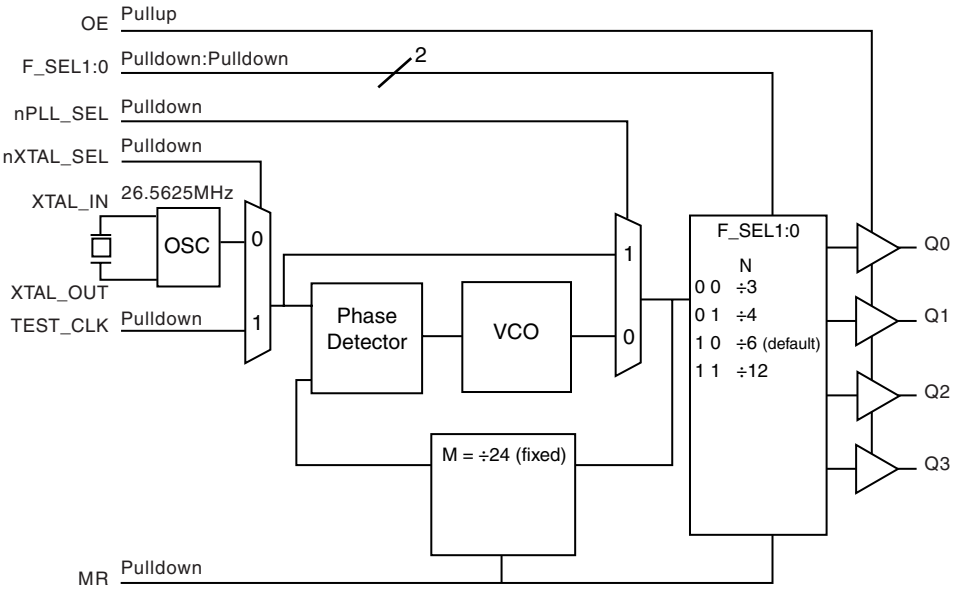
Offset	Noise Power
100Hz	-88.8 dBc/Hz
1KHz	-109.0 dBc/Hz
10KHz	-116.1 dBc/Hz
100KHz	-117.5 dBc/Hz

- Full 3.3V or 3.3V core/2.5V output supply mode
- 0°C to 70°C ambient operating temperature

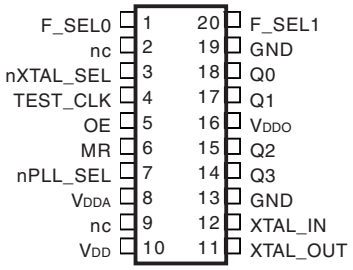
FREQUENCY SELECT FUNCTION TABLE

Inputs						Output Frequency Range
Input Frequency	F_SEL1	F_SEL0	M Divider Value	N Divider Value	M/N Ratio Value	
26.5625	0	0	24	3	8	212.5
26.5625	0	1	24	4	6	159.375
26.5625	1	0	24	6	4	106.25
26.5625	1	1	24	12	2	53.125
26.04166	0	1	24	4	6	156.25

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS840004

20-Lead TSSOP

6.5mm x 4.4mm x 0.92mm package body

G Package

Top View

The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	F_SEL0	Input	Pulldown	Frequency select pin. LVCMOS/LVTTL interface levels.
2, 9	nc	Unused		No connect.
3	nXTAL_SEL	Input	Pulldown	Selects between the crystal or TEST_CLK inputs as the PLL reference source. When HIGH, selects TEST_CLK. When LOW, selects XTAL inpus. LVCMOS/LVTTL interface levels.
4	TEST_CLK	Input	Pulldown	Single-ended LVCMOS/LVTTL clock input.
5	OE	Input	Pullup	Output enable pin. When HIGH, the outputs are active. When LOW, the outputs are in a high impedance state. LVCMOS/LVTTL interface levels.
6	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the otuputs to go low. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
7	nPLL_SEL	Input	Pulldown	PLL Bypass. When LOW, the output is driven from the VCO output. When HIGH, the PLL is bypassed and the output frequency = reference clock frequency/N output divider. LVCMOS/LVTTL interface levels.
8	V_{DDA}	Power		Analog supply pin.
10	V_{DD}	Power		Core supply pin.
11, 12	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_OUT is the output. XTAL_IN is the input.
13, 19	GND	Power		Power supply ground.
14, 15 17, 18	Q3, Q2, Q1, Q0	Output		Single-ended clock outputs. LVCMOS/LVTTL interface levels. 15Ω typical output impedence.
16	V_{DDO}	Power		Output supply pin.
20	F_SEL1	Input	Pulldown	Frequency select pin. LVCMOS/LVTTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
C_{PD}	Power Dissipation Capacitance	V_{DD}, V_{DDA}, V_{DDO} = 3.465V		TBD		pF
		V_{DD}, V_{DDA} = 3.465V, V_{DDO} = 2.625V		TBD		pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ
R_{OUT}	Output Impedance			15		Ω

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	73.2°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, $V_{DDD} = V_{DDA} = 3.3V±5\%$, $V_{DDO} = 3.3V±5\%$ OR $2.5V±5\%$, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
I_{DD}	Power Supply Current			87		mA
I_{DDA}	Analog Supply Current			8		mA
I_{DDO}	Output Supply Current			5		mA

TABLE 3B. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V±5\%$, $V_{DDO} = 3.3V±5\%$ OR $2.5V±5\%$, T_A = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	F_SEL1:0, nPLL_SEL, nXTAL_SEL, OE, MR		2		V_{DD} + 0.3	V
		TEST_CLK		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	F_SEL1:0, nPLL_SEL, nXTAL_SEL, OE, MR		-0.3		0.8	V
		TEST_CLK		-0.3		1.3	V
I_{IH}	Input High Current	OE	$V_{DD} = V_{IN} = 3.465V$			5	µA
		F_SEL0:1, nPLL_SEL, MR, nXTAL_SEL, TEST_CLK	$V_{DD} = V_{IN} = 3.465V$			150	µA
I_{IL}	Input Low Current	OE	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-150			µA
		F_SEL0:1, nPLL_SEL, MR, nXTAL_SEL, TEST_CLK	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-5			µA
V_{OH}	Output High Voltage; NOTE 1		$V_{DDO} = 3.3V ± 5\%$	2.6			V
			$V_{DDO} = 2.5V ± 5\%$	1.8			V
V_{OL}	Output Low Voltage; NOTE 1		$V_{DDO} = 3.3V$ or $2.5V ± 5\%$			0.5	V

NOTE 1: Outputs terminated with 50Ω to $V_{DDO}/2$. See Parameter Measurement Information, Output Load Test Circuit.

TABLE 4. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency			26.5625		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

NOTE: Characterized using an 18pf parallel resonant crystal.

TABLE 5A. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V±5\%$, $T_A = 0°C$ TO $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency			212.5		MHz
				159.375		MHz
				156.25		MHz
				106.25		MHz
				53.125		MHz
*t*sk(o)	Output Skew; NOTE 1, 3			TBD		ps
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 2	212.5MHz (637KHz - 10MHz)		0.98		ps
		159.375MHz (637KHz - 10MHz)		0.84		ps
		156.25MHz (1.875MHz - 20MHz)		TBD		ps
		106.25MHz (637KHz - 10MHz)		0.83		ps
		53.125MHz (637KHz - 10MHz)		1.0		ps
t_L	PLL Lock Time				1	ms
t_R / t_F	Output Rise/Fall Time	20% to 80%		500		ps
odc	Output Duty Cycle			50		%

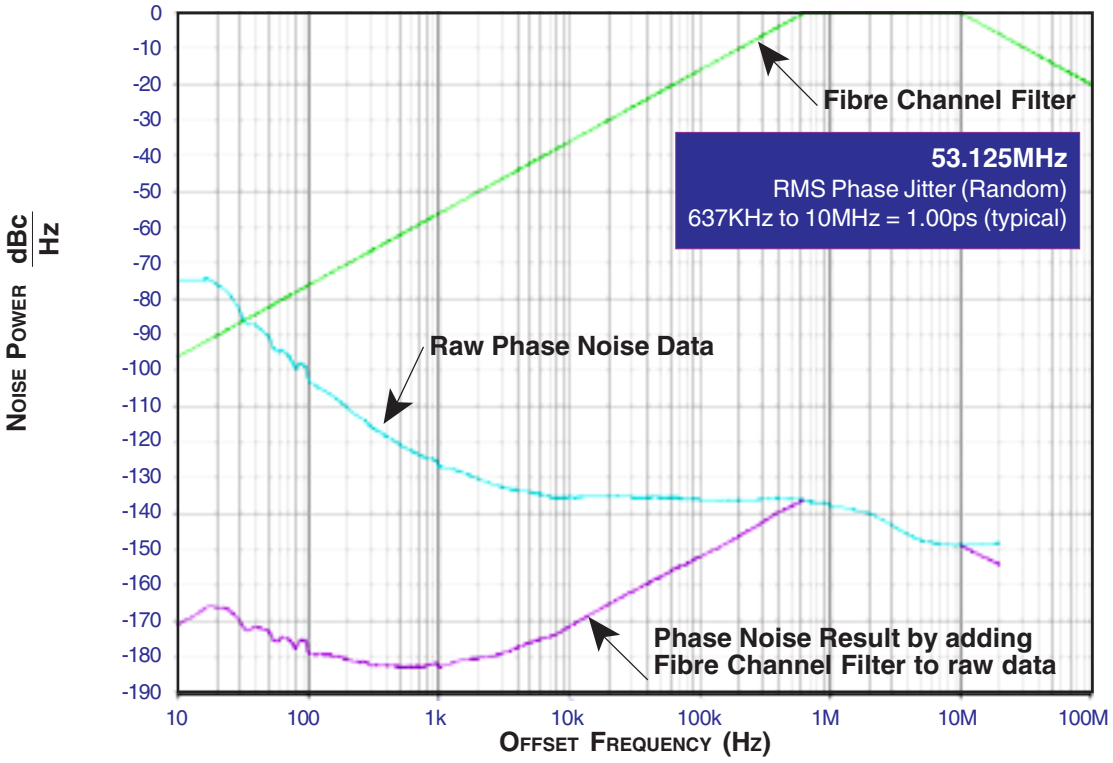
NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 2: Please refer to the Phase Noise Plot.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5B. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V±5\%$, $V_{DDO} = 3.3V±5\%$ OR $2.5V±5\%$, $T_A = 0°C$ TO $70°C$

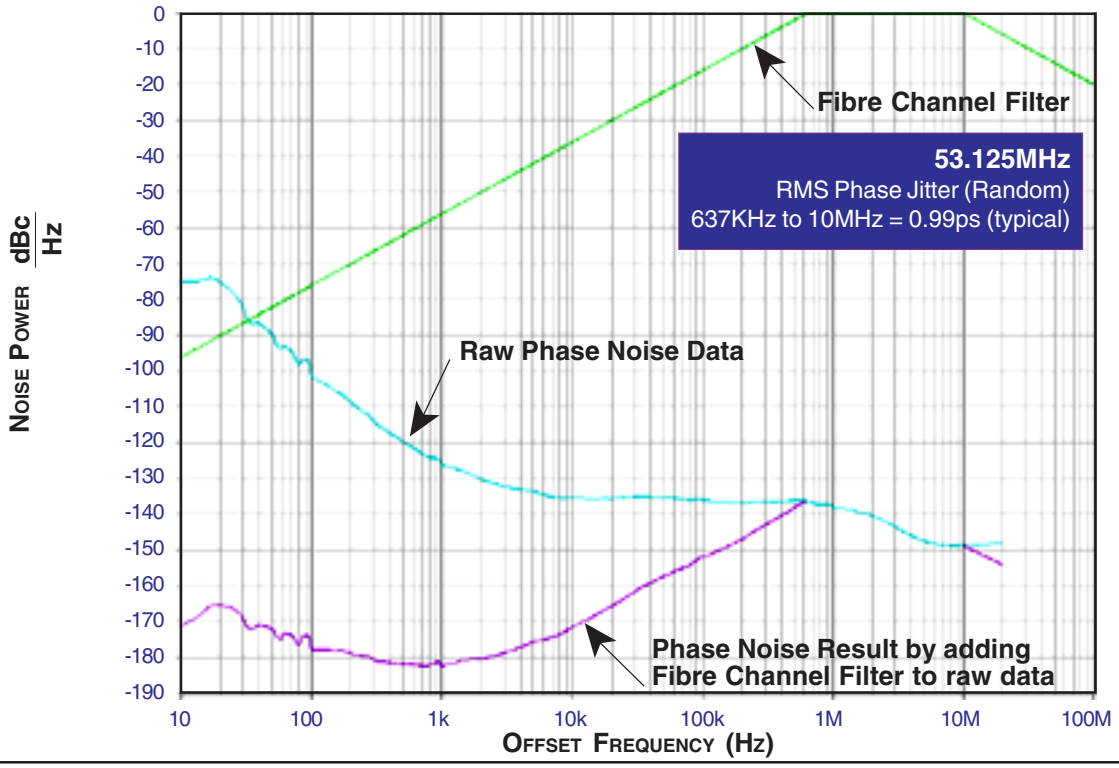
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency			212.5		MHz
				159.375		MHz
				156.25		MHz
				106.25		MHz
				53.125		MHz
*t*sk(o)	Output Skew; NOTE 1, 3			TBD		ps
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 2	212.5MHz (637KHz - 10MHz)		0.93		ps
		159.375MHz (637KHz - 10MHz)		0.76		ps
		156.25MHz (1.875MHz - 20MHz)		TBD		ps
		106.25MHz (637KHz - 10MHz)		0.81		ps
		53.125MHz (637KHz - 10MHz)		0.99		ps
t_L	PLL Lock Time				1	ms
t_R / t_F	Output Rise/Fall Time	20% to 80%		500		ps
odc	Output Duty Cycle			50		%

For notes see above, Table 4A.

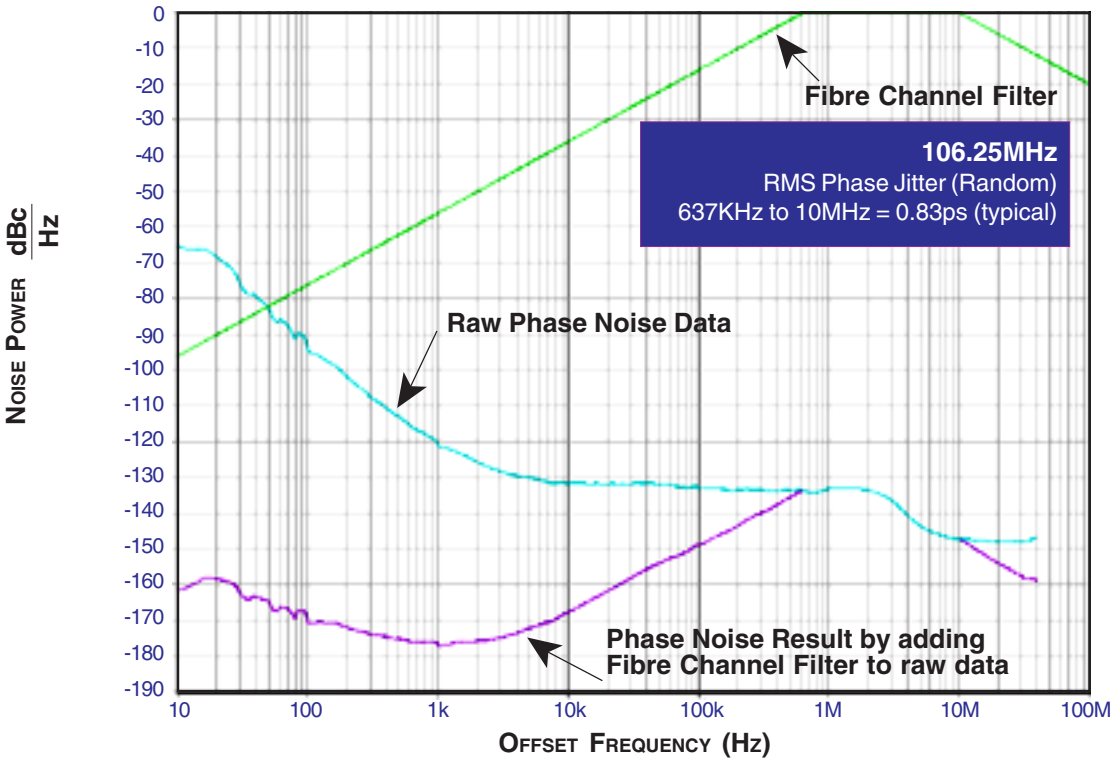
TYPICAL PHASE NOISE AT 53.125MHZ @3.3V



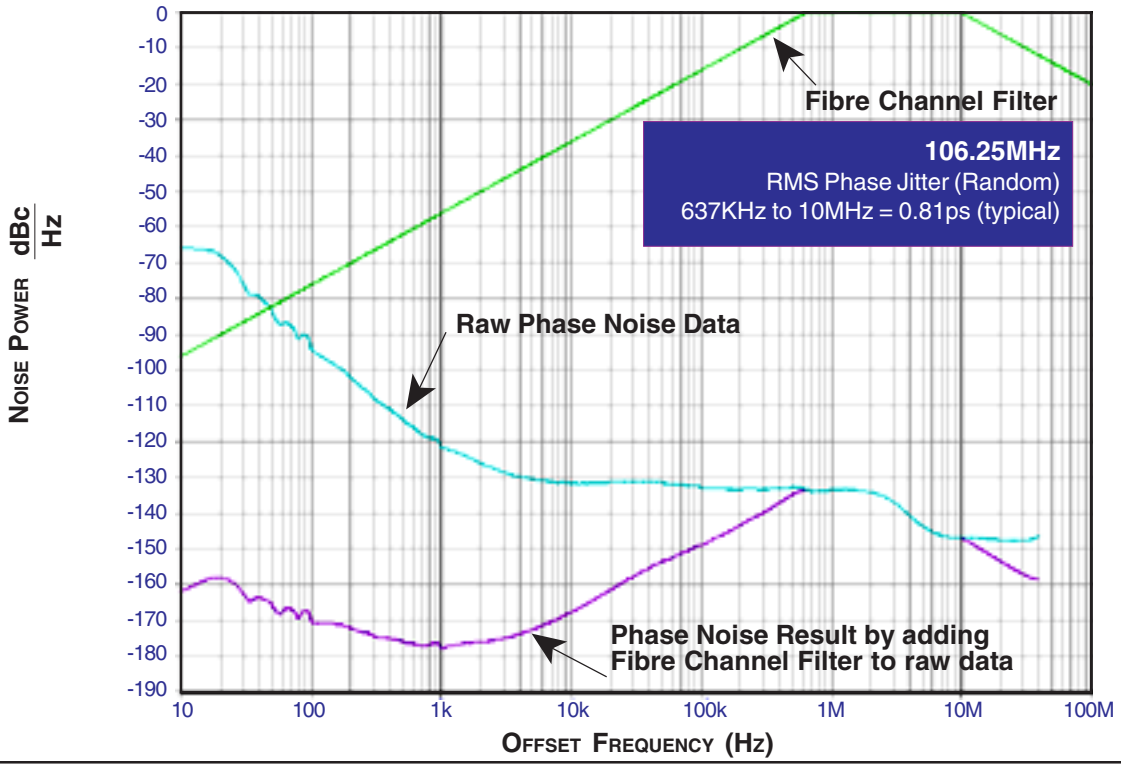
TYPICAL PHASE NOISE AT 53.125MHZ @2.5V



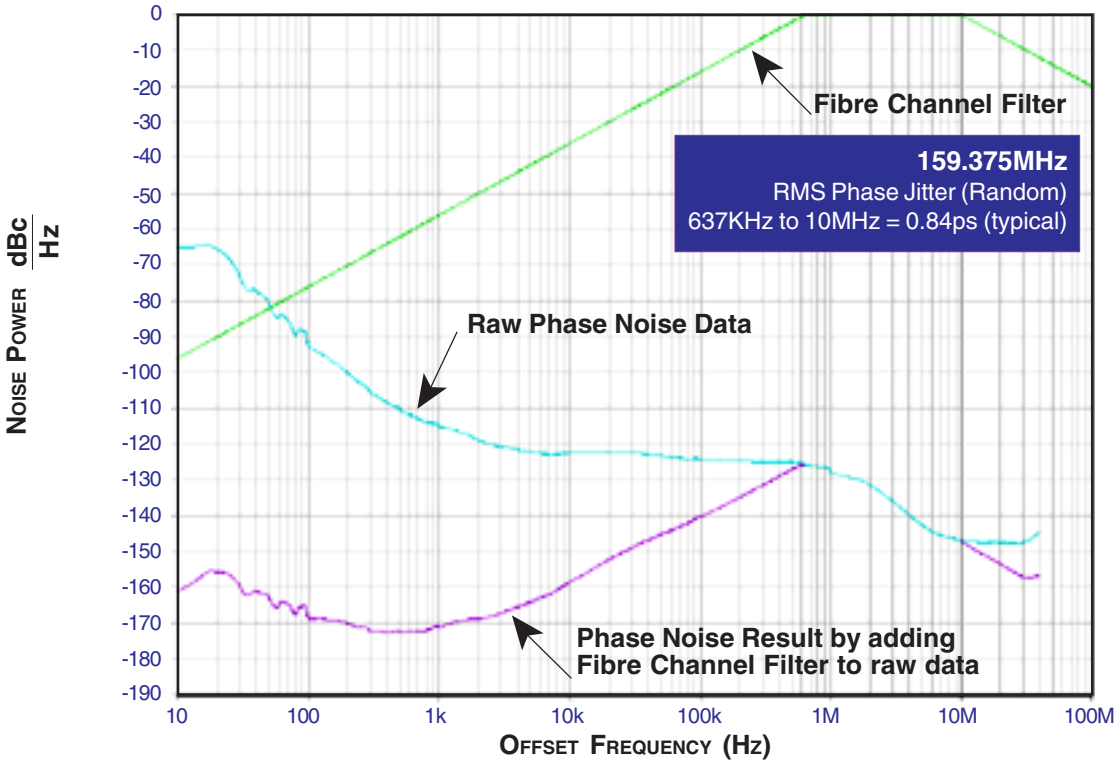
TYPICAL PHASE NOISE AT 106.25MHZ @3.3V



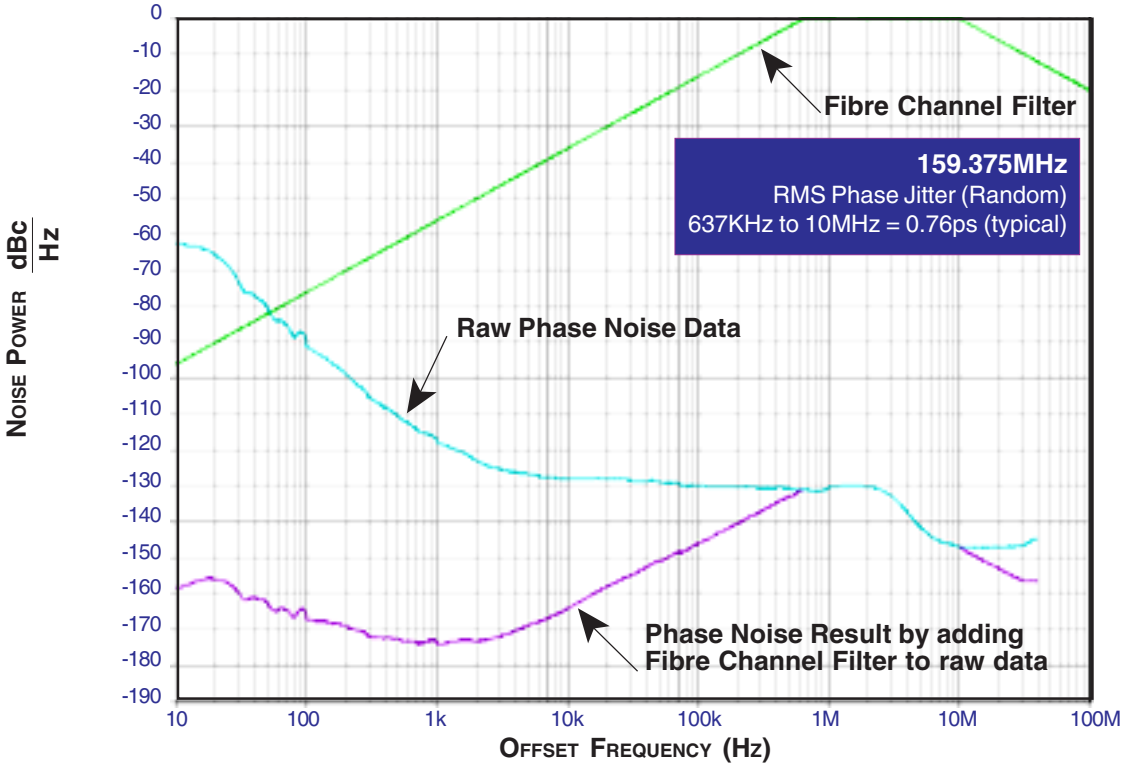
TYPICAL PHASE NOISE AT 106.25MHZ @ 2.5V



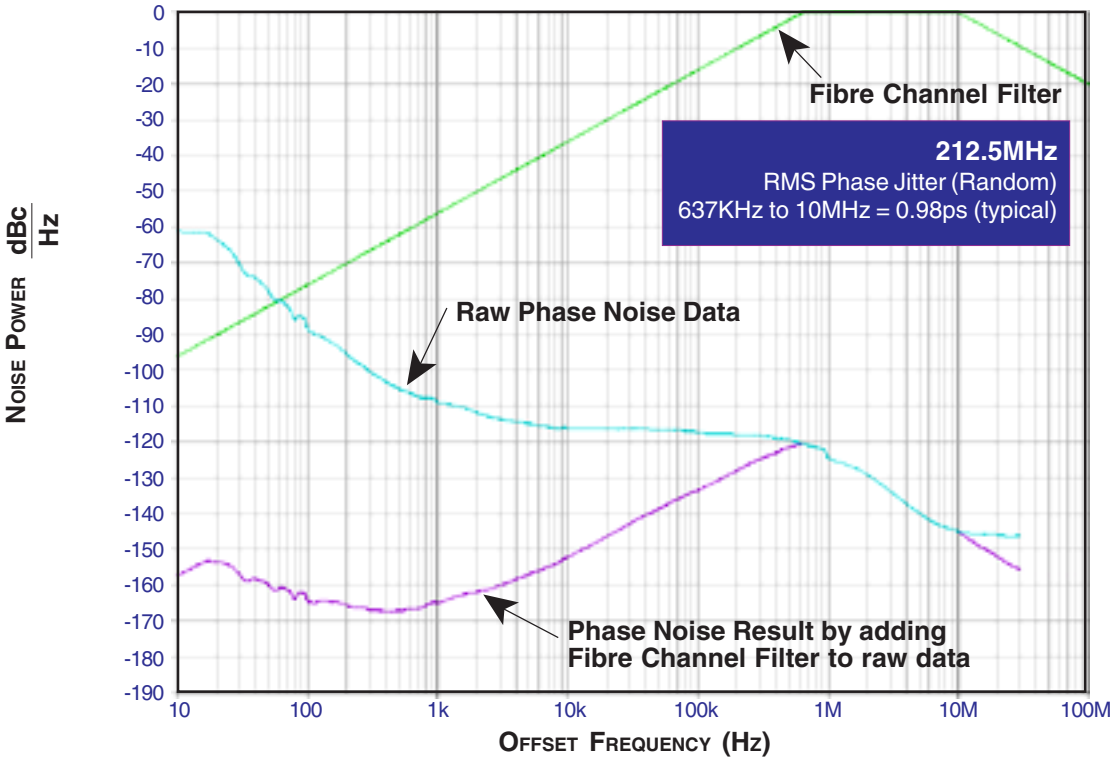
TYPICAL PHASE NOISE AT 159.375MHZ @3.3V



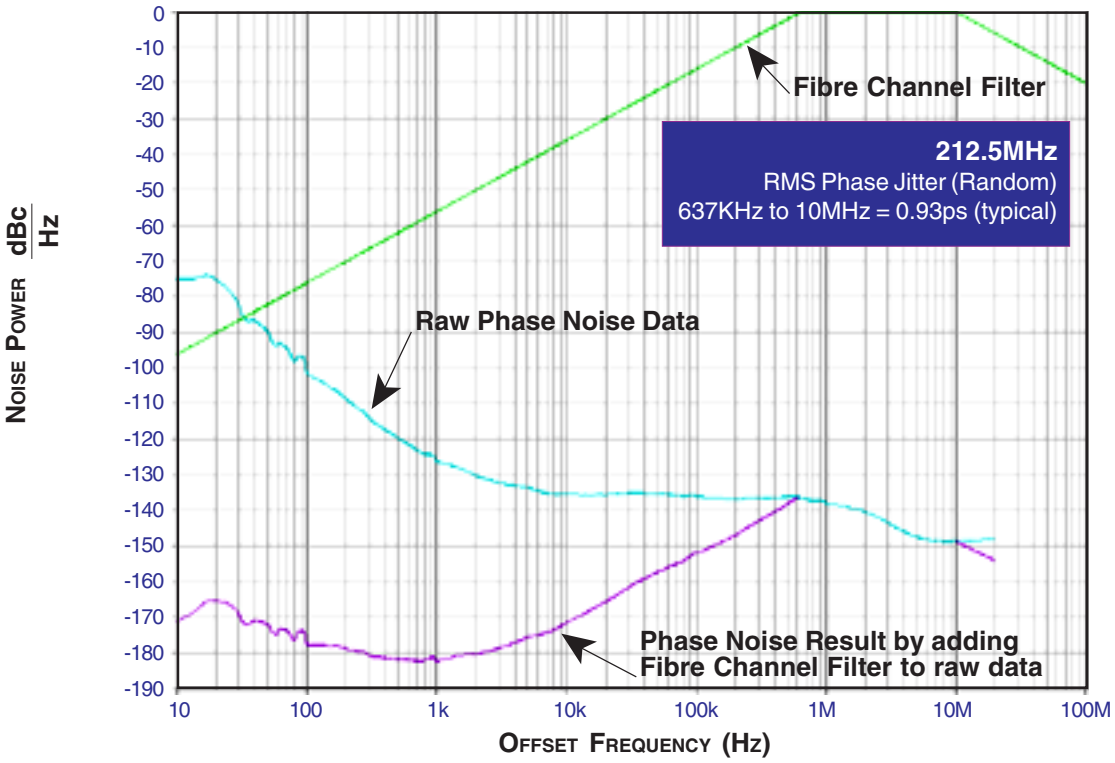
TYPICAL PHASE NOISE AT 159.375MHZ@ 2.5V



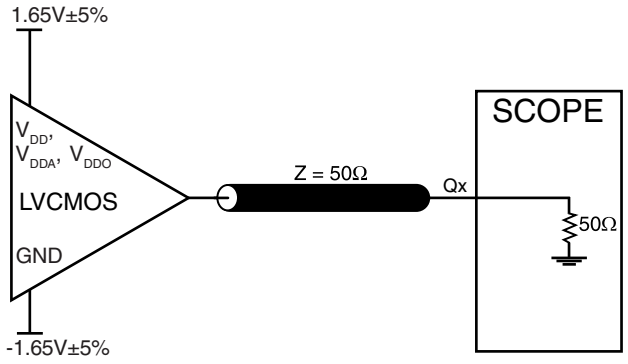
TYPICAL PHASE NOISE AT 212.5MHZ@ 3.3V



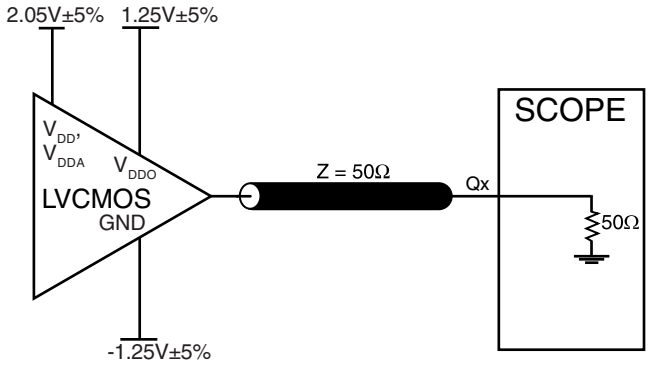
TYPICAL PHASE NOISE AT 212.5MHZ@ 2.5V



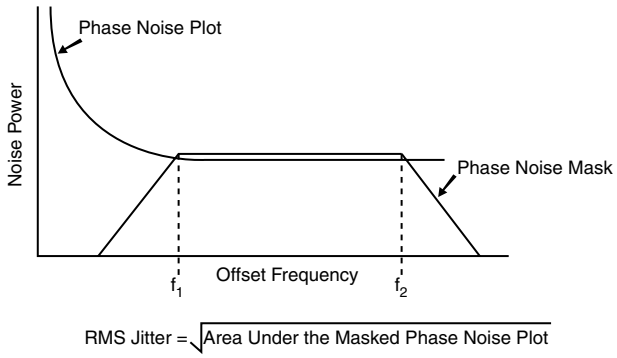
PARAMETER MEASUREMENT INFORMATION



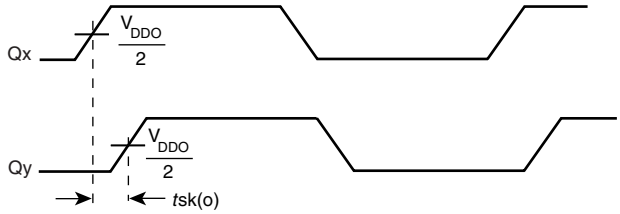
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



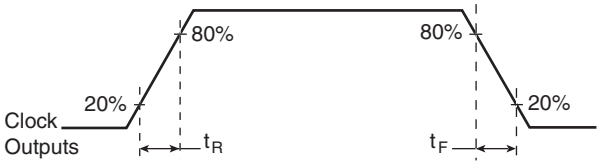
3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



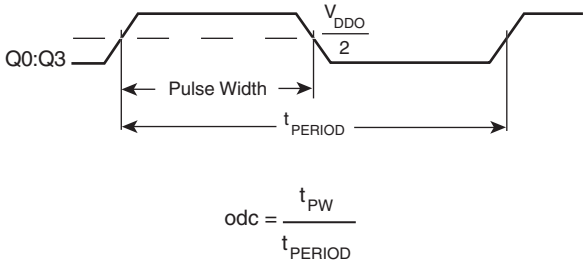
RMS PHASE JITTER



OUTPUT SKEW



OUTPUT RISE/FALL TIME



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS840004 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA}, and V_{DDO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{DDA}.

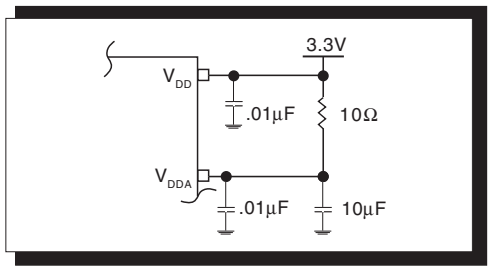


FIGURE 1. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The ICS840004 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using a 26.5625MHz 18pF parallel resonant crystal and were chosen to minimize the ppm error.

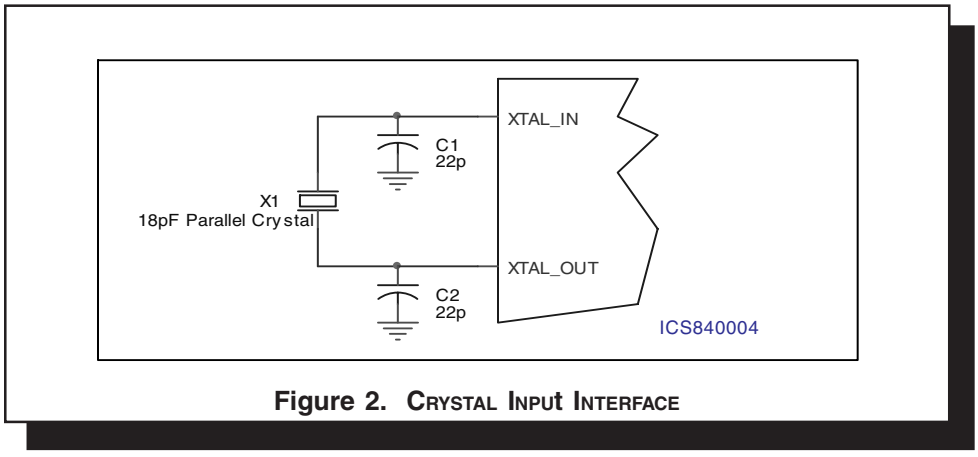


Figure 2. CRYSTAL INPUT INTERFACE

LAYOUT GUIDELINE

Figure 3 shows a schematic example of the ICS840004. An example of LVCMOS termination is shown in this schematic. Additional LVCMOS termination approaches are shown in the LVCMOS Termination Application Note. In this example, an 18 pF parallel resonant 26.5625MHz crystal is used. The C1=22pF and C2=22pF are recommended for frequency accuracy. For different board layout, the C1 and C2 may be slightly adjusted for optimizing frequency accuracy. 1KΩ pullup or pulldown resistors can be used for the logic control input pins.

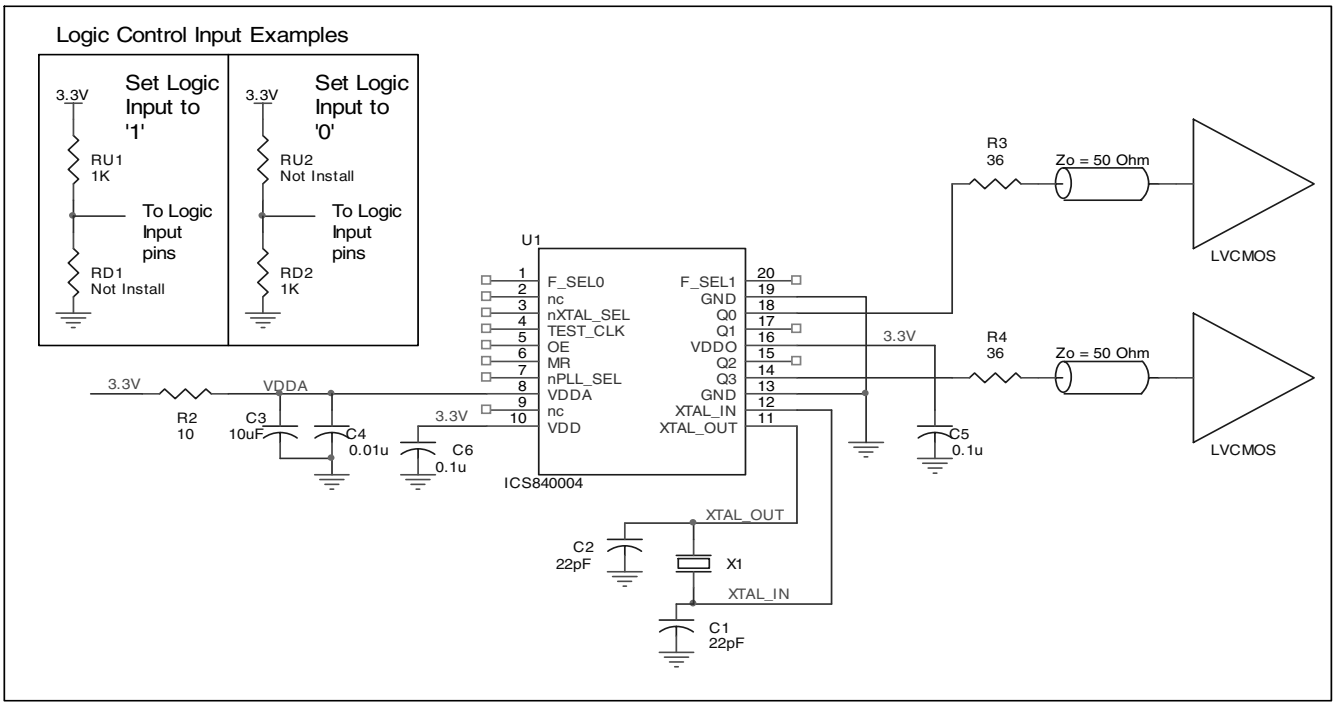


FIGURE 3. ICS840004 SCHEMATIC EXAMPLE

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE FOR 20 LEAD TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS840004 is: TBD

PACKAGE OUTLINE - G SUFFIX FOR 20 LEAD TSSOP

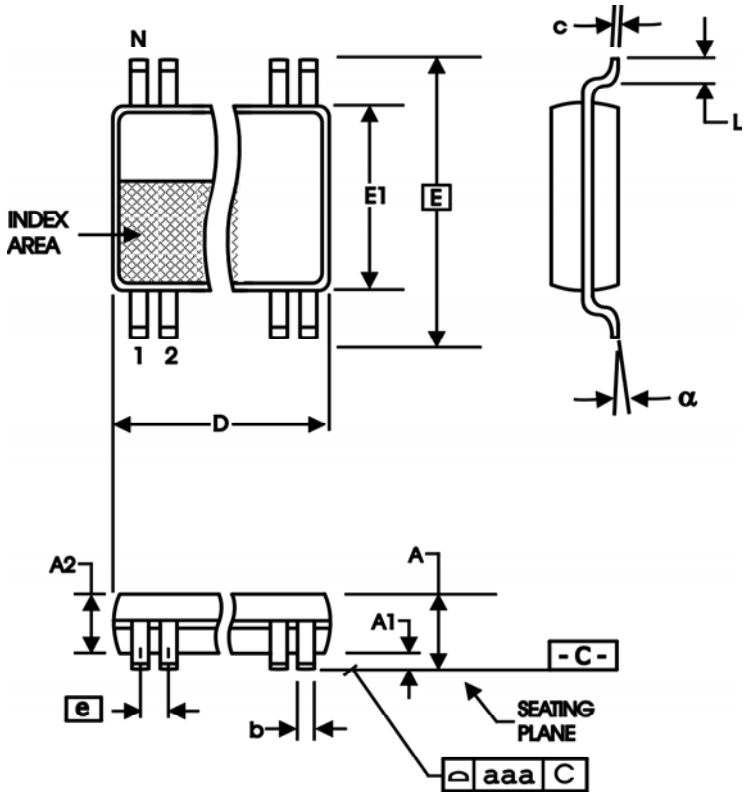


TABLE 7. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	MIN	MAX
N	20	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS840004AG	ICS840004AG	20 Lead TSSOP	72 per tube	0°C to 70°C
ICS840004AGT	ICS840004AG	20 Lead TSSOP on Tape and Reel	2500	0°C to 70°C