

# FEMTOCLOCKS™ CRYSTAL-TO-LVDS 400MHZ FREQUENCY SYNTHESIZER

## ICS844801I-24

### GENERAL DESCRIPTION



The ICS844801I-24 is a 400MHz Frequency Synthesizer and a member of the HiPerClocks™ family of high performance devices from IDT. The ICS844801I-24 uses an 18pF parallel resonant crystal over the range of 21.5625MHz - 25.3125MHz. The ICS844801I-24 has excellent <1ps phase jitter performance, over the 12kHz - 20MHz integration range. The ICS844801I-24 is packaged in a small 8-pin TSSOP, making it ideal for use in systems with limited board space.

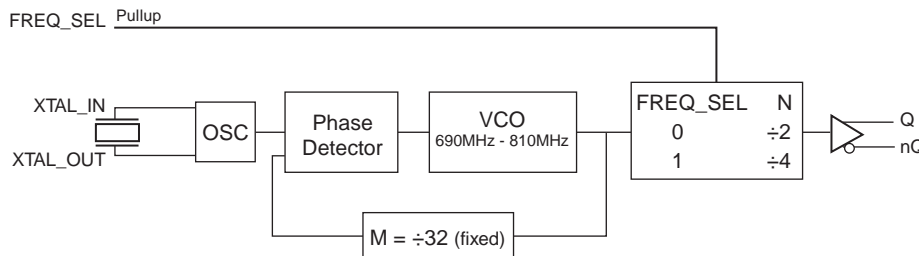
### FEATURES

- One differential LVDS output
- Crystal oscillator interface, 18pF parallel resonant crystal (21.5625MHz - 25.3125MHz)
- Output frequency range: 172.5MHz - 202.5MHz, and 345MHz - 405MHz
- VCO range: 690MHz - 810MHz
- RMS phase jitter @ 400MHz, using a 25MHz crystal (12kHz - 20MHz): 0.57ps (typical) @ 3.3V
- 3.3V or 2.5V operating supply
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

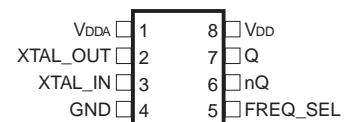
### COMMON CONFIGURATION TABLE

Crystal Frequency (MHz)	Inputs			Multiplication Value M/N	Output Frequency (MHz)
	FREQ_SEL	M	N		
25	0	32	2	16	400
25	1	32	4	8	200

### BLOCK DIAGRAM



### PIN ASSIGNMENT



### ICS844801I-24

8-Lead TSSOP

4.40mm x 3.0mm x 0.925mm  
package body  
**G Package**  
Top View

The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	V <sub>DDA</sub>	Power		Analog supply pin.
2, 3	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
4	GND	Power		Power supply ground.
5	FREQ_SEL	Input	Pullup	Frequency select pin. LVCMOS/LVTTL interface levels.
6, 7	nQ, Q	Output		Differential clock outputs. LVDS interface levels.
8	V <sub>DD</sub>	Power		Core supply pin.

NOTE: *Pullup* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
R <sub>PULLUP</sub>	Input Pullup Resistor			51		kΩ

## ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $V_{DD}$	4.6V
Inputs, $V_I$	-0.5V to $V_{DD} + 0.5V$
Outputs, $I_O$	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, $\theta_{JA}$	101.7°C/W (0 mps)
Storage Temperature, $T_{STG}$	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = V_{DDA} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$ 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Power Supply Voltage		3.135	3.3	3.465	V
$V_{DDA}$	Analog Supply Voltage		$V_{DD} - 0.07$	3.3	$V_{DD}$	V
$I_{DD}$	Power Supply Current			80		mA
$I_{DDA}$	Analog Supply Current			7		mA

TABLE 3B. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = V_{DDA} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$ 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Power Supply Voltage		2.375	2.5	2.625	V
$V_{DDA}$	Analog Supply Voltage		$V_{DD} - 0.07$	2.5	$V_{DD}$	V
$I_{DD}$	Power Supply Current			75		mA
$I_{DDA}$	Analog Supply Current			7		mA

TABLE 3C. LVCMOS/LVTTL DC CHARACTERISTICS,  $V_{DD} = V_{DDA} = 3.3V \pm 5\%$  OR  $2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$ 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage	$V_{DD} = 3.3V$	2		$V_{DD} + 0.3$	V
		$V_{DD} = 2.5V$	1.7		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage	$V_{DD} = 3.3V$	-0.3		0.8	V
		$V_{DD} = 2.5V$	-0.3		0.7	V
$I_{IH}$	Input High Current	$V_{DD} = V_{IN} = 3.465V$ or $2.625V$			5	$\mu\text{A}$
$I_{IL}$	Input Low Current	$V_{DD} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$	-150			$\mu\text{A}$

TABLE 3D. LVDS DC CHARACTERISTICS,  $V_{DD} = V_{DDA} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$ 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OD}$	Differential Output Voltage			415		mV
$\Delta V_{OD}$	$V_{OD}$ Magnitude Change			40		mV
$V_{OS}$	Offset Voltage			1.22		V
$\Delta V_{OS}$	$V_{OS}$ Magnitude Change			50		mV

NOTE: Please refer to Parameter Measurement Information for output information.

**TABLE 3D. LVDS DC CHARACTERISTICS,  $V_{DD} = V_{DDA} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OD}$	Differential Output Voltage			380		mV
$\Delta V_{OD}$	$V_{OD}$ Magnitude Change			40		mV
$V_{OS}$	Offset Voltage			1.17		V
$\Delta V_{OS}$	$V_{OS}$ Magnitude Change			50		mV

NOTE: Please refer to Parameter Measurement Information for output information.

**TABLE 4. CRYSTAL CHARACTERISTICS**

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		21.5625		25.3125	MHz
Equivalent Series Resistance (ESR)				50	$\Omega$
Shunt Capacitance				7	pF
Drive Level				1	mW

**TABLE 5A. AC CHARACTERISTICS,  $V_{DD} = V_{DDA} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$** 

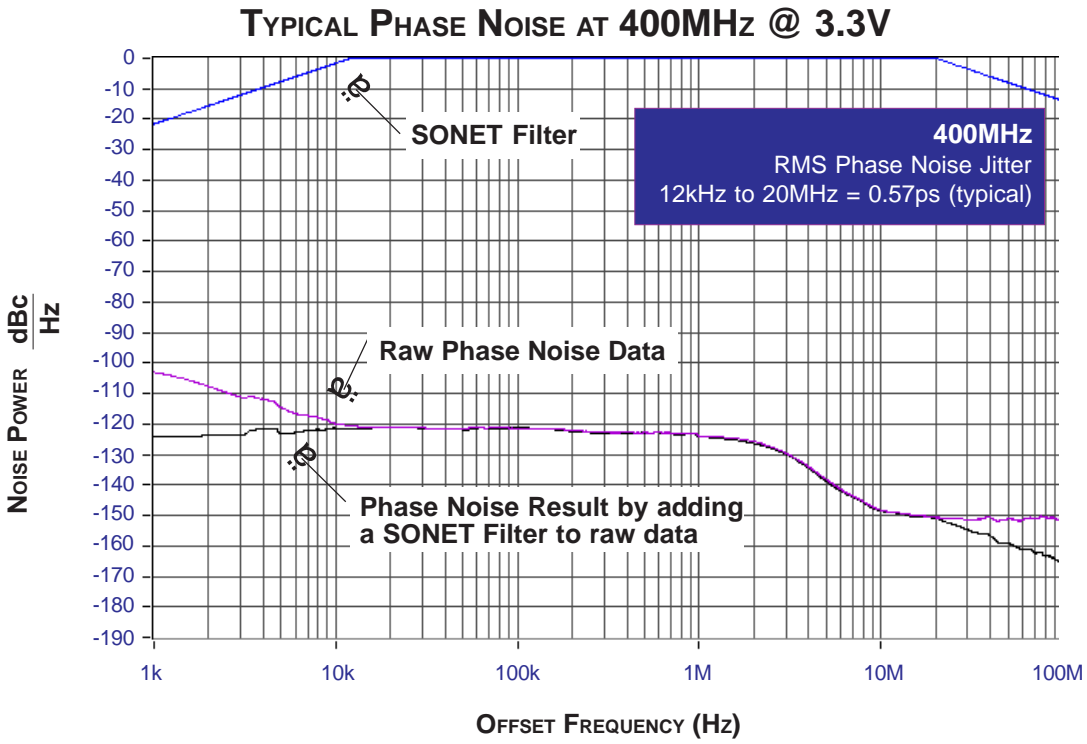
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency		172.5		202.5	MHz
			345		405	MHz
$f_{jit}(\emptyset)$	RMS Phase Jitter ( Random); NOTE 1	200MHz @ Integration Range: 12kHz - 20MHz		0.62		ps
		400MHz @ Integration Range: 12kHz - 20MHz		0.57		ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%		305		ps
odc	Output Duty Cycle			50		%

NOTE 1: Please refer to the Phase Noise Plots following this section.

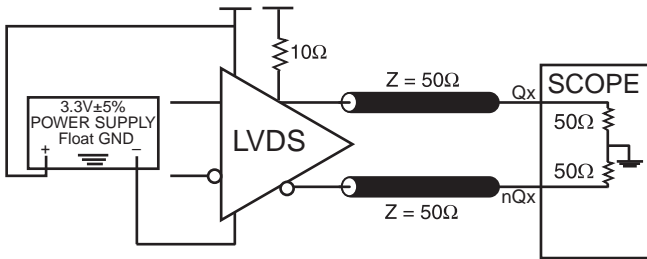
**TABLE 5B. AC CHARACTERISTICS,  $V_{DD} = V_{DDA} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency		172.5		202.5	MHz
			345		405	MHz
$f_{jit}(\emptyset)$	RMS Phase Jitter ( Random); NOTE 1	200MHz @ Integration Range: 12kHz - 20MHz		0.64		ps
		400MHz @ Integration Range: 12kHz - 20MHz		0.57		ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%		310		ps
odc	Output Duty Cycle			50		%

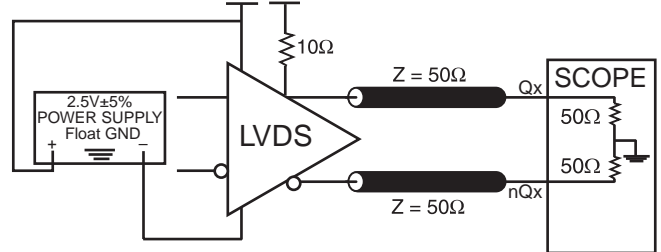
NOTE 1: Please refer to the Phase Noise Plots following this section.



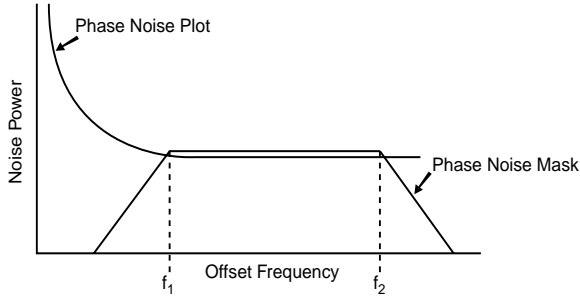
# PARAMETER MEASUREMENT INFORMATION



LVDS 3.3V OUTPUT LOAD AC TEST CIRCUIT

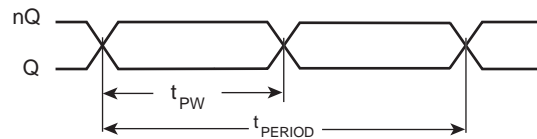


LVDS 2.5V OUTPUT LOAD AC TEST CIRCUIT



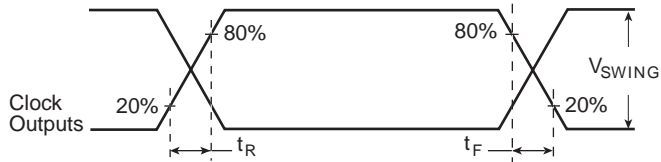
$$\text{RMS Jitter} = \sqrt{\text{Area Under the Masked Phase Noise Plot}}$$

RMS PHASE JITTER

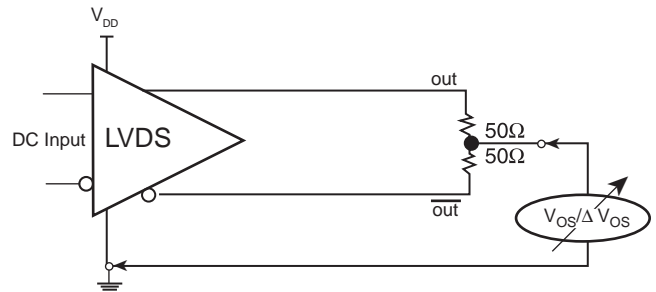


$$\text{odc} = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

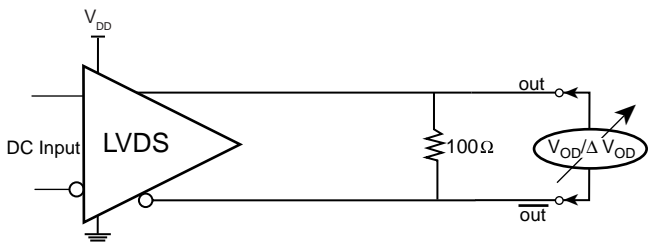
OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME



OFFSET VOLTAGE SETUP



DIFFERENTIAL OUTPUT VOLTAGE SETUP

## APPLICATION INFORMATION

### POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS844801I-24 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL.  $V_{DD}$  and  $V_{DDA}$  should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a  $10\Omega$  resistor along with a  $10\mu\text{F}$  and a  $.01\mu\text{F}$  bypass capacitor should be connected to each  $V_{DDA}$  pin. The  $10\Omega$  resistor can also be replaced by a ferrite bead.

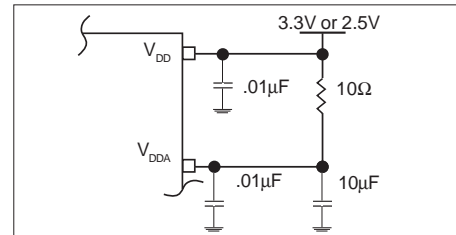


FIGURE 1. POWER SUPPLY FILTERING

### CRYSTAL INPUT INTERFACE

The ICS844801I-24 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 2* below were determined using a 25MHz, 18pF parallel

resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

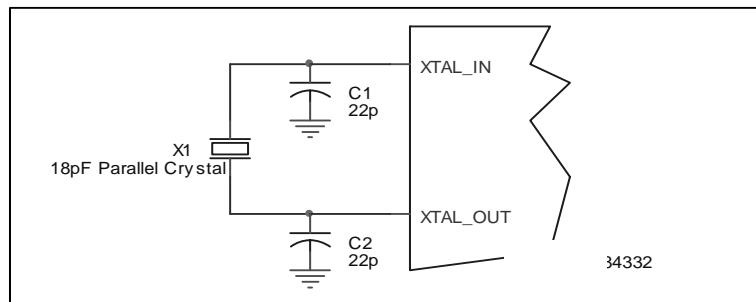


Figure 2. CRYSTAL INPUT INTERFACE

### LVC MOS TO XTAL INTERFACE

The XTAL\_IN input can accept a single-ended LVC MOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3*. The XTAL\_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVC MOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output

impedance of the driver ( $R_o$ ) plus the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First,  $R_1$  and  $R_2$  in parallel should equal the transmission line impedance. For most  $50\Omega$  applications,  $R_1$  and  $R_2$  can be  $100\Omega$ . This can also be accomplished by removing  $R_1$  and making  $R_2$   $50\Omega$ .

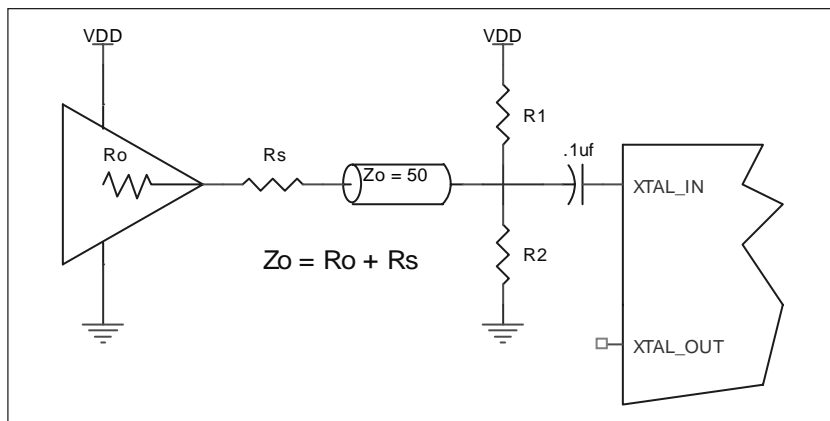


FIGURE 3. GENERAL DIAGRAM FOR LVC MOS DRIVER TO XTAL INPUT INTERFACE

### 3.3V, 2.5V LVDS DRIVER TERMINATION

A general LVDS interface is shown in *Figure 4*. In a  $100\Omega$  differential transmission line environment, LVDS drivers require a matched load termination of  $100\Omega$  across near

the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

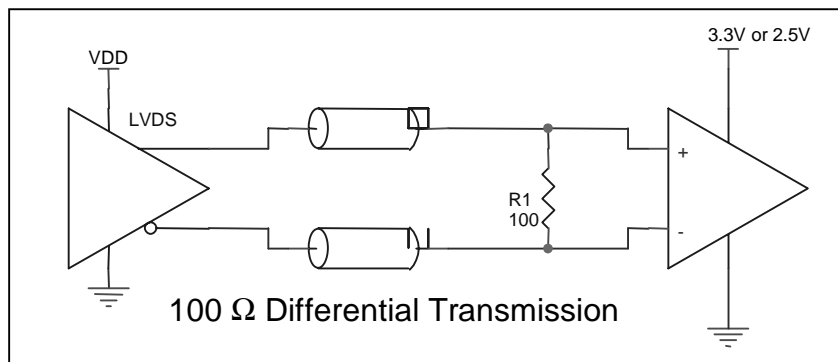


FIGURE 4. TYPICAL LVDS DRIVER TERMINATION



## POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS844801I-24. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS844801I-24 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{DD} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

$$\text{Power}_{\text{MAX}} = V_{DD\_MAX} * I_{DD\_MAX} = 3.465V * 80mA = \mathbf{277.2mW}$$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming a moderate air flow of 1 meter per second and a multi-layer board, the appropriate value is 90.5°C/W per Table 6 below.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:  
 $85^\circ\text{C} + 0.277\text{W} * 90.5^\circ\text{C}/\text{W} = 110.1^\circ\text{C}$ . This is well below the limit of 125°C.

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

**TABLE 6. THERMAL RESISTANCE  $\theta_{JA}$  FOR 8 LEAD TSSOP, FORCED CONVECTION**

$\theta_{JA}$ by Velocity (Meters per Second)			
	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	101.7°C/W	90.5°C/W	89.8°C/W

## RELIABILITY INFORMATION

TABLE 7.  $\theta_{JA}$  vs. AIR FLOW TABLE FOR 8 LEAD TSSOP

$\theta_{JA}$ by Velocity (Meters per Second)			
	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	101.7°C/W	90.5°C/W	89.8°C/W

### TRANSISTOR COUNT

The transistor count for ICS844801I-24 is: 1622

## PACKAGE OUTLINE - G SUFFIX FOR 8 LEAD TSSOP

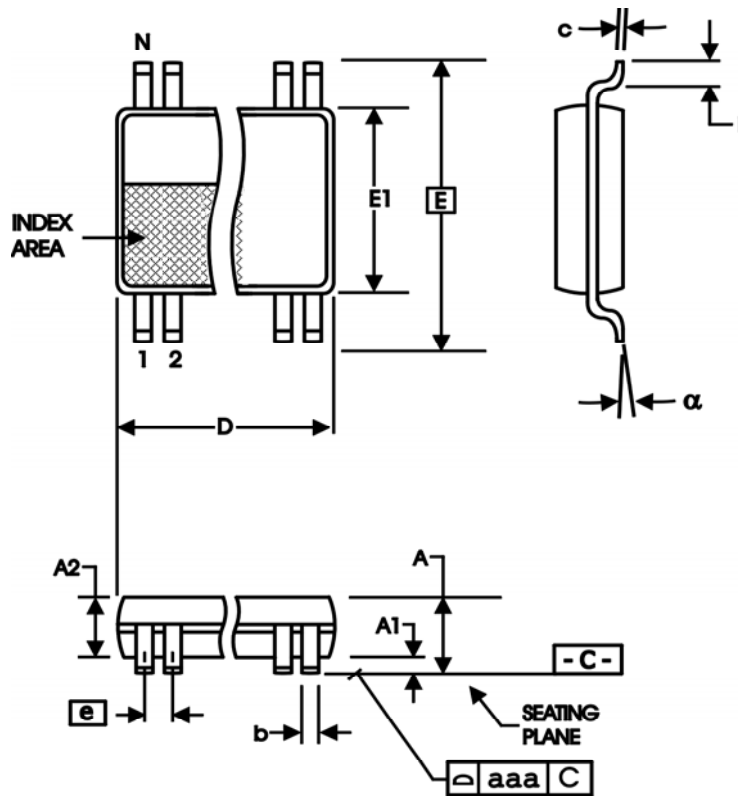


TABLE 8. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	8	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
$\alpha$	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS844801AGI-24	4AI24	8 Lead TSSOP	tube	-40°C to 85°C
ICS844801AGI-24T	4AI24	8 Lead TSSOP	2500 tape & reel	-40°C to 85°C
ICS844801AGI-24LF	AI24L	8 Lead "Lead-Free" TSSOP	tube	-40°C to 85°C
ICS844801AGI-24LFT	AI24L	8 Lead "Lead-Free" TSSOP	2500 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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