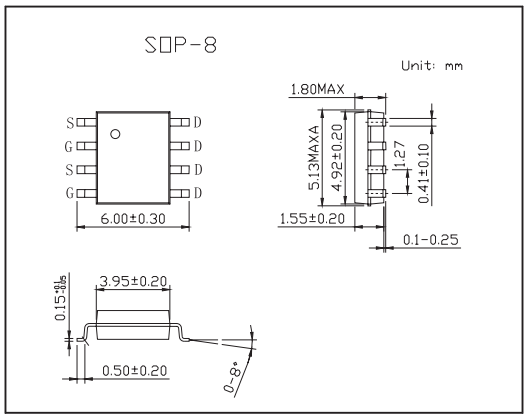
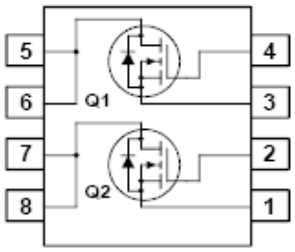
Dual N-Channel Logic Level PowerTrench MOSFET

KDS6910



■ Features

- 7.5 A, 30 V. $R_{DS(ON)}$ = 13mΩ @ V_{GS} = 10 V
  $R_{DS(ON)}$ = 17mΩ @ V_{GS} =4.5V
- Low gate charge
- Fast switching speed
- High performance trench technology for extremely low $R_{DS(ON)}$
- High power and current handling capability



■ Absolute Maximum Ratings Ta = 25℃

Parameter	Symbol	Rating	Unit
Drain to Source Voltage	V_{DSS}	30	V
Gate to Source Voltage	V_{GS}	±20	V
Drain Current Continuous (Note 1a)	I_D	7.5	A
Drain Current Pulsed		20	A
Power Dissipation for Single Operation (Note 1a)	P_D	1.6	W
Power Dissipation for Single Operation (Note 1b)		1	
Power Dissipation for Single Operation (Note 1c)		0.9	
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	℃
Thermal Resistance Junction to Case (Note 1)	$R_{\theta JC}$	40	℃/W
Thermal Resistance Junction to Ambient (Note 1a)	$R_{\theta JA}$	78	℃/W

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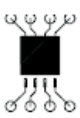
■ Electrical Characteristics Ta = 25℃

Parameter	Symbol	Testconditons	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	B_{VDSS}	V_{GS} = 0 V, I_D = 250 μA	30			V
Breakdown Voltage Temperature Coefficient	$\frac{\Delta BV_{DSS}}{\Delta T_J}$	I_D = 250 μA, Referenced to 25℃		28		mV/℃
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 24 V, V_{GS} = 0 V			1	μA
		V_{DS} = 24 V, V_{GS} = 0 V,T_J = 55℃			10	
Gate-Body Leakage, Forward	I_{GSSF}	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
Gate-Body Leakage, Reverse	I_{GSSR}	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	1	1.8	3	V
Gate Threshold Voltage Temperature Coefficient	$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	I_D = 250 μA, Referenced to 25℃		-4.7		mV/℃
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D =7.5 A		10.6	13	mΩ
		V_{GS} = 4.5 V, I_D = 6.5 A		13	17	
		V_{GS} = 10 V, I_D =7.5 A,TJ = 125℃		14.5	20	
On-State Drain Current	$I_{D(on)}$	V_{GS} = 10 V, V_{DS} = 5V	20			A
Forward Transconductance	g_{FS}	V_{DS} = 5 V, I_D = 7.5A		36		S
Input Capacitance	C_{iss}	V_{DS} = 15 V, V_{GS} = 0 V,f = 1.0 MHz		1130		pF
Output Capacitance	C_{oss}			300		pF
Reverse Transfer Capacitance	C_{rss}			100		pF
Gate Resistance	R_G	V_{GS} = 15 mV, f = 1.0 MHz		2.4		Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 15 V, I_D = 1 A,V_{GS} = 10 V, R_{GEN} = 6 Ω		9	18	ns
Turn-On Rise Time	tr			5	10	ns
Turn-Off Delay Time	$t_{d(off)}$			26	42	ns
Turn-Off Fall Time	tf			7	14	ns
Total Gate Charge at V_{gs}=10V	$Q_{g(TOT)}$	V_{DS} = 15 V, I_D = 7.5 A(Note 2)		17	24	nC
Total Gate Charge V_{gs}=5V	Q_g			9	13	nC
Gate-Source Charge	Q_{gs}			3.1		nC
Gate-Drain Charge	Q_{gd}			2.7		nC
Maximum Continuous Drain-Source Diode Forward Current	I_S				1.3	A
Drain-Source Diode Forward Voltage	V_{SD}	V_{GS} = 0 V, Is = 1.3 A (Not 2)			1.2	V
Diode Reverse Recovery Time	trr	I_F =7.5A		24		nS
Diode Reverse Recovery Charge	Qrr	d_{iF}/d_t = 100 A/μs		13		nC

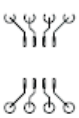
Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

a) 78°C/W when mounted on a 0.5in² pad of 2 oz copper



b) 125°C/W when mounted on a 0.02 in² pad of 2 oz copper



c) 135°C/W when mounted on a minimum mounting pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%