

# MC74HC238A

## 1-of-8 Decoder/ Demultiplexer

### High-Performance Silicon-Gate CMOS

The MC74HC238A is identical in pinout to the LS238. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC238A decodes a three-bit Address to one-of-eight active-high outputs. This device features three Chip Select inputs, two active-low and one active-high to facilitate the demultiplexing, cascading, and chip-selecting functions. The demultiplexing function is accomplished by using the Address inputs to select the desired device output; one of the Chip Selects is used as a data input while the other Chip Selects are held in their active states.

#### Features

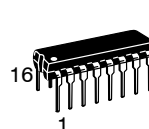
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 100 FETs or 29 Equivalent Gates
- These are Pb-Free Devices\*



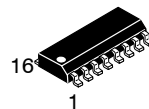
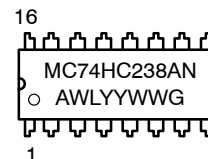
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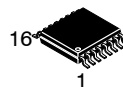
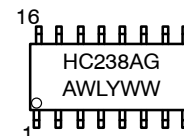
#### MARKING DIAGRAMS



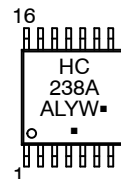
PDIP-16  
N SUFFIX  
CASE 648



SOIC-16  
D SUFFIX  
CASE 751B



TSSOP-16  
DT SUFFIX  
CASE 948F



A = Assembly Location  
WL, L = Wafer Lot  
YY, Y = Year  
WW, W = Work Week  
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# MC74HC238A

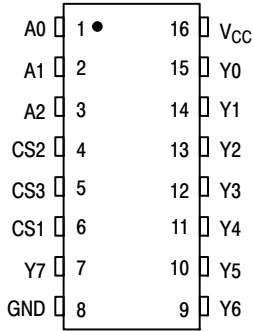


Figure 1. Pin Assignment

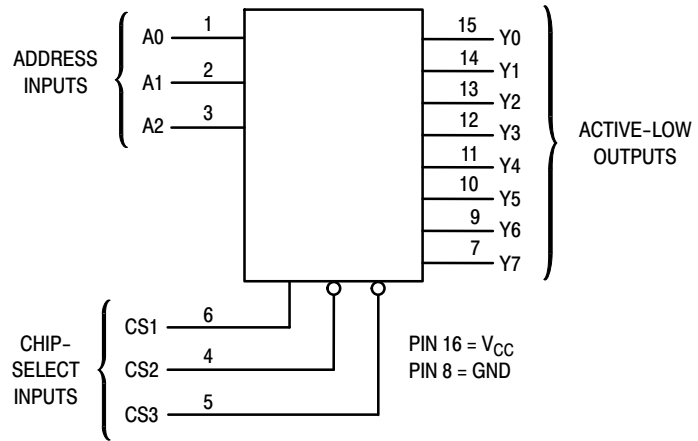


Figure 2. Logic Diagram

## ORDERING INFORMATION

| Device          | Package              | Shipping <sup>†</sup> |
|-----------------|----------------------|-----------------------|
| MC74HC238ANG    | PDIP-16<br>(Pb-Free) | 500 Units / Rail      |
| MC74HC238ADG    | SOIC-16<br>(Pb-Free) | 48 Units / Rail       |
| MC74HC238ADR2G  | SOIC-16<br>(Pb-Free) | 2500 Tape & Reel      |
| MC74HC238ADTR2G | TSSOP-16*            | 2500 Tape & Reel      |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*This package is inherently Pb-Free.

## TRUTH TABLE

| Inputs |     |     |    |    |    | Outputs |    |    |    |    |    |    |    |
|--------|-----|-----|----|----|----|---------|----|----|----|----|----|----|----|
| CS1    | CS2 | CS3 | A0 | A1 | A2 | Y0      | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |
| H      | X   | X   | X  | X  | X  | L       | L  | L  | L  | L  | L  | L  | L  |
| X      | H   | X   | X  | X  | X  | L       | L  | L  | L  | L  | L  | L  | L  |
| X      | X   | L   | X  | X  | X  | L       | L  | L  | L  | L  | L  | L  | L  |
| L      | L   | H   | L  | L  | L  | H       | L  | L  | L  | L  | L  | L  | L  |
| L      | L   | H   | H  | L  | L  | L       | H  | L  | L  | L  | L  | L  | L  |
| L      | L   | H   | L  | H  | L  | L       | L  | H  | L  | L  | L  | L  | L  |
| L      | L   | H   | H  | H  | L  | L       | L  | L  | H  | L  | L  | L  | L  |
| L      | L   | H   | L  | L  | H  | L       | L  | L  | L  | H  | L  | L  | L  |
| L      | L   | H   | H  | L  | H  | L       | L  | L  | L  | L  | H  | L  | L  |
| L      | L   | H   | L  | H  | H  | L       | L  | L  | L  | L  | L  | H  | L  |
| L      | L   | H   | H  | H  | H  | L       | L  | L  | L  | L  | L  | L  | H  |

# MC74HC238A

## MAXIMUM RATINGS

| Symbol    | Parameter   | Value                   | Unit |
|-----------|---|-------------------------|------|
| $V_{CC}$  | DC Supply Voltage (Referenced to GND)   | - 0.5 to + 7.0          | V    |
| $V_{in}$  | DC Input Voltage (Referenced to GND)  | - 0.5 to $V_{CC} + 0.5$ | V    |
| $V_{out}$ | DC Output Voltage (Referenced to GND)   | - 0.5 to $V_{CC} + 0.5$ | V    |
| $I_{in}$  | DC Input Current, per Pin   | $\pm 20$                | mA   |
| $I_{out}$ | DC Output Current, per Pin  | $\pm 25$                | mA   |
| $I_{CC}$  | DC Supply Current, $V_{CC}$ and GND Pins  | $\pm 50$                | mA   |
| $P_D$     | Power Dissipation in Still Air,<br>Plastic DIP†<br>SOIC Package†<br>TSSOP Package†      | 750<br>500<br>450       | mW   |
| $T_{stg}$ | Storage Temperature   | - 65 to + 150           | °C   |
| $T_L$     | Lead Temperature, 1 mm from Case for 10 Seconds<br>(Plastic DIP, SOIC or TSSOP Package) | 260                     | °C   |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

†Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C  
SOIC Package: - 7 mW/°C from 65° to 125°C  
TSSOP Package: - 6.1 .W/°C from 65° to 125°C

## RECOMMENDED OPERATING CONDITIONS

| Symbol            | Parameter  | Min  | Max      | Unit |
|-------------------|--|------|----------|------|
| $V_{CC}$          | DC Supply Voltage (Referenced to GND)                | 2.0  | 6.0      | V    |
| $V_{in}, V_{out}$ | DC Input Voltage, Output Voltage (Referenced to GND) | 0    | $V_{CC}$ | V    |
| $T_A$             | Operating Temperature, All Package Types             | - 55 | + 125    | °C   |
| $t_r, t_f$        | Input Rise and Fall Time<br>(Figure 2)               |      |          | ns   |
|                   | $V_{CC} = 2.0 \text{ V}$                             | 0    | 1000     |      |
|                   | $V_{CC} = 4.5 \text{ V}$                             | 0    | 500      |      |
|                   | $V_{CC} = 6.0 \text{ V}$                             | 0    | 400      |      |

# MC74HC238A

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol          | Parameter                         | Test Conditions  | V <sub>CC</sub><br>V | Guaranteed Limit |        |         | Unit |
|-----------------|-----------------------------------|--|----------------------|------------------|--------|---------|------|
|                 |                                   |  |                      | -55°C to 25°C    | ≤ 85°C | ≤ 125°C |      |
| V <sub>IH</sub> | Minimum High-Level Input Voltage  | V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V<br> I <sub>out</sub>   ≤ 20 μA   | 2.0                  | 1.5              | 1.5    | 1.5     | V    |
|                 |                                   |  | 3.0                  | 2.1              | 2.1    | 2.1     |      |
|                 |                                   |  | 4.5                  | 3.15             | 3.15   | 3.15    |      |
|                 |                                   |  | 6.0                  | 4.2              | 4.2    | 4.2     |      |
| V <sub>IL</sub> | Maximum Low-Level Input Voltage   | V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V<br> I <sub>out</sub>   ≤ 20 μA   | 2.0                  | 0.5              | 0.5    | 0.5     | V    |
|                 |                                   |  | 3.0                  | 0.9              | 0.9    | 0.9     |      |
|                 |                                   |  | 4.5                  | 1.35             | 1.35   | 1.35    |      |
|                 |                                   |  | 6.0                  | 1.8              | 1.8    | 1.8     |      |
| V <sub>OH</sub> | Minimum High-Level Output Voltage | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 20 μA  | 2.0                  | 1.9              | 1.9    | 1.9     | V    |
|                 |                                   |  | 4.5                  | 4.4              | 4.4    | 4.4     |      |
|                 |                                   |  | 6.0                  | 5.9              | 5.9    | 5.9     |      |
|                 |                                   | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 2.4 mA<br> I <sub>out</sub>   ≤ 4.0 mA<br> I <sub>out</sub>   ≤ 5.2 mA | 3.0                  | 2.48             | 2.34   | 2.20    |      |
|                 |                                   |  | 4.5                  | 3.98             | 3.84   | 3.70    |      |
|                 |                                   |  | 6.0                  | 5.48             | 5.34   | 5.20    |      |

|                 |  |  |     |       |       |       |    |
|-----------------|--|--|-----|-------|-------|-------|----|
| V <sub>OL</sub> | Maximum Low-Level Output Voltage               | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 20 μA  | 2.0 | 0.1   | 0.1   | 0.1   | V  |
|                 |  |  | 4.5 | 0.1   | 0.1   | 0.1   |    |
|                 |  |  | 6.0 | 0.1   | 0.1   | 0.1   |    |
|                 |  | V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub><br> I <sub>out</sub>   ≤ 2.4 mA<br> I <sub>out</sub>   ≤ 4.0 mA<br> I <sub>out</sub>   ≤ 5.2 mA | 3.0 | 0.26  | 0.33  | 0.40  |    |
|                 |  |  | 4.5 | 0.26  | 0.33  | 0.40  |    |
|                 |  |  | 6.0 | 0.26  | 0.33  | 0.40  |    |
| I <sub>in</sub> | Maximum Input Leakage Current                  | V <sub>in</sub> = V <sub>CC</sub> or GND   | 6.0 | ± 0.1 | ± 1.0 | ± 1.0 | μA |
| I <sub>CC</sub> | Maximum Quiescent Supply Current (per Package) | V <sub>in</sub> = V <sub>CC</sub> or GND<br>I <sub>out</sub> = 0 μA  | 6.0 | 4     | 40    | 160   | μA |

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6.0 ns)

| Symbol                                 | Parameter  | V <sub>CC</sub><br>V | Guaranteed Limit |        |         | Unit |
|--|--|----------------------|------------------|--------|---------|------|
|  |  |                      | -55°C to 25°C    | ≤ 85°C | ≤ 125°C |      |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Maximum Propagation Delay, Input A to Output Y<br>(Figures 3 and 6)    | 2.0                  | 135              | 170    | 205     | ns   |
|  |  | 3.0                  | 90               | 125    | 165     |      |
|  |  | 4.5                  | 27               | 34     | 41      |      |
|  |  | 6.0                  | 23               | 29     | 35      |      |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Maximum Propagation Delay, CS1 to Output Y<br>(Figures 4 and 6)        | 2.0                  | 110              | 140    | 165     | ns   |
|  |  | 3.0                  | 85               | 100    | 125     |      |
|  |  | 4.5                  | 22               | 28     | 33      |      |
|  |  | 6.0                  | 19               | 24     | 28      |      |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Maximum Propagation Delay, CS2 or CS3 to Output Y<br>(Figures 5 and 6) | 2.0                  | 120              | 150    | 180     | ns   |
|  |  | 3.0                  | 90               | 120    | 150     |      |
|  |  | 4.5                  | 24               | 30     | 36      |      |
|  |  | 6.0                  | 20               | 26     | 31      |      |
| t <sub>TLH</sub> ,<br>t <sub>THL</sub> | Maximum Output Transition Time, Any Output<br>(Figures 4 and 6)        | 2.0                  | 75               | 95     | 110     | ns   |
|  |  | 3.0                  | 30               | 40     | 55      |      |
|  |  | 4.5                  | 15               | 19     | 22      |      |
|  |  | 6.0                  | 13               | 16     | 19      |      |
| C <sub>in</sub>                        | Maximum Input Capacitance  | -                    | 10               | 10     | 10      | pF   |

|                 |  |   |  |  |    |
|-----------------|--|---|--|--|----|
| C <sub>PD</sub> | Power Dissipation Capacitance (Per Package)* | Typical @ 25°C, V <sub>CC</sub> = 5.0 V |  |  | pF |
|                 |  | 55                                      |  |  |    |

\* Used to determine the no-load dynamic power consumption: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup>f + I<sub>CC</sub> V<sub>CC</sub>.

# MC74HC238A

## SWITCHING WAVEFORMS

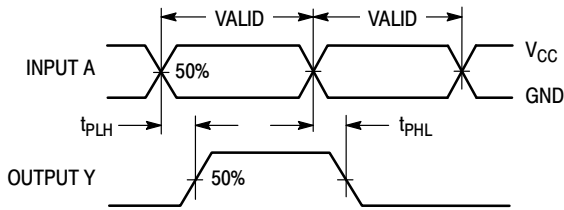


Figure 3.

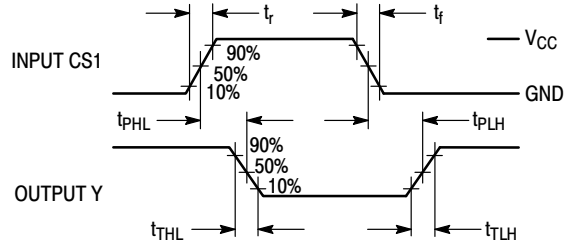


Figure 4.

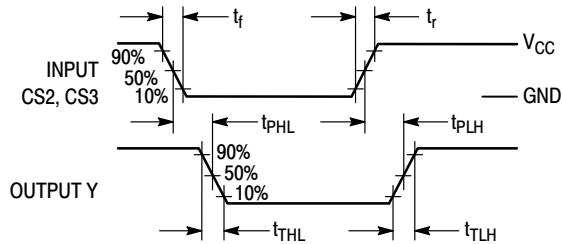
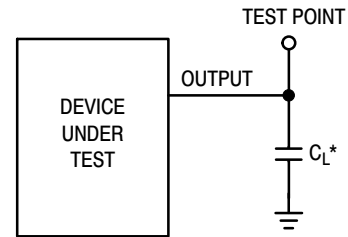


Figure 5.



\*Includes all probe and jig capacitance

Figure 6. Test Circuit

## PIN DESCRIPTIONS

### ADDRESS INPUTS

#### A0, A1, A2 (Pins 1, 2, 3)

Address inputs. These inputs, when the chip is selected, determine which of the eight outputs is active-low.

### CONTROL INPUTS

#### CS1, CS2, CS3 (Pins 6, 4, 5)

Chip select inputs. For CS1 at a high level and CS2, CS3 at a low level, the chip is selected and the outputs follow the

Address inputs. For any other combination of CS1, CS2, and CS3, the outputs are at a logic high.

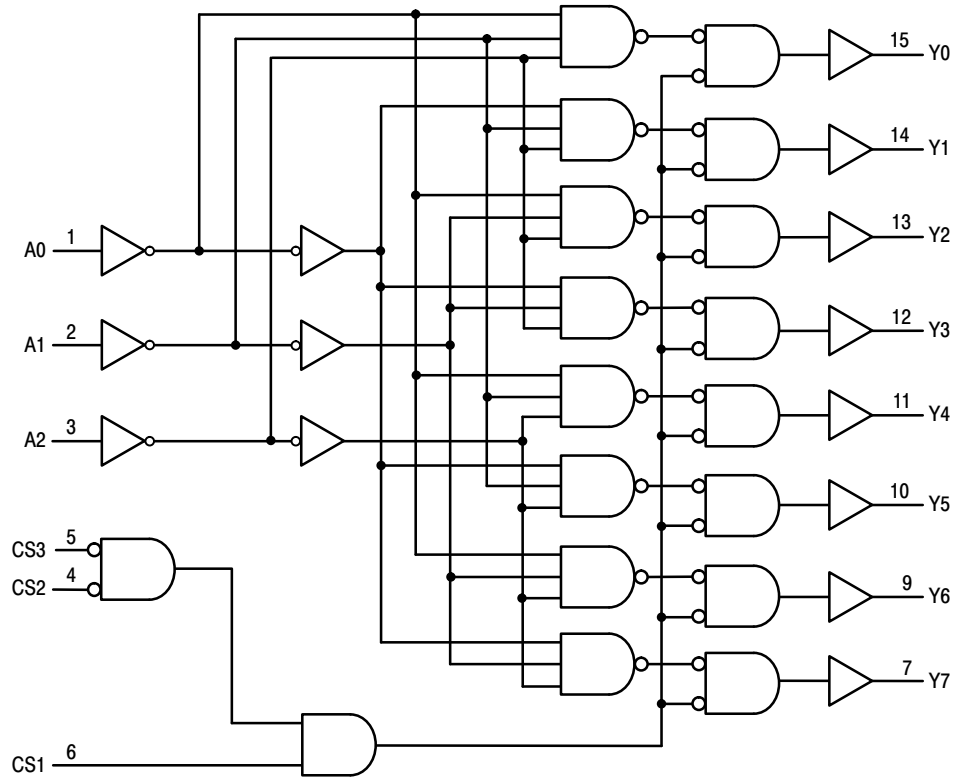
### OUTPUTS

#### Y0 - Y7 (Pins 15, 14, 13, 12, 11, 10, 9, 7)

Active-high Decoded outputs. These outputs assume a high level when addressed and the chip is selected. These outputs remain low when not addressed or the chip is not selected.

# MC74HC238A

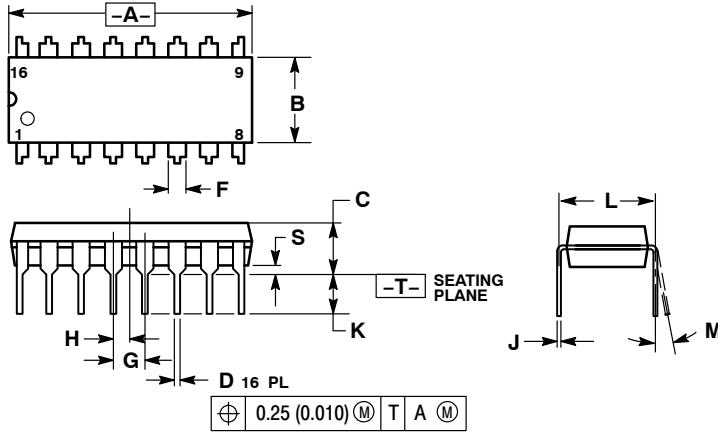
## EXPANDED LOGIC DIAGRAM



# MC74HC238A

## PACKAGE DIMENSIONS

PDIP-16  
N SUFFIX  
CASE 648-08  
ISSUE T

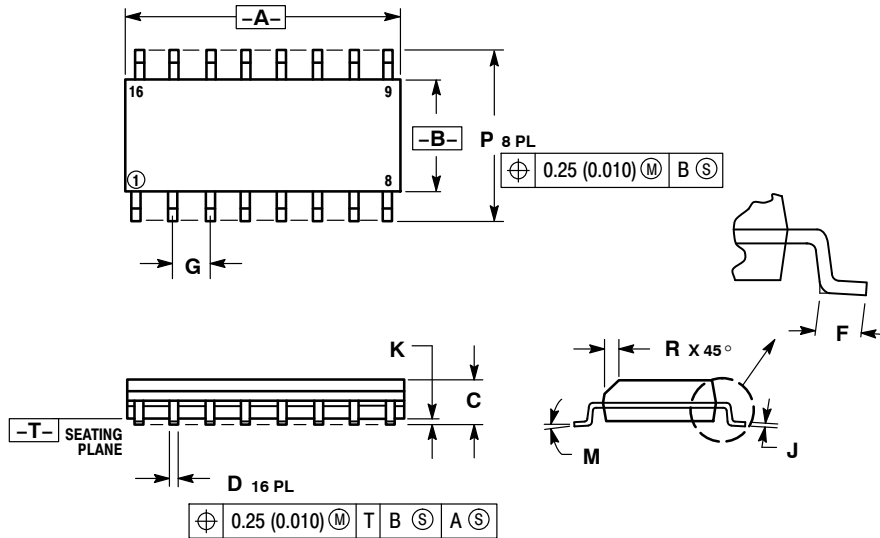


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

| DIM | INCHES    |       | MILLIMETERS |       |
|-----|-----------|-------|-------------|-------|
|     | MIN       | MAX   | MIN         | MAX   |
| A   | 0.740     | 0.770 | 18.80       | 19.55 |
| B   | 0.250     | 0.270 | 6.35        | 6.85  |
| C   | 0.145     | 0.175 | 3.69        | 4.44  |
| D   | 0.015     | 0.021 | 0.39        | 0.53  |
| F   | 0.040     | 0.70  | 1.02        | 1.77  |
| G   | 0.100 BSC |       | 2.54 BSC    |       |
| H   | 0.050 BSC |       | 1.27 BSC    |       |
| J   | 0.008     | 0.015 | 0.21        | 0.38  |
| K   | 0.110     | 0.130 | 2.80        | 3.30  |
| L   | 0.295     | 0.305 | 7.50        | 7.74  |
| M   | 0°        | 10°   | 0°          | 10°   |
| S   | 0.020     | 0.040 | 0.51        | 1.01  |

SOIC-16  
D SUFFIX  
CASE 751B-05  
ISSUE J



NOTES:

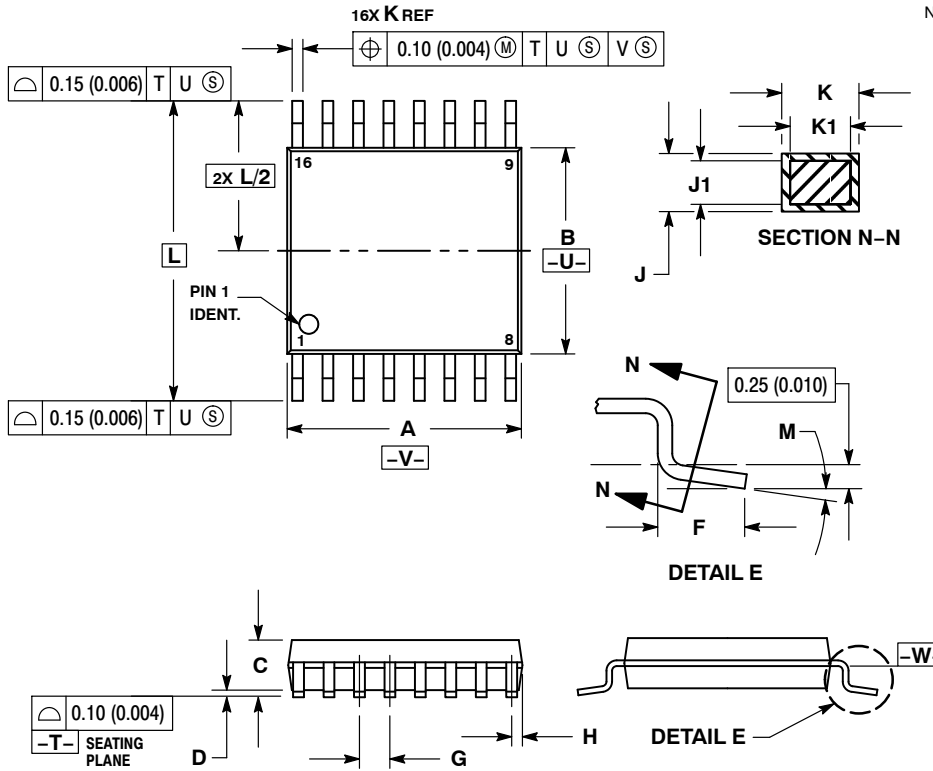
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS |       | INCHES    |       |
|-----|-------------|-------|-----------|-------|
|     | MIN         | MAX   | MIN       | MAX   |
| A   | 9.80        | 10.00 | 0.386     | 0.393 |
| B   | 3.80        | 4.00  | 0.150     | 0.157 |
| C   | 1.35        | 1.75  | 0.054     | 0.068 |
| D   | 0.35        | 0.49  | 0.014     | 0.019 |
| F   | 0.40        | 1.25  | 0.016     | 0.049 |
| G   | 1.27 BSC    |       | 0.050 BSC |       |
| J   | 0.19        | 0.25  | 0.008     | 0.009 |
| K   | 0.10        | 0.25  | 0.004     | 0.009 |
| M   | 0°          | 7°    | 0°        | 7°    |
| P   | 5.80        | 6.20  | 0.229     | 0.244 |
| R   | 0.25        | 0.50  | 0.010     | 0.019 |

# MC74HC238A

## PACKAGE DIMENSIONS

TSSOP-16  
DT SUFFIX  
CASE 948F-01  
ISSUE A



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.90        | 5.10 | 0.193     | 0.200 |
| B   | 4.30        | 4.50 | 0.169     | 0.177 |
| C   | ---         | 1.20 | ---       | 0.047 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.50        | 0.75 | 0.020     | 0.030 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| H   | 0.18        | 0.28 | 0.007     | 0.011 |
| J   | 0.09        | 0.20 | 0.004     | 0.008 |
| J1  | 0.09        | 0.16 | 0.004     | 0.006 |
| K   | 0.19        | 0.30 | 0.007     | 0.012 |
| K1  | 0.19        | 0.25 | 0.007     | 0.010 |
| L   | 6.40 BSC    |      | 0.252 BSC |       |
| M   | 0°          | 8°   | 0°        | 8°    |

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