LANSDALE
Semiconductor, Inc.

ML145554 ML145564
ML145557 ML145567
PCM Codec–Filter

Legacy Device: *Motorola MC145554, MC145557, MC145564, MC145567*

The ML145554, ML145557, ML145564, and ML145567 are all per channel PCM Codec–Filters. These devices perform the voice digitization and reconstruction as well as the band limiting and smoothing required for PCM systems. They are designed to operate in both synchronous and asynchronous applications and contain an on–chip precision voltage reference. The ML145554 (Mu–Law) and ML145557 (A–Law) are general purpose devices that are offered in 16–pin packages. The ML145564 (Mu–Law) and ML145567 (A–Law), offered in 20–pin packages, add the capability of analog loopback and push–pull power amplifiers with adjustable gain.

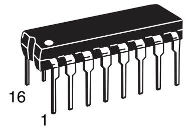
These devices have an input operational amplifier whose output is the input to the encoder section. The encoder section immediately low–pass filters the analog signal with an active R–C filter to eliminate very–high–frequency noise from being modulated down to the pass band by the switched capacitor filter. From the active R–C filter, the analog signal is converted to a differential signal. From this point, all analog signal processing is done differentially. This allows processing of an analog signal that is twice the amplitude allowed by a single–ended design, which reduces the significance of noise to both the inverted and non–inverted signal paths. Another advantage of this differential design is that noise injected via the power supplies is a common–mode signal that is cancelled when the inverted and non–inverted signals are recombined. This dramatically improves the power supply rejection ratio.

After the differential converter, a differential switched capacitor filter bandpasses the analog signal from 200 Hz to 3400 Hz before the signal is digitized by the differential compressing A/D converter.

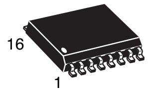
The decoder accepts PCM data and expands it using a differential D/A converter. The output of the D/A is low–pass filtered at 3400 Hz and sinX/X compensated by a differential switched capacitor filter. The signal is then filtered by an active R–C filter to eliminate the out–of–band energy of the switched capacitor filter.

These PCM Codec–Filters accept both long–frame and short–frame industry standard clock formats. They also maintain compatibility with Motorola’s family of TSACs and MC3419/MC34120 SLIC products.

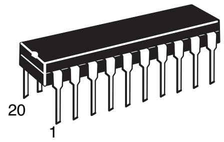
The ML145554/57/64/67 family of PCM Codec–Filters utilizes CMOS due to its reliable low–power performance and proven capability for complex analog/digital VLSI functions.



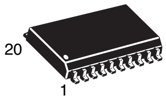
P DIP 16 = EP
PLASTIC DIP
CASE 648
ML145554/57



SOG 16 = -5P
SOG PACKAGE
CASE 751G
ML145554/57



P DIP 20 = RP
PLASTIC DIP
CASE 738
ML145564/67



SOG 20 = -6P
SOG PACKAGE
CASE 751D
ML145564/67

CROSS REFERENCE/ORDERING INFORMATION

PACKAGE	MOTOROLA	LANSDALE
P DIP 16	MC145554P	ML145554EP
SO 16W	MC145554DW	ML145554-5P
P DIP 16	MC145557P	ML145557EP
SO 16W	MC145557DW	ML145557-5P
P DIP 20	MC145564P	ML145564RP
SO 20W	MC145564DW	ML145564-6P
P DIP 20	MC145567P	ML145567RP
SO 20W	MC145567DW	ML145567-6P

Note: Lansdale lead free (**Pb**) product, as it becomes available, will be identified by a part number prefix change from **ML** to **MLE**.

FEATURES

ML145554/57(16–Pin Package)

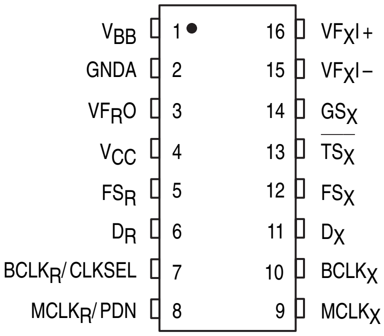
- Fully Differential Analog Circuit Design for Lowest Noise
- Performance Specified for Extended Temperature Range of – 40 to + 85°C
- Transmit Band–Pass and Receive Low–Pass Filters On–Chip
- Active R–C Pre–Filtering and Post–Filtering
- Mu–Law Companding ML145554
- A–Law Companding ML145557
- On–Chip Precision Voltage Reference (2.5 V)
- Typical Power Dissipation of 40 mW, Power Down of 1.0 mW at ±5 V

ML145564/67(20–Pin Package) — All of the Features of the ML145554/57 Plus:

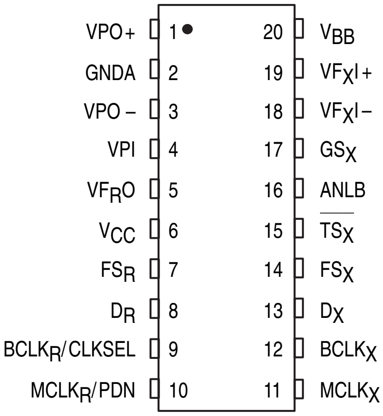
- Mu–Law Companding ML145564
- A–Law Companding ML145567
- Push–Pull Power Drivers with External Gain Adjust
- Analog Loopback

PIN ASSIGNMENTS

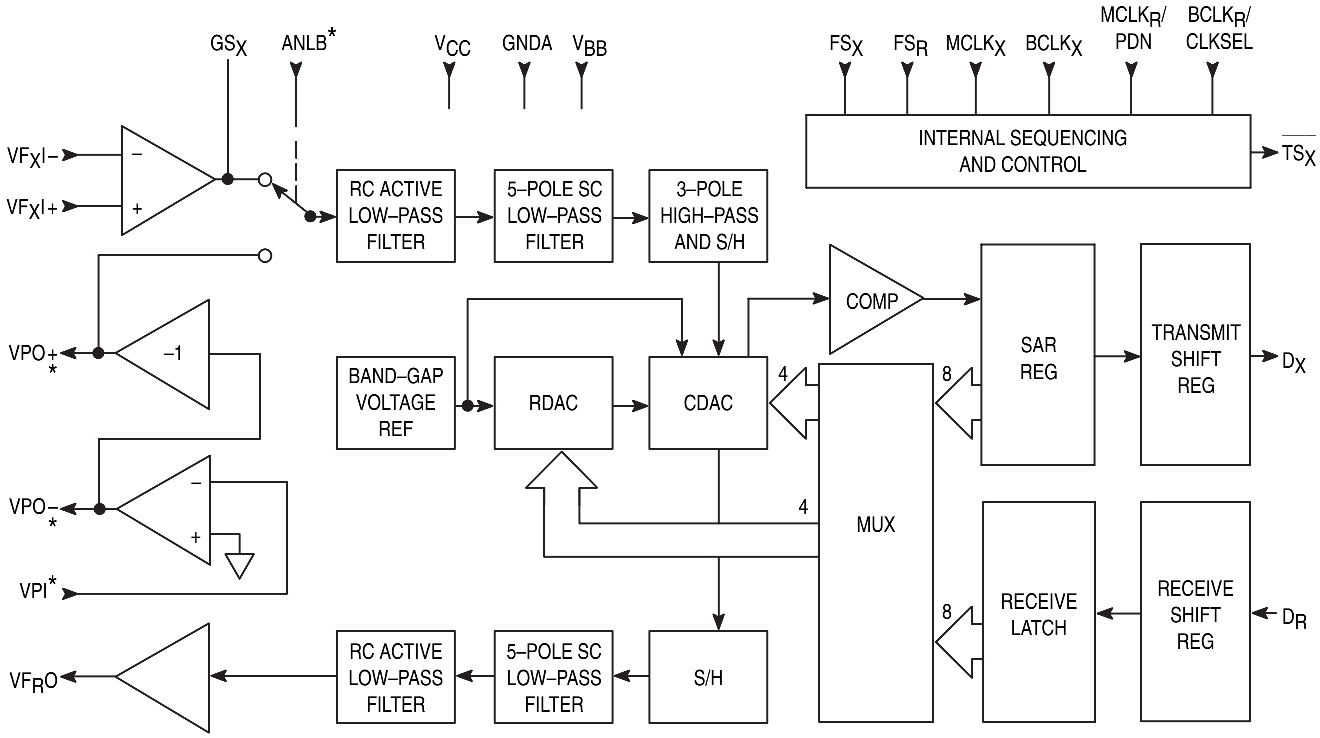
ML145554, ML145557



ML145564, ML145567



FUNCTIONAL BLOCK DIAGRAM



* ML145564 and ML145567 only.

DEVICE DESCRIPTION

A codec–filter is used for digitizing and reconstructing thehuman voice. These devices were developed primarily for the telephone network to facilitate voice switching and transmission. Once the voice is digitized, it may be switched by digital switching methods or transmitted long distance (T1, microwave, satellites, etc.) without degradation. The name codec is an acronym from "COder" (for the A/D used to digitize voice) and "DECoder" (for the D/A used for reconstructing voice). A codec is a single device that does both the A/D and D/A conversions.

To digitize intelligible voice requires a signal–to–distortion ratio of about 30 dB over a dynamic range of about 40 dB. This can be accomplished with a linear 13–bit A/D and D/A, but will far exceed the required signal–to–distortion ratio at amplitudes greater than 40 dB below the peak amplitude. This excess performance is at the expense of data per sample. Methods of data reduction are implemented by compressing the 13–bit linear scheme to companded 8–bit schemes. There are two companding schemes used: Mu–255 Law specifically in North America, and A–Law specifically in Europe. These companding schemes are accepted world wide. These companding schemes follow a segmented or "piecewise–linear" curve formatted as sign bit, three chord bits, and four step bits. For a given chord, all sixteen of the steps have the same voltage weighting. As the voltage of the analog input increases, the four step bits increment and carry to the three chord bits which increment. When the chord bits increment, the step bits double their voltage weighting. This results in an effective resolution of six bits (sign + chord + four step bits) across a 42 dB dynamic range (seven chords above zero, by 6 dB per chord). Tables 3 and 4 show the linear quantization levels to PCM words for the two companding schemes.

In a sampling environment, Nyquist theory says that to properly sample a continuous signal, it must be sampled at a frequency higher than twice the signal's highest frequency component. Voice contains spectral energy above 3 kHz, but its absence is not detrimental to intelligibility. To reduce the digital data rate, which is proportional to the sampling rate, a sample rate of 8 kHz was adopted, consistent with a bandwidth of 3 kHz. This sampling requires a low–pass filter to limit the high frequency energy above 3 kHz from distorting the in–band signal. The telephone line is also subject to 50/60 Hz power line coupling, which must be attenuated from the signal by a high–pass filter before the A/D converter.

The D/A process reconstructs a staircase version of the desired in–band signal, which has spectral images of the in–band signal modulated about the sample frequency and its harmonics. These spectral images, called aliasing components, need to be attenuated to obtain the desired signal. The low–pass filter used to attenuate these aliasing components is typically called a reconstruction or smoothing filter.

The ML145554/57/64/67 PCM Codec–Filters have the codec, both presampling and reconstruction filters, and a precision voltage reference on–chip, and require no external components.

PIN DESCRIPTION

DIGITAL

FS$_R$
Receive Frame Sync

This is an 8 kHz enable that must be synchronous with BCLK$_R$. Following a rising FS$_R$ edge, a serial PCM word at D$_R$ is clocked by BCLK$_R$ into the receive data register. FSR also initiates a decode on the previous PCM word. In the absence of FS$_X$, the length of the FS$_R$ pulse is used to determine whether the I/O conforms to the Short Frame Sync or Long Frame Sync convention.

D$_R$
Receive Digital Data Input

BCLK$_R$/CLKSEL
Receive Data Clock and Master Clock Frequency Selector

If this input is a clock, it must be between 128 kHz and 4.096 MHz, and synchronous with FS$_R$. In synchronous applications this pin may be held at a constant level; then BCLK$_X$ is used as the data clock for both the transmit and receive sides, and this pin selects the assumed frequency of the master clock (see Table 1 in **Functional Description**).

MCLK$_R$/PDN
Receive Master Clock and Power–Down Control

Because of the shared DAC architecture used on these devices, only one master clock is needed. Whenever FS$_X$ is clocking, MCLK$_X$ is used to derive all internal clocks, and the MCLK$_R$/PDN pin merely serves as a power–down control. If MCLK$_R$/PDN pin is held low or is clocked (and at least one of the frame syncs is present), the part is powered up. If this pin is held high, the part is powered down. If FS$_X$ is absent but FSR is still clocking, the device goes into receive half–channel mode, and MCLK$_R$ (if clocking) generates the internal clocks.

MCLK$_X$
Transmit Master Clock

This clock is used to derive the internal sequencing clocks; it must be 1.536 MHz, 1.544 MHz, or 2.048 MHz.

BCLK$_X$
Transmit Data Clock

BCLK$_X$ may be any frequency between 128 kHz and 4.096 MHz, but it should be synchronous with MCLK$_X$.

D$_X$
Transmit Digital Data Output

This output is controlled by FS$_X$ and BCLK$_X$ to output the PCM data word; otherwise this pin is in a high–impedance state.

FS$_X$
Transmit Frame Sync

This is an 8 kHz enable that must be synchronous with BCLK$_X$. A rising FS$_X$ edge initiates the transmission of a serial PCM word, clocked by BCLK$_X$, out of D$_X$. If the FS$_X$ pulse is high for more than eight BCLK$_X$ periods, the D$_X$ and $\overline{\text{TS}}_X$ outputs will remain in a low–impedance state until FS$_X$ is brought low. The length of the FS$_X$ pulse is used to determine whether the transmit and receive digital I/O conforms to the Short Frame Sync or to the Long Frame Sync convention.

$\overline{\text{TSX}}$
Transmit Time Slot Indicator

This is an open–drain output that goes low whenever the D$_X$ output is in a low–impedance state (i.e., during the transmit time slot when the PCM word is being output) for enabling a PCM bus driver.

ANLB
Analog Loopback Control Input (ML145564/67 Only)

When held high, this pin causes the input of the transmit RC active filter to be disconnected from GS$_X$ and connected to VPO+ for analog loopback testing. This pin is held low in normal operation.

ANALOG

GS$_X$
Gain–Setting Transmit

This output of the transmit gain–adjust operational amplifier is internally connected to the encoder section of the device. It must be used in conjunction with VFXI– and VFXI+ to set the transmit gain for a maximum signal amplitude of 2.5 V peak. This output can drive a 600 Ω load to 2.5 V peak.

VF$_X$I–
Voice–Frequency Transmit Input (Inverting)

This is the inverting input of the transmit gain–adjust operational amplifier.

VF$_X$I+
Voice–Frequency Transmit Input (Non–Inverting)

This is the non–inverting input of the transmit gain–adjust operational amplifier.

VF$_R$O
Voice–Frequency Receive Output

This receive analog output is capable of driving a 600 Ω load to 2.5 V peak.

VPI
Voltage Power Input (ML145564/67 Only)

This is the inverting input to the first receive power amplifier. Both of the receive power amplifiers can be powered down by connecting this input to V$_{BB}$.

VPO–
Voltage Power Output (Inverted) (ML145564/67 Only)

This inverted output of the receive push–pull power amplifiers can drive 300 Ω to 3.3 V peak.

VPO+
Voltage Power Output (Non–Inverted) (ML145554/67 Only)

This non–inverted output of the receive push–pull power amplifier pair can drive 300 Ω to 3.3 V peak.

POWER SUPPLY

GNDA
Analog Ground

This terminal is the reference level for all signals, both analog and digital. It is 0 V.

V$_{CC}$
Positive Power Supply

V$_{CC}$ is typically 5 V.

V$_{BB}$
Negative Power Supply

V$_{BB}$ is typically – 5 V.

FUNCTIONAL DESCRIPTION

ANALOG INTERFACE AND SIGNAL PATH

The transmit portion of these codec–filters includes a low–noise gain setting amplifier capable of driving a 600 Ω load. Its output is fed to a three–pole anti–aliasing pre–filter. This pre–filter incorporates a two–pole Butterworth active low–pass filter, and a single passive pole. This pre–filter is followed by a single ended–to–differential converter that is clocked at 256 kHz. All subsequent analog processing utilizes fully differential circuitry. The next section is a fully–differential, five–pole switched capacitor low–pass filter with a 3.4 kHz passband. After this filter is a 3–pole switched–capacitor high–pass filter having a cutoff frequency of about 200 Hz. This high–pass stage has a transmission zero at DC that eliminates any DC coming from the analog input or from accumulated operational amplifier offsets in the preceding filter stages. The last stage of the high–pass filter is an autozeroed sample and hold amplifier.

One bandgap voltage reference generator and digital–to–analog converter (DAC) are shared by the transmit and receive sections. The autozeroed, switched–capacitor bandgap reference generates precise positive and negative reference voltages that are independent of temperature and power supply voltage. A binary–weighted capacitor array (CDAC) forms the chords of the companding structure, while a resistor string (RDAC) implements the linear steps within each chord. The encode process uses the DAC, the voltage reference, and a frame–by–frame autozeroed comparator to implement a successive–approximation conversion algorithm. All of the analog circuitry involved in the data conversion the voltage reference, RDAC, CDAC, and comparator are implemented with a differential architecture.

The receive section includes the DAC described above, asample and hold amplifier, a five–pole 3400 Hz switched-capacitor low–pass filter with sinX/X correction, and a two–pole active smoothing filter to reduce the spectral components of the switched capacitor filter. The output of the smoothing filter is a power amplifier that is capable of driving a 600 Ω load. The ML145564 and ML145567 add a pair of power amplifiers that are connected in a push–pull configuration; two external resistors set the gain of both of the complementary outputs. The output of the second amplifier may be internally connected to the input of the transmit anti–aliasing filter by bringing the ANLB pin high. The power amplifiers can drive unbalanced 300 Ω loads or a balanced 600 Ω load; they may be powered down independent of the rest of the chip by tying the VPI pin to V$_{BB}$.

MASTER CLOCKS

Since the codec–filter design has a single DAC architecture, only one master clock is used. In normal operation (both frame syncs clocking), the MCLK$_X$ is used as the master clock, regardless of whether the MCLK$_R$/PDN pin is clocking or low. The same is true if the part is in transmit half–channel mode (FS$_X$ clocking, FS$_R$ held low). But if the codec–filter is in the receive half–channel mode, with FS$_R$ clocking and FS$_X$ held low, MCLK$_R$ is used for the internal master clock if it is clocking; if MCLK$_R$ is low, then MCLK$_X$ is still used for the internal master clock. Since only one of the master clocks isused at any given time, they need not be synchronous.

The master clock frequency must be 1.536 MHz, 1.544 MHz, or 2.048 MHz. The frequency that the codec–filter expects depends upon whether the part is a Mu–Law or an A–Law part, and on the state of the BCLK$_R$/CLKSEL pin.The allowable options are shown In Table 1. When a level (rather than a clock) is provided for BCLK$_R$/CLKSEL, BCLK$_X$ is used as the bit clock for both transmit and receive.

Table 1. Master Clock Frequency Determination

BCLK$_R$/CLKSEL	Master Clock Frequency Expected	
	ML145554/64	ML145557/67
Clocked, 1, or Open	1.536 MHz 1.544 MHz	2.048 MHz
0	2.048 MHz	1.536 MHz 1.544 MHz

FRAME SYNCS AND DIGITAL I/O

These codec–filters can accommodate both of the industry standard timing formats. The Long Frame Sync mode isused by Lansdale's ML145500 family of codec–filters and the UDLT family of digital loop transceivers. The Short Frame Sync mode is compatible with the IDL (Interchip Digital Link) serial format used in Motorola and Lansdale's ISDN family and by other companies in their telecommunication devices. These codec–filters use the length of the transmit frame sync (FS$_X$) to determine the timing format for both transmit and receive unless the part is operating in the receive half–channel mode.

In the Long Frame Sync mode, the frame sync pulses must be at least three bit clock periods long. The D$_X$ and $\overline{TS}_X$ outputs are enabled by the logical ANDing of FS$_X$ and BCLK$_X$; when both are high, the sign bit appears at the D$_X$ output. The next seven rising edges of BCLK$_X$ clock out the remaining seven bits of the PCM word. The D$_X$ and $\overline{TS}_X$ outputs return to a high impedance state on the falling edge of the eighth bit clock or the falling edge of FS$_X$, whichever comes later. The receive PCM word is clocked into D$_R$ on the eight falling BCLK$_R$ edges following an FS$_R$ rising edge.

For Short Frame Sync operation, the frame sync pulses must be one bit clock period long. On the first BCLK$_X$ rising edge after the falling edge of BCLK$_X$ has latched FS$_X$ high, the D$_X$ and $\overline{TS}_X$ outputs are enabled and the sign bit is presented on D$_X$. The next seven rising edges of BCLK$_X$ clock out the remaining seven bits of the PCM word; on the eighth BCLK$_X$ falling edge, the D$_X$ and $\overline{TS}_X$ outputs return to a high impedance state. On the second falling BCLK$_R$ edge following an FS$_R$ rising edge, the receive sign bit is clocked into D$_R$. The next seven BCLK$_R$ falling edges clock in the remaining seven bits of the receive PCM word.

Table 2 shows the coding format of the transmit and receive PCM words.

HALF–CHANNEL MODES

In addition to the normal full–duplex operating mode, these codec–filters can operate in both transmit and receive half–channel modes. Transmit half–channel mode is entered by holding FS$_R$ low. The VF$_R$O output goes to analog ground but remains in a low impedance state (to facilitate a hybrid interface); PCM data at D$_R$ is ignored. Holding FS$_X$ low while clocking FSR puts these devices in the receive half–channel mode. In this state, the transmit input operational amplifier continues to operate, but the rest of the transmit circuitry is disabled; the D$_X$ and $\overline{TS}_X$ outputs remain in a high impedance state. MCLK$_R$ is used as the internal master clock if it is clocking. If MCLK$_R$ is not clocking, then MCLK$_X$ is used for the internal master clock, but in that case it should be synchronous with FS$_R$. If BCLK$_R$ is not clocking, BCLK$_X$ will be used for the receive data, just as in the full–channel operating mode. In receive half–channel mode only, the length ofthe FS$_R$ pulse is used to determine whether Short Frame Sync or Long Frame Sync timing is used at D$_R$.

POWER–DOWN

Holding both FS$_X$ and FS$_R$ low causes the part to go into the power–down state. Power–down occurs approximately 2 ms after the last frame sync pulse is received. An alternative way to put these devices in power–down is to hold the MCLK$_R$/PDN pin high. When the chip is powered down, the D$_X$, $\overline{TS}_X$, and GS$_X$ outputs are high impedance, the VF$_R$O, VPO–, and VPO+ operational amplifiers are biased with a trickle current so that their respective outputs remain stable at analog ground. To return the chip to the power–up state, MCLK$_R$/PDN must be low or clocking and at least one of the frame sync pulses must be present. The D$_X$ and $\overline{TS}_X$ outputs will remain in a high–impedance state until the second FS$_X$ pulse after power–up.

Table 2. PCM Data Format

Level	Mu–Law (ML145554/64)			A–Law (ML145557/67)		
	Sign Bit	Chord Bits	Step Bits	Sign Bit	Chord Bits	Step Bits
+ Full Scale	1	0 0 0	0 0 0 0	1	0 1 0	1 0 1 0
+ Zero	1	1 1 1	1 1 1 1	1	1 0 1	0 1 0 1
– Zero	0	1 1 1	1 1 1 1	0	1 0 1	0 1 0 1
– Full Scale	0	0 0 0	0 0 0 0	0	0 1 0	1 0 1 0

MAXIMUM RATINGS (Voltage Referenced to GNDA)

Rating	Symbol	Value	Unit
DC Supply Voltage V_{CC} to V_{BB} V_{CC} to GNDA V_{BB} to GNDA		– 0.5 to + 13 – 0.3 to + 7.0 – 7.0 to + 0.3	V
Voltage on Any Analog Input or Output Pin		V_{BB} – 0.3 to V_{CC} + 0.3	V
Voltage on Any Digital Input or Output Pin		GNDA – 0.3 to V_{CC} + 0.3	V
Operating Temperature Range	T_A	– 40 to + 85	°C
Storage Temperature Range	T_{stg}	– 85 to + 150	°C

This device contains circuitry to protect against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., V_{BB}, GNDA, or V_{CC}).

POWER SUPPLY (T_A = – 40 to + 85°C)

Characteristic		Min	Typ	Max	Unit
DC Supply Voltage	V_{CC}	4.75	5.0	5.25	V
	V_{BB}	– 4.75	– 5.0	– 5.25	
Active Power Dissipation (No Load)	ML145554/57	—	40	60	mW
	ML145564/67	—	45	70	
	ML145564/67, VPI = V_{BB}	—	40	60	
Power–Down Dissipation (No Load)	ML145554/57	—	1.0	3.0	mW
	ML145564/67	—	2.0	5.0	
	ML145564/67, VPI = V_{BB}	—	1.0	3.0	

DIGITAL LEVELS (V_{CC} = 5 V ± 5%, V_{BB} = – 5 V ± 5%, GNDA = 0 V, T_A = – 40 to + 85°C)

Characteristic		Symbol	Min	Max	Unit
Input Low Voltage		V_{IL}	—	0.6	V
Input High Voltage		V_{IH}	2.2	—	V
Output Low Voltage	D_X or TS_X, I_{OL} = 3.2 mA	V_{OL}	—	0.4	V
Output High Voltage	D_X, I_{OH} = – 3.2 mA	V_{OH}	2.4	—	V
	I_{OH} = – 1.6 mA		V_{CC} – 0.5	—	
Input Low Current	GNDA ≤ V_{in} ≤ V_{CC}	I_{IL}	– 10	+ 10	µA
Input High Current	GNDA ≤ V_{in} ≤ V_{CC}	I_{IH}	– 10	+ 10	µA
Output Current in High Impedance State	GNDA ≤ D_X ≤ V_{CC}	I_{OZ}	– 10	+ 10	µA

ANALOG ELECTRICAL CHARACTERISTICS

(V_{CC} = + 5 V ± 5%, V_{BB} = – 5 V ± 5%, VF_XI – Connected to GS_X, T_A = – 40 to + 85°C)

Characteristic		Min	Typ	Max	Unit
Input Current (– 2.5 ≤ V_{in} ≤ + 2.5 V)	VF_XI +, VF_XI –	—	± 0.05	± 0.2	µA
AC Input Impedance to GNDA (1 kHz)	VF_XI +, VF_XI –	10	20	—	MΩ
Input Capacitance	VF_XI +, VF_XI –	—	—	10	pF
Input Offset Voltage of GS_X Op Amp	VF_XI +, VF_XI –	—	—	± 25	mV
Input Common Mode Voltage Range	VF_XI +, VF_XI –	– 2.5	—	2.5	V
Input Common Mode Rejection Ratio	VF_XI +, VF_XI –	—	65	—	dB
Unity Gain Bandwidth of GS_X Op Amp (R_{load} ≥ 10 kΩ)		—	1000	—	kHz
DC Open Loop Gain of GS_X Op Amp (R_{load} ≥ 10 kΩ)		75	—	—	dB
Equivalent Input Noise (C–Message) Between VF_XI+ and VF_XI– at GS_X		—	–20	—	dBrnC0
Output Load Capacitance for GS_X Op Amp		0	—	100	pF
Output Voltage Range for GS_X	R_{load} = 10 kΩ to GNDA	– 3.5	—	+ 3.5	V
	R_{load} = 600 Ω to GNDA	– 2.8	—	+ 2.8	
Output Current (– 2.8 V ≤ V_{out} ≤ + 2.8 V)	GS_X, VF_RO	± 5.0	—	—	mA
Output Impedance VF_RO (0 to 3.4 kHz)		—	1	—	Ω
Output Load Capacitance for VF_RO		0	—	500	pF
VF_RO Output DC Offset Voltage Referenced to GNDA		—	—	± 100	mV
Transmit Power Supply Rejection	Positive, 0 to 100 kHz, C–Message	45	—	—	dBC
	Negative, 0 to 100 kHz, C–Message	45	—	—	
Receive Power Supply Rejection	Positive, 0 to 100 kHz, C–Message	50	—	—	dBC
	Positive, 4 kHz to 25 kHz	50	—	—	dB
	Positive, 25 kHz to 50 kHz	43	—	—	dB
	Negative, 0 to 100 kHz, C–Message	50	—	—	dBC
	Negative, 4 kHz to 25 kHz	45	—	—	dB
	Negative, 25 kHz to 50 kHz	38	—	—	dB

ML145564/67 Power Drivers

Characteristic		Min	Typ	Max	Unit
Input Current (– 1 V ≤ VPI ≤ + 1 V)	VPI	—	±0.05	±0.5	µA
Input Resistance (– 1 V ≤ VPI ≤ + 1 V)	VPI	5	10	—	MΩ
Input Offset Voltage (VPI Connected to VPO–)	VPI	—	—	±50	mV
Output Resistance, Inverted Unity Gain	VPO+ or VPO–	—	1	—	Ω
Unity Gain Bandwidth, Open Loop	VPO–	—	400	—	kHz
Load Capacitance (∞ Ω ≥ R_{load} ≥ 300 Ω)	VPO+ or VPO– to GNDA	0	—	1000	pF
Gain from VPO– to VPO+ (R_{load} = 300 Ω, VPO+ to GNDA Level at VPO– = 1.77 Vrms, +3 dBm0)		—	–1	—	V/V
Maximum 0 dBm0 Level for Better than ± 0.1 dB Linearity Over the Range – 10 dBm0 to + 3 dBm0 (For R_{load} between VPO+ and VPO–)	R_{load} = 600 Ω	3.3	—	—	Vrms
	R_{load} = 1200 Ω	3.5	—	—	
	R_{load} = 10 kΩ	4.0	—	—	
Power Supply Rejection of V_{CC} or V_{BB} (VPO– Connected to VPI) VPO + or VPO – to GNDA	0 to 4 kHz	55	—	—	dB
	4 to 50 kHz	35	—	—	
Differential Power Supply Rejection of V_{CC} or V_{BB} (VPO– Connected to VPI)	VPO+ to VPO–, 0 to 50 kHz	50	—	—	dB

ANALOG TRANSMISSION PERFORMANCE

(V_{CC} = + 5 V ± 5%, V_{BB} = – 5 V ± 5%, GNDA = 0 V, 0 dBm0 = 1.2276 Vrms = + 4 dBm @ 600 Ω, FS_X = FS_R = 8 kHz, $BCLK_X$ = $MCLK_X$ = 2.048 MHz Synchronous Operation, VF_XI – Connected to GS_X, T_A = – 40 to + 85°C Unless Otherwise Noted)

Characteristic	End–to–End		A/D		D/A		Unit
	Min	Max	Min	Max	Min	Max	
Absolute Gain (0 dBm0 @ 1.02 kHz, T_A = 25°C, V_{CC} = 5 V, V_{BB} = – 5 V)	—	—	–0.25	– 0.25	– 0.25	+ 0.25	dB
Absolute Gain Variation with Temperature 0 to 70°C	—	—	—	± 0.03	—	± 0.03	dB
– 40 to + 85°C	—	—	—	± 0.06	—	± 0.06	
Absolute Gain Variation with Power Supply (V_{CC} = 5 V, ± 5%, V_{BB} = – 5 V, ± 5%)	—	—	—	± 0.02	—	± 0.02	dB
Gain vs Level Tone (Relative to – 10 dBm0, 1.02 kHz) + 3 to – 40 dBm0	– 0.4	+ 0.4	– 0.2	+ 0.2	– 0.2	+ 0.2	dB
– 40 to – 50 dBm0	– 0.8	+ 0.8	– 0.4	+ 0.4	– 0.4	+ 0.4	
– 50 to – 55 dBm0	– 1.6	+ 1.6	– 0.8	+ 0.8	– 0.8	+ 0.8	
Gain vs Level Pseudo Noise CCITT G.712 – 10 to – 40 dBm0	—	—	– 0.25	+ 0.25	– 0.25	+ 0.25	dB
(ML145557/67 A–Law Relative to – 10 dBm0) – 40 to – 50 dBm0	—	—	– 0.30	+ 0.30	– 0.30	+ 0.30	
– 50 to – 55 dBm0	—	—	– 0.45	+ 0.45	– 0.45	+ 0.45	
Total Distortion, 1.02 kHz Tone (C–Message) + 3 dBm0	33	—	33	—	33	—	dBC
0 to – 30 dBm0	35	—	36	—	36	—	
– 40 dBm0	29	—	30	—	30	—	
– 45 dBm0	24	—	25	—	25	—	
– 55 dBm0	15	—	15	—	15	—	
Total Distortion With Pseudo Noise CCITT G.714 – 3 dBm0	27.5	—	28	—	28.5	—	dB
(ML145557/67 A–Law) – 6 to – 27 dBm0	35	—	35.5	—	36	—	
– 34 dBm0	33.1	—	33.5	—	34.2	—	
– 40 dBm0	28.2	—	28.5	—	30	—	
– 55 dBm0	13.2	—	13.5	—	15	—	
Idle Channel Noise (For End–End and A/D, Note 1)							
(ML145554/64 Mu–Law, C–Message Weighted)	—	15	—	15	—	7	dBrnC0
(ML145557/67 A–Law, Psophometric Weighted)	—	–70	—	– 70	—	– 83	dBm0p
Frequency Response (Relative to 1.02 kHz @ 0 dBm0) 15 Hz	—	– 40	—	– 40	– 0.15	0	dB
50 Hz	—	– 30	—	– 30	– 0.15	0	
60 Hz	—	– 26	—	– 26	– 0.15	0	
200 Hz	—	—	– 1.0	– 0.4	– 0.15	0	
300 to 3000 Hz	– 0.3	0.3	– 0.15	+ 0.15	– 0.15	+ 0.15	
3300 Hz	– 0.70	+ 0.3	– 0.35	+ 0.15	– 0.35	+ 0.15	
3400 Hz	– 1.6	0	– 0.8	0	– 0.8	0	
4000 Hz	—	– 28	—	– 14	—	– 14	
4600 Hz	—	– 60	—	– 32	—	– 30	
In–Band Spurious 300 to 3000 Hz (1.02 kHz @ 0 dBm0, Transmit and Receive)	—	–48	—	– 48	—	– 48	dBm0
Out–of–Band Spurious at VF_RO (300 – 3400 Hz @ 0 dBm0 In)							dB
4600 to 7600 Hz	—	– 30	—	—	—	– 30	
7600 to 8400 Hz	—	– 40	—	—	—	– 40	
8400 to 100,000 Hz	—	– 30	—	—	—	– 30	
Idle Channel Noise Selective (8 kHz, Input = GNDA, 30 Hz Bandwidth)	—	–70	—	—	—	– 70	dBm0
Absolute Delay (1600 Hz)	—	—	—	315	—	215	µs
Group Delay Referenced to 1600 Hz 500 to 600 Hz	—	—	—	220	– 40	—	µs
600 to 800 Hz	—	—	—	145	– 40	—	
800 to 1000 Hz	—	—	—	75	– 40	—	
1000 to 1600 Hz	—	—	—	40	– 30	—	
1600 to 2600 Hz	—	—	—	75	—	90	
2600 to 2800 Hz	—	—	—	105	—	125	
2800 to 3000 Hz	—	—	—	155	—	175	
Crosstalk of 1020 Hz @ 0 dBm0 from A/D or D/A (Note 2)	—	—	—	– 75	—	– 75	dB
Intermodulation Distortion of Two Frequencies of Amplitudes – 4 to – 21 dBm0 from the Range 300 to 3400 Hz	—	– 41	—	– 41	—	– 41	dB

NOTES:

1. Extrapolated from a 1020 Hz @ – 50 dBm0 distortion measurement to correct for encoder enhancement.
2. Selectively measured while the A/D is stimulated with 2667 Hz @ – 50 dBm0.

DIGITAL SWITCHING CHARACTERISTICS

(V_{CC} = 5 V ± 5%, V_{BB} = – 5 V ± 5%, GNDA = 0 V, All Signals Referenced to GNDA; T_A = – 40 to + 85°C, C_{load} = 150 pF Unless Otherwise Noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Master Clock Frequency $MCLK_X$ or $MCLK_R$	f_M	— — —	1.536 1.544 2.048	— — —	MHz
Minimum Pulse Width High or Low $MCLK_X$ or $MCLK_R$	$t_{w(M)}$	100	—	—	ns
Minimum Pulse Width High or Low $BCLK_X$ or $BCLK_R$	$t_{w(B)}$	50	—	—	ns
Minimum Pulse WIdth Low FS_X or FS_R	$t_{w(FL)}$	50	—	—	ns
Rise Time for all Digital Signals	t_r	—	—	50	ns
Fall Time for all Digital Signals	t_f	—	—	50	ns
Bit Clock Data Rate $BCLK_X$ or $BCLK_R$	f_B	128	—	4096	kHz
Setup Time from $BCLK_X$ Low to $MCLK_R$ High	$t_{su(BRM)}$	50	—	—	ns
Setup Time from $MCLK_X$ High to $BCLK_X$ Low	$t_{su(MFB)}$	20	—	—	ns
Hold Time from $BCLK_X$ ($BCLK_R$) Low to FS_X (FS_R) High	$t_{h(BF)}$	20	—	—	ns
Setup Time for FS_X (FS_R) High to $BCLK_X$ ($BCLK_R$) Low for Long Frame	$t_{su(FB)}$	80	—	—	ns
Delay Time from $BCLK_X$ High to D_X Data Valid	$t_{d(BD)}$	20	60	140	ns
Delay Time from $BCLK_X$ High to $\overline{TS}_X$ Low	$t_{d(BTS)}$	20	50	140	ns
Delay Time from the 8th $BCLK_X$ Low of FS_X Low to D_X Output Disabled	$t_{d(ZC)}$	50	70	140	ns
Delay Time to Valid Data from FS_X or $BCLK_X$, Whichever is Later	$t_{d(ZF)}$	20	60	140	ns
Setup Time from D_R Valid to $BCLK_X$ Low	$t_{su(DB)}$	0	—	—	ns
Hold Time from $BCLK_R$ Low to D_R Invalid	$t_{h(BD)}$	50	—	—	ns
Setup Time from FS_X (FS_R) High to $BCLK_X$ ($BCLK_R$) Low in Short Frame	$t_{su(F)}$	50	—	—	ns
Hold Time from $BCLK_X$ ($BCLK_R$) Low to FS_X (FS_R) Low in Short Frame	$t_{h(F)}$	50	—	—	ns
Hold Time from 2nd Period of $BCLK_X$ ($BCLK_R$) Low to FS_X (FS_R) Low in Long Frame	$t_{h(BFI)}$	50	—	—	ns

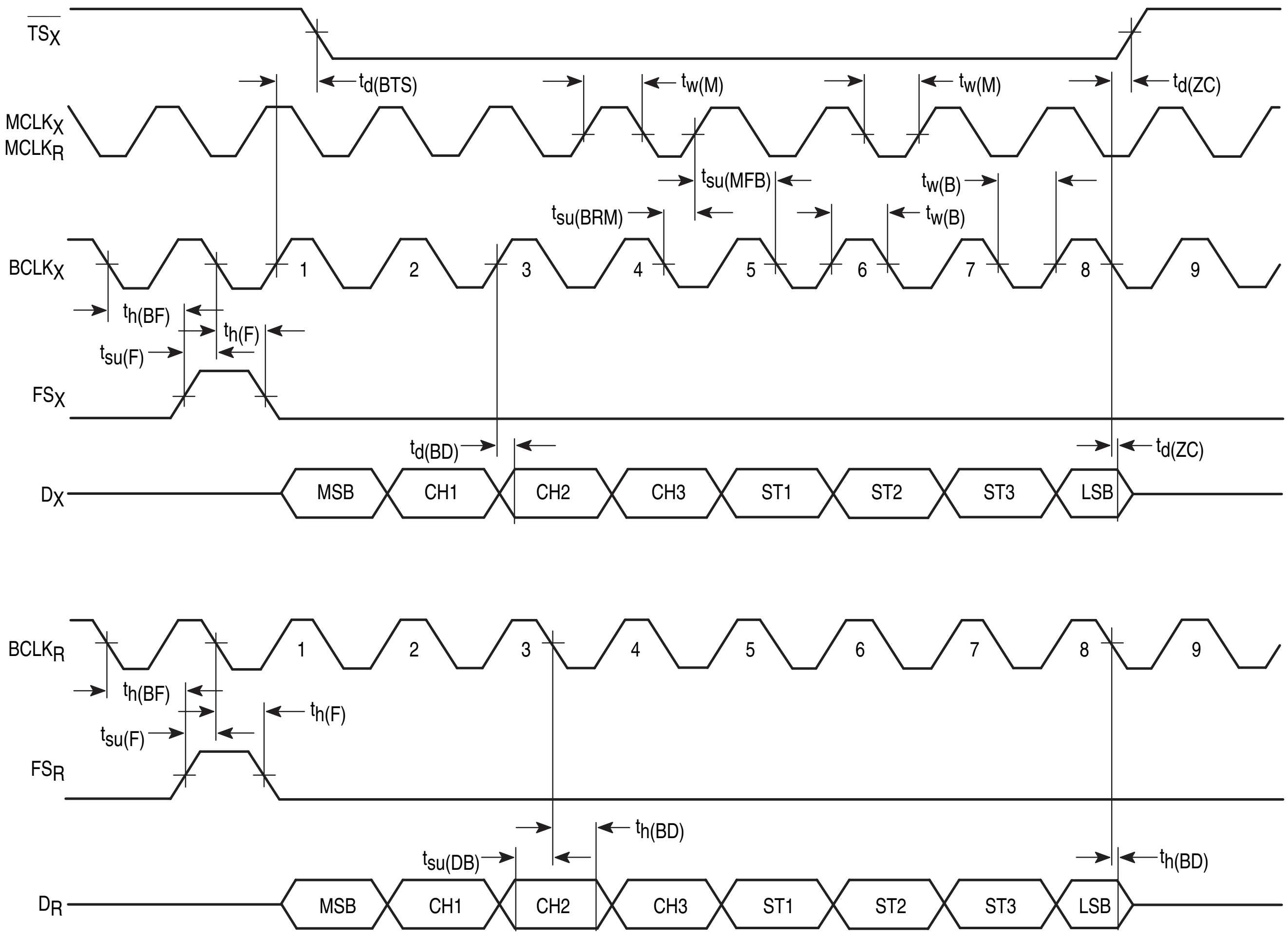


Figure 1. Short Frame Sync Timing

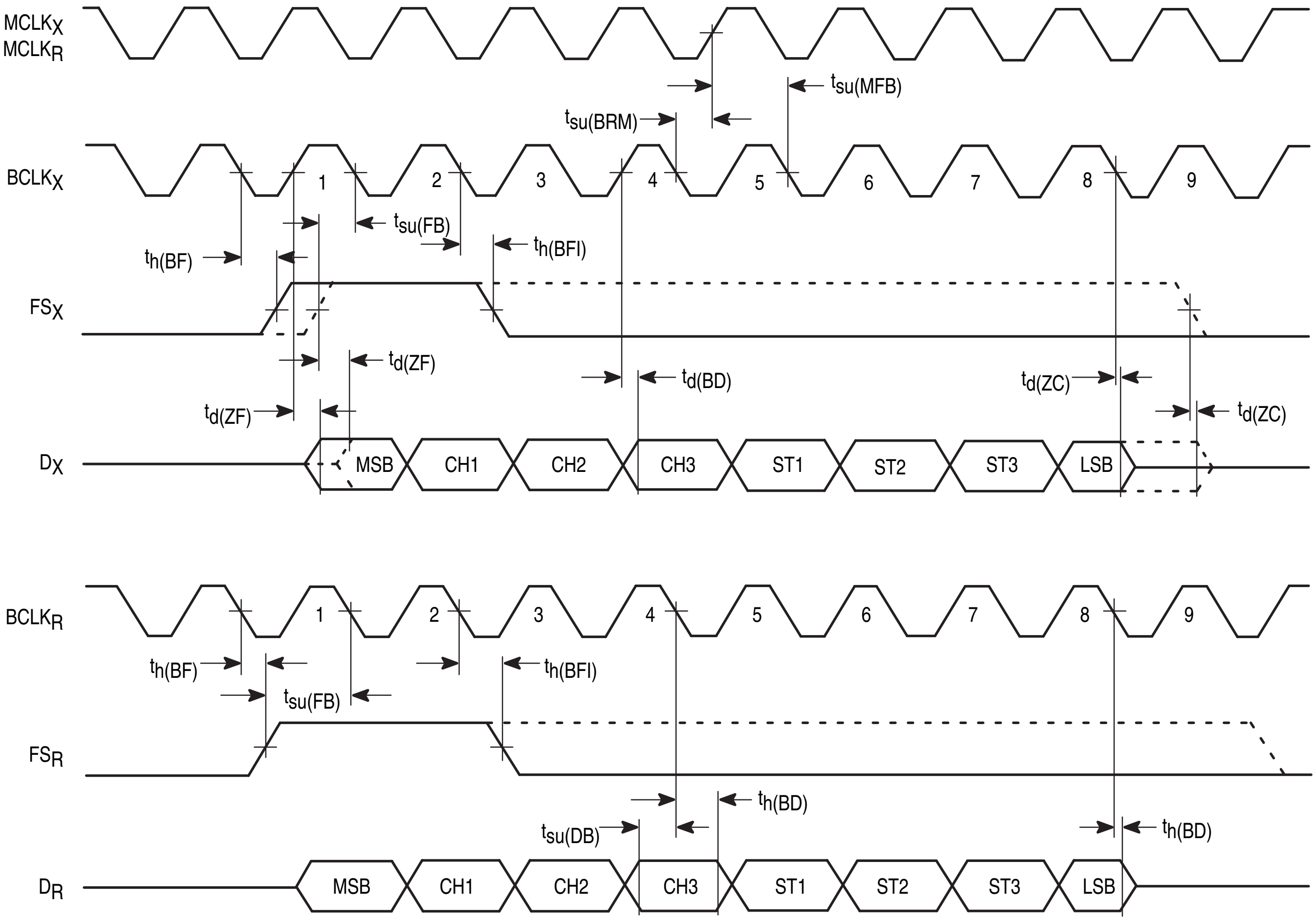


Figure 2. Long Frame Sync Timing

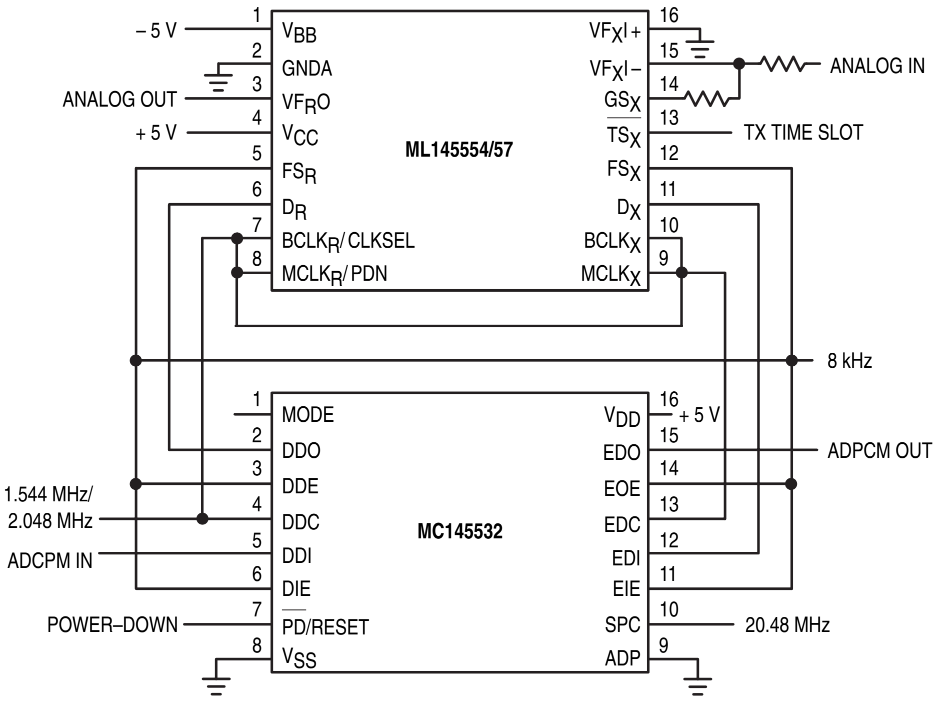
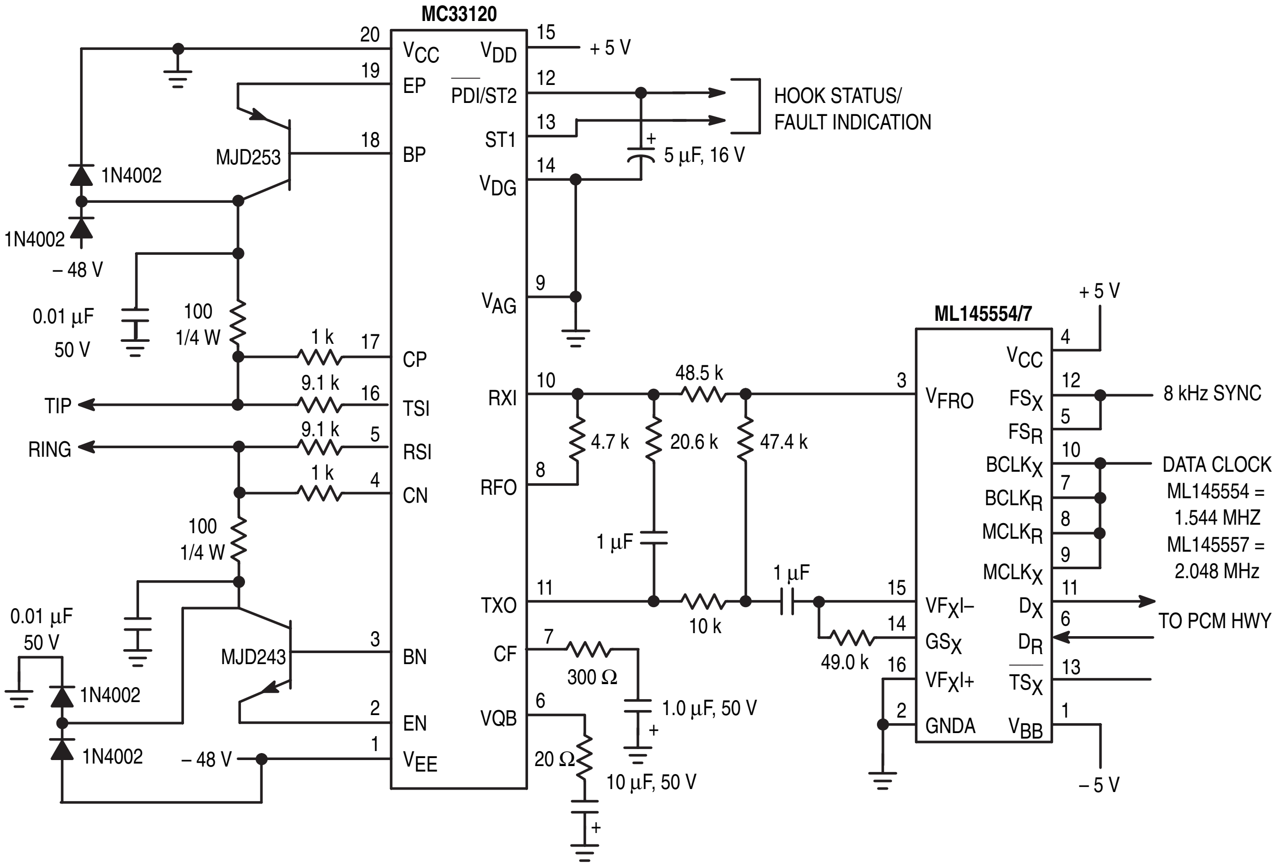


Figure 3. ADPCM Transcoder Application



NOTE: Six resistors and two capacitors on the two–wire side can be 5% tolerance.

Figure 4. A Complete Single Party Channel Unit Using ML145554/57 PCM Codec–Filter and MC33120 SLIC

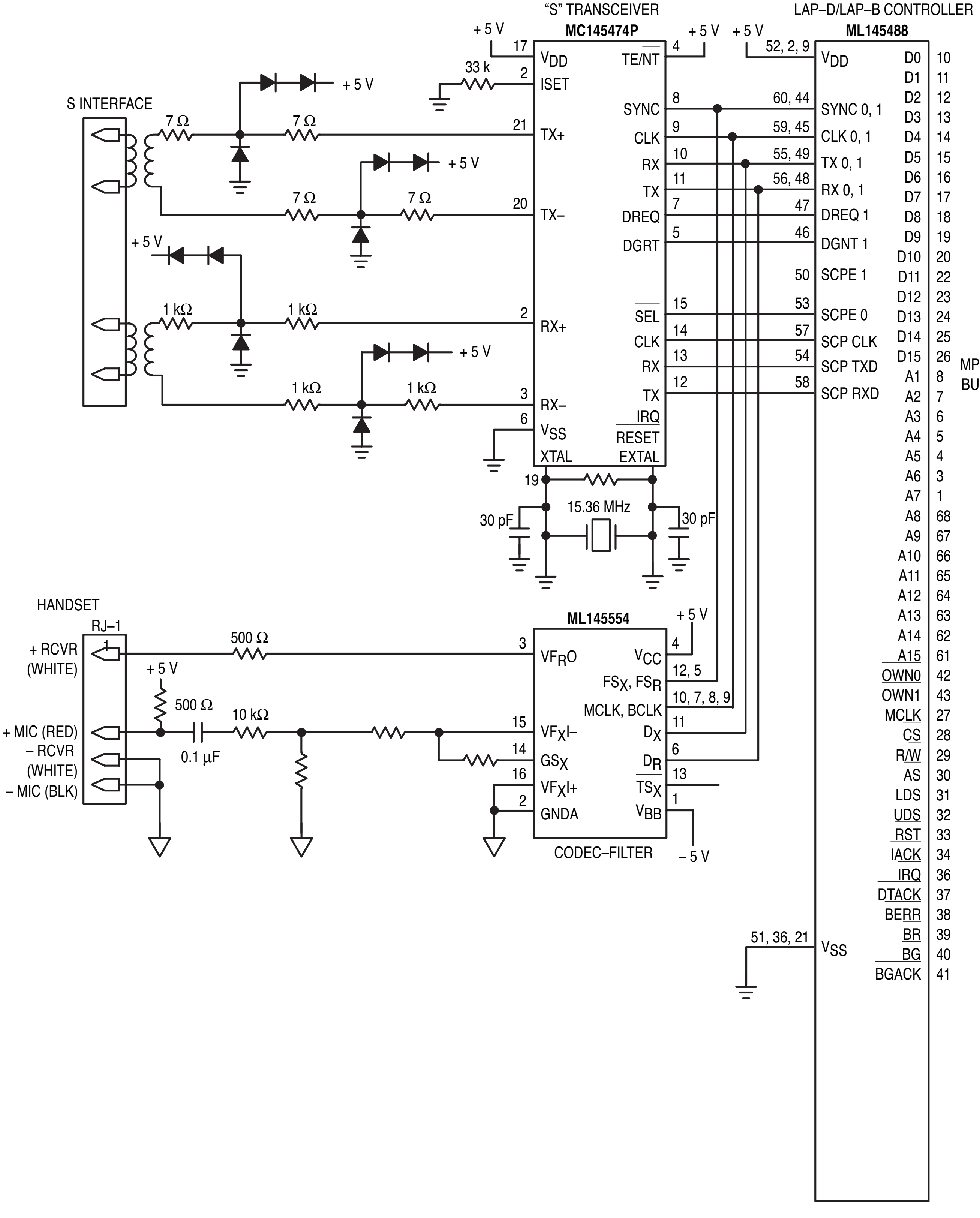


Figure 5. ISDN Voice/Data Terminal

Table 3. Mu–Law Encode–Decode Characteristics

Chord Number	Number of Steps	Step Size	Normalized Encode Decision Levels	Digital Code								Normalized Decode Levels
				1	2	3	4	5	6	7	8	
				Sign	Chord	Chord	Chord	Step	Step	Step	Step	
8	16	256	8159									
				1	0	0	0	0	0	0	0	8031
			7903 ⋮ 4319					⋮				⋮
				1	0	0	0	1	1	1	1	4191
7	16	128	4063 ⋮ 2143					⋮				⋮
				1	0	0	1	1	1	1	1	2079
6	16	64	2015 ⋮ 1055					⋮				⋮
				1	0	1	0	1	1	1	1	1023
5	16	32	991 ⋮ 511					⋮				⋮
				1	0	1	1	1	1	1	1	495
4	16	16	479 ⋮ 239					⋮				⋮
				1	1	0	0	1	1	1	1	231
3	16	8	223 ⋮ 103					⋮				⋮
				1	1	0	1	1	1	1	1	99
2	16	4	95 ⋮ 35					⋮				⋮
				1	1	1	0	1	1	1	1	33
1	15	2	31 ⋮ 3					⋮				⋮
				1	1	1	1	1	1	1	0	2
			1									
	1	1		1	1	1	1	1	1	1	1	0
			0									

NOTES:

1. Characteristics are symmetrical about analog zero with sign bit = 0 for negative analog values.
2. Digital code includes inversion of all magnitude bits.

Table 4. A–Law Encode–Decode Characteristics

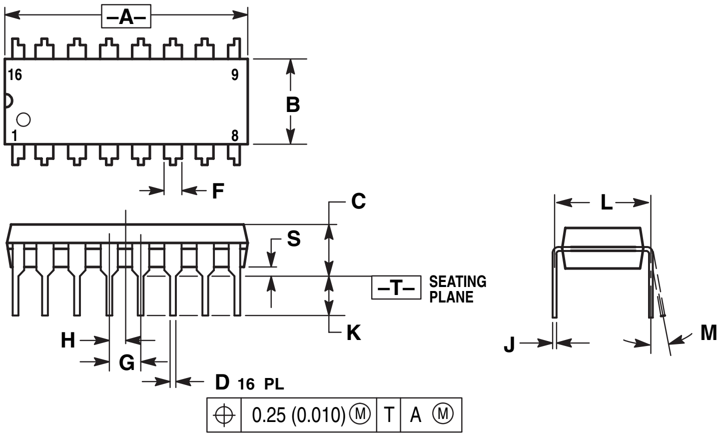
Chord Number	Number of Steps	Step Size	Normalized Encode Decision Levels	Digital Code								Normalized Decode Levels
				1	2	3	4	5	6	7	8	
				Sign	Chord	Chord	Chord	Step	Step	Step	Step	
			4096									
7	16	128		1	0	1	0	1	0	1	0	4032
			3968 ⋮ 2176				⋮					⋮
				1	0	1	0	0	1	0	1	2112
			2048									
6	16	64	⋮ 1088				⋮					⋮
				1	0	1	1	0	1	0	1	1056
			1024									
5	16	32	⋮ 544				⋮					⋮
				1	0	0	0	0	1	0	1	528
			512									
4	16	16	⋮ 272				⋮					⋮
				1	0	0	1	0	1	0	1	264
			256									
3	16	8	⋮ 136				⋮					⋮
				1	1	1	0	0	1	0	1	132
			128									
2	16	4	⋮ 68				⋮					⋮
				1	1	1	1	0	1	0	1	66
			64									
1	32	2	⋮ 2				⋮					⋮
				1	1	0	1	0	1	0	1	1
			0									

NOTES:

1. Characteristics are symmetrical about analog zero with sign bit = 0 for negative analog values.
2. Digital code includes alternate bit inversion, as specified by CCITT.

OUTLINE DIMENSIONS

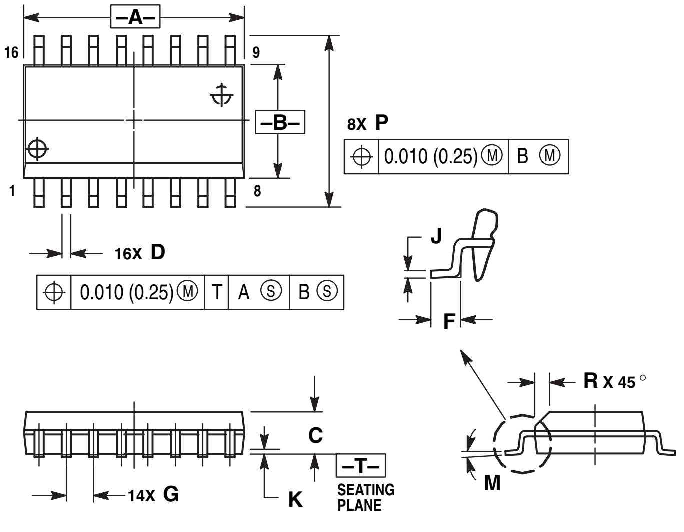
P DIP 16 = EP
(ML145554EP, ML145557EP)
PLASTIC DIP
CASE 648–08



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

SOG 16 = -5P
(ML145554-5P, ML145557-5P)
SOG PACKAGE
CASE 751G–02

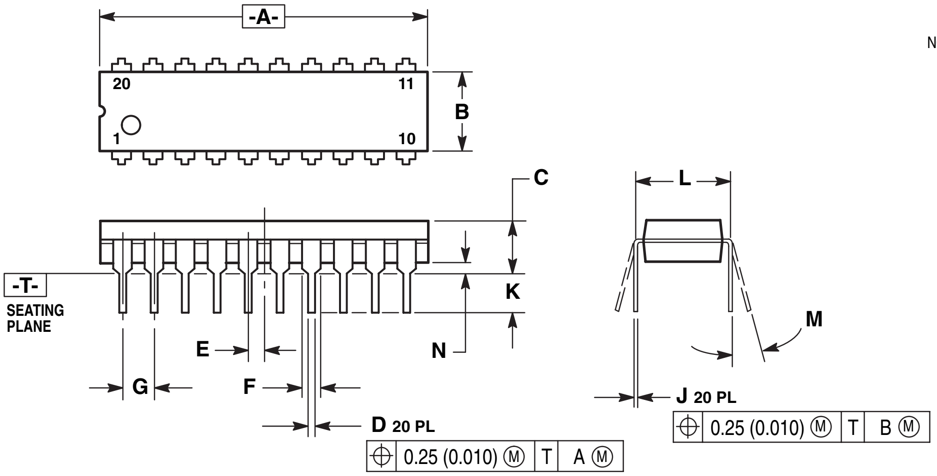


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

OUTLINE DIMENSIONS

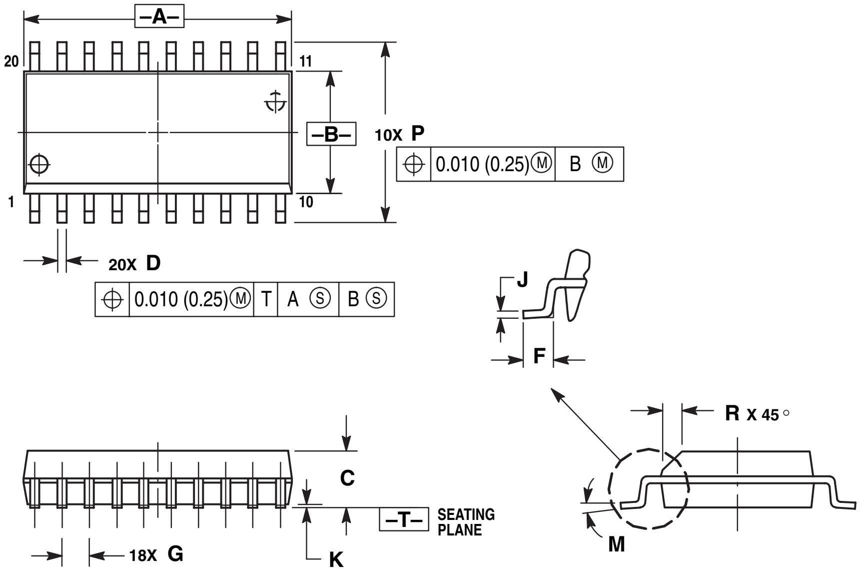
P DIP 20 = RP
(ML145564RP, ML145567RP)
PLASTIC DIP
CASE 738–03



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

SOG 20 = -6P
(ML145564-6P, ML145567-6P)
SOG PACKAGE
CASE 751D–04



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029