

ADC0831A, ADC0832A, ADC0831B, ADC0832B A/D PERIPHERALS WITH SERIAL CONTROL

SLAS006 – AUGUST 1985 – REVISED JUNE 1986

- **8-Bit Resolution**
- **Easy Microprocessor interface or Stand-Alone Operation**
- **Operates Ratiometrically or With 5-V Reference**
- **Single Channel or Multiplexed Twin Channels With Single-Ended or Differential Input Options**
- **Input Range 0 to 5 V With Single 5-V Supply**
- **Inputs and Outputs Are Compatible With TTL and MOS**
- **Conversion Time of 32 μ s at CLK = 250 kHz**
- **Designed to Be interchangeable With National Semiconductor ADC0831 and ADC0832**

DEVICE	TOTAL UNADJUSTED ERROR	
	A-SUFFIX	B-SUFFIX
ADC0831	± 1 LSB	$\pm 1/2$ LSB
ADC0832	± 1 LSB	$\pm 1/2$ LSB

description

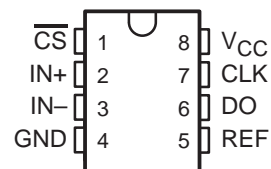
These devices are 8-bit successive-approximation analog-to-digital converters. The ADC0831A and ADC0831B have single input channels; the ADC0832A and ADC0832B have multiplexed twin input channels. The serial output is configured to interface with standard shift registers or microprocessors. Detailed information on interfacing to most popular microprocessors is readily available from the factory.

The ADC0832 multiplexer is software configured for single-ended or differential inputs. The differential analog voltage input allows for common-mode rejection or offset of the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

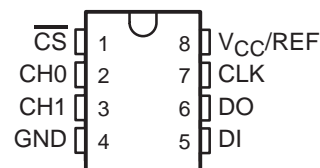
The operation of the ADC0831 and ADC0832 devices is very similar to the more complex ADC0834 and ADC0838 devices. Ratiometric conversion can be attained by setting the REF input equal to the maximum analog input signal value, which gives the highest possible conversion resolution. Typically, REF is set equal to V_{CC} (done internally on the ADC0832). For more detail on the operation of the ADC0831 and ADC0832 devices, refer to the ADC0834/A DC0838 data sheet.

The ADC0831AC, ADC0831BC, ADC0832AC, and ADC0832BC are characterized for operation from 0°C to 70°C. The ADC0831AI, ADC0831BI, ADC0832AI, and ADC0832BI are characterized for operation from -40°C to 85°C.

ADC0831 . . . P PACKAGE
(TOP VIEW)



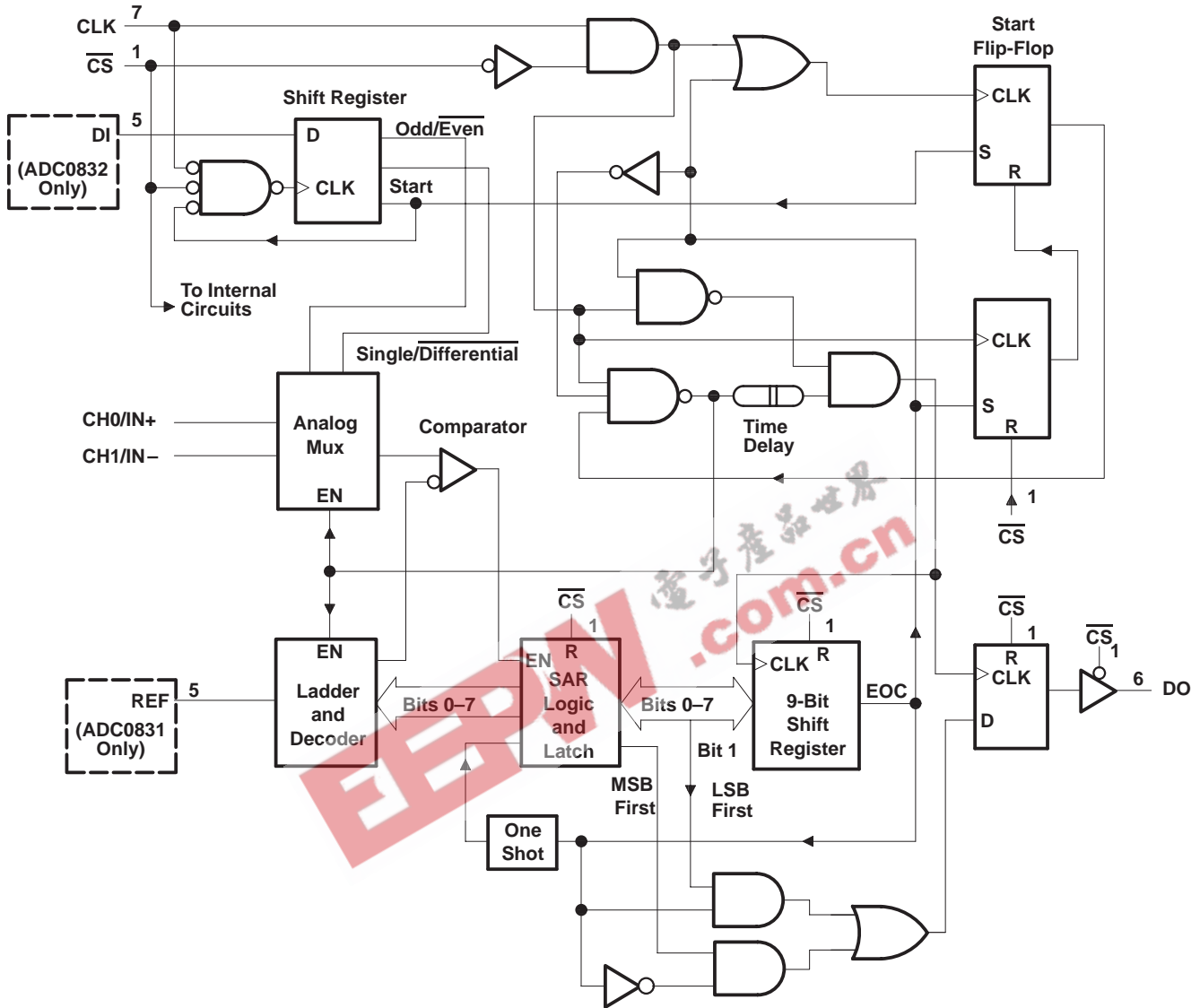
ADC0832 . . . P PACKAGE
(TOP VIEW)



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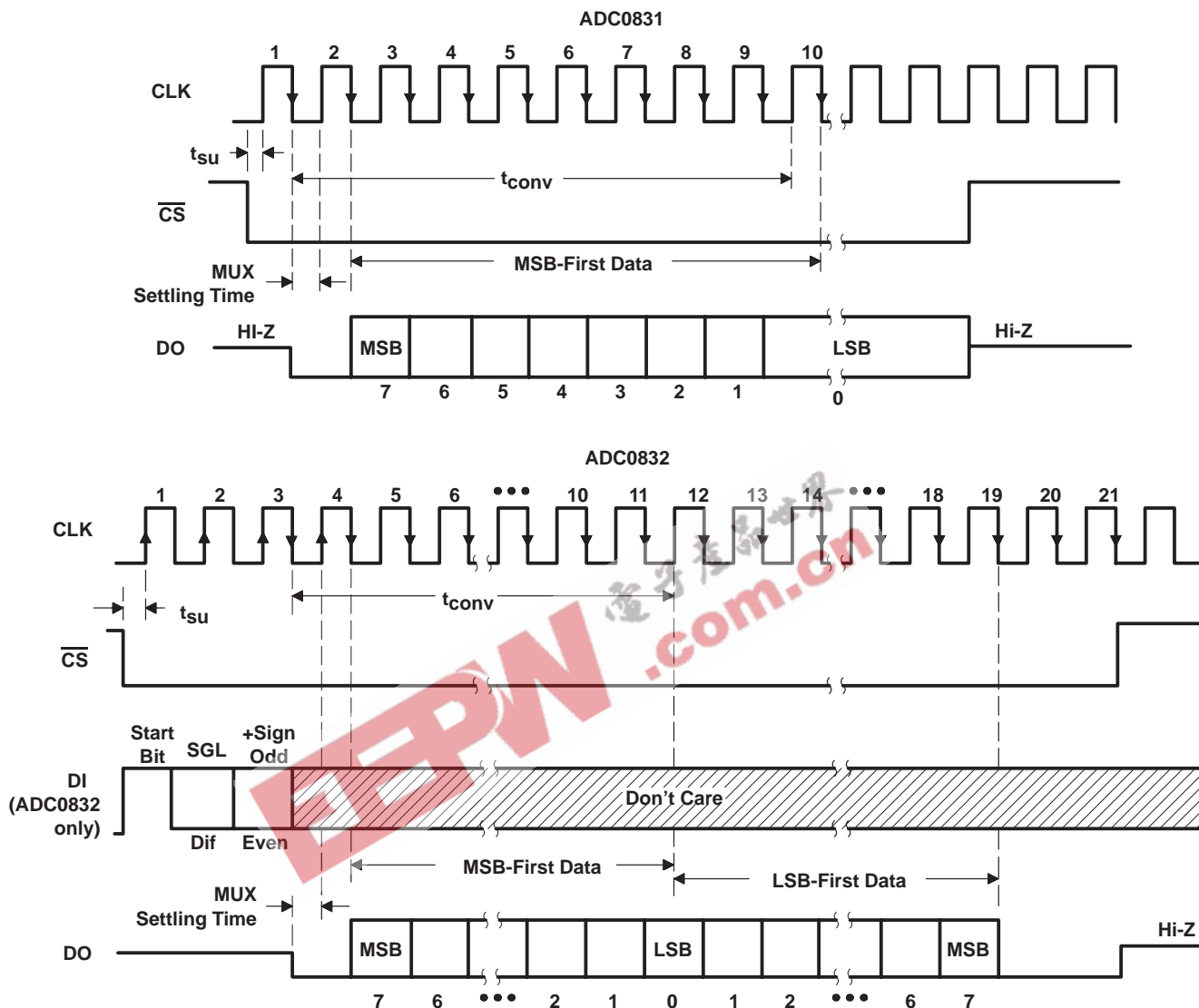
functional block diagram



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sequence of operation



ADC0832 MUX ADDRESS CONTROL LOGIC TABLE

MUX ADDRESS		CHANNEL NUMBER	
SGL/ \overline{DIF}	ODD/ \overline{EVEN}	0	1
L	L	+	-
L	H	-	+
H	L	+	-
H	H	-	+

H = high level, L = low level,
- or + = polarity of selected input pin

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electrical characteristics over recommended range of operating free-air temperature, $V_{CC} = 5\text{ V}$, $f_{clock} = 250\text{ kHz}$ (unless otherwise noted)

analog and converter section

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{ICR}	Common-mode input voltage range	See Note 3	-0.05 to $V_{CC}+0.05$			V
$I_{I(stdb)}$	Standby input current (see Note 4)	On-channel	$V_I = 5\text{ V}$		1	μA
		Off-channel	$V_I = 0$		-1	
		On-channel	$V_I = 0$		-1	
		Off-channel	$V_I = 5\text{ V}$		1	
$r_{i(REF)}$	Input resistance to reference ladder		1.3	2.4	5.9	$\text{k}\Omega$

total device

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
I_{CC}	Supply current	ADC0831		1	2.5	mA
		ADC0832		3	5.2	

† All parameters are measured under open-loop conditions with zero common-mode input voltage.

‡ All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

NOTES: 3. If channel $IN-$ is more positive than channel $IN+$, the digital output code will be 0000 0000. Connected to each analog input are two on-chip diodes that conduct forward current for analog input voltages one diode drop above V_{CC} . Care must be taken during testing at low V_{CC} levels (4.5 V) because high-level analog input voltage (5 V) can, especially at high temperatures, cause this input diode to conduct and cause errors for analog inputs that are near full-scale. As long as the analog voltage does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V to 5 V input voltage range requires a minimum V_{CC} of 4.95 V for all variations of temperature and load.

4. Standby input currents are currents going into or out of the on or off channels when the A/D converter is not performing conversion and the clock is in a high or low steady-state condition.

operating characteristics $V_{CC} = REF = 5\text{ V}$, $f_{clock} = 250\text{ kHz}$, $t_r = t_f = 20\text{ ns}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS§	AI, AC SUFFIX			BI, BC SUFFIX			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Supply-voltage variation error		$V_{CC} = 4.75\text{ V to } 5.25\text{ V}$	$\pm 1/16$	$\pm 1/4$		$\pm 1/16$	$\pm 1/4$	LSB	
Total unadjusted error (see Note 5)		$V_{ref} = 5\text{ V}$, $T_A = \text{MIN to MAX}$			± 1		$\pm 1/2$	LSB	
Common-mode error		Differential mode	$\pm 1/16$	$\pm 1/4$		$\pm 1/16$	$\pm 1/4$	LSB	
t_{pd}	Propagation delay time, output data after $CLK\uparrow$ (see Note 6)	MSB-first data		650	1500		650	1500	ns
		LSB-first data	$C_L = 100\text{ pF}$	250	600		250	600	
t_{dis}	Output disable time, DO after $CS\uparrow$	$C_L = 10\text{ pF}$, $R_L = 10\text{ k}\Omega$		125	250		125	250	ns
		$C_L = 100\text{ pF}$, $R_L = 2\text{ k}\Omega$			500			500	
t_{conv}	Conversion time (multiplexer addressing time not included)			8			8	clock periods	

§ All parameters are measured under open-loop conditions with zero common-mode input voltage. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTES: 5. Total unadjusted error includes offset, full-scale, linearity, and multiplexer errors.

6. The most significant-bit-first data is output directly from the comparator and therefore requires additional delay to allow for comparator response time. Least-significant-bit-first data applies only to ADC0832.



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PARAMETER MEASUREMENT INFORMATION

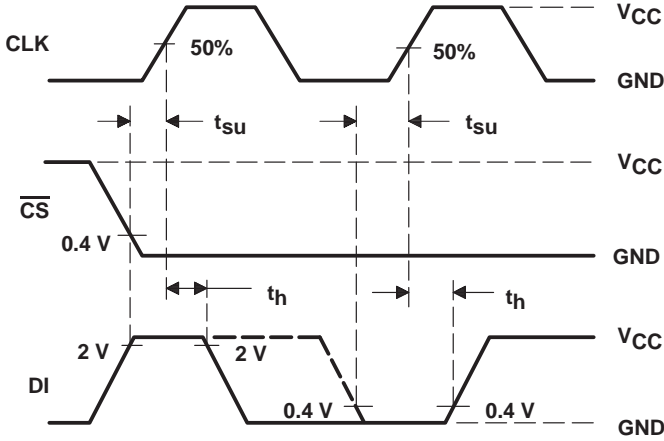


Figure 1. ADC0832 Data Input Timing

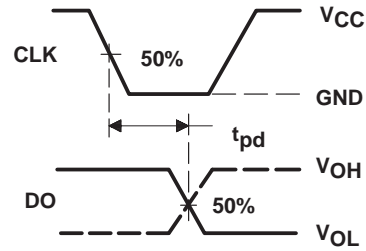
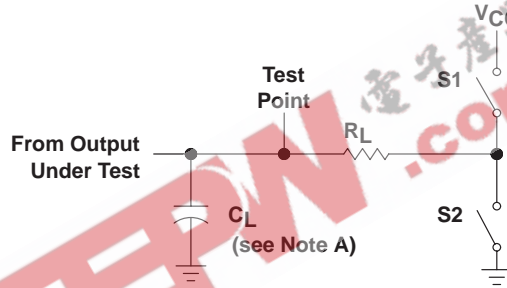
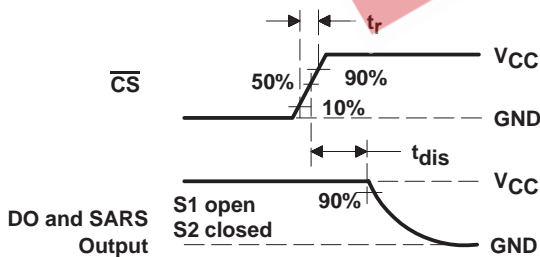


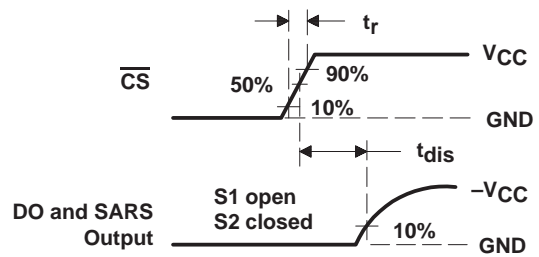
Figure 2. Data Output Timing



LOAD CIRCUIT



VOLTAGE WAVEFORMS

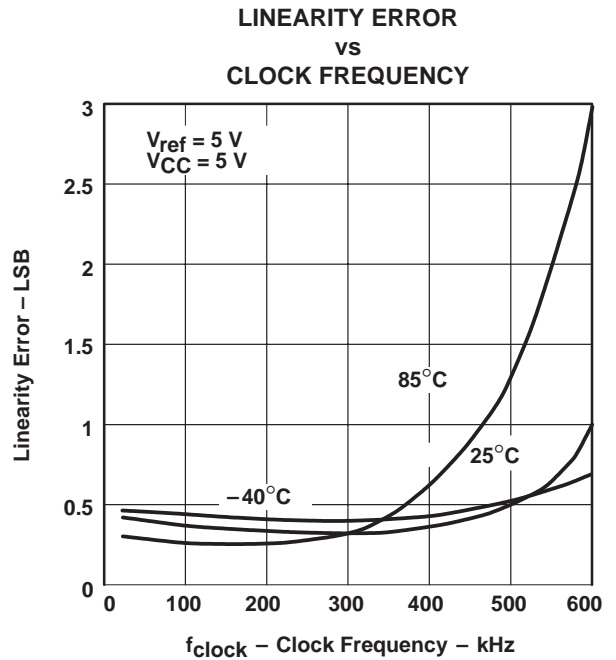
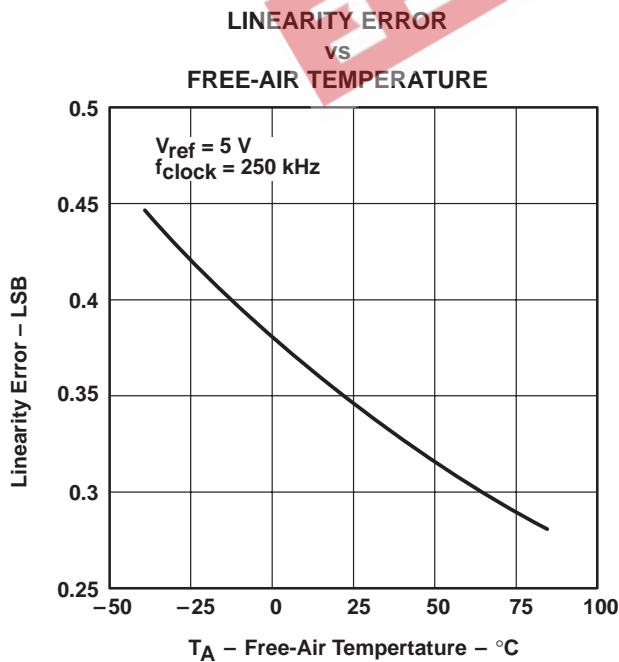
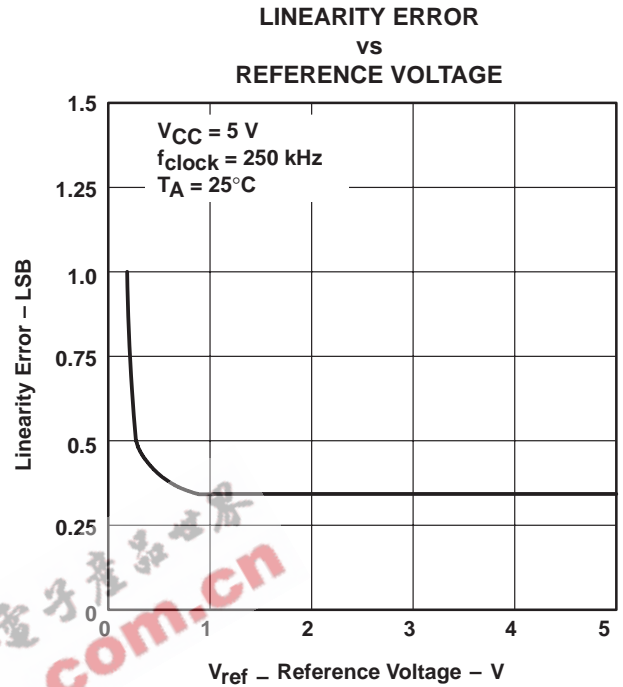
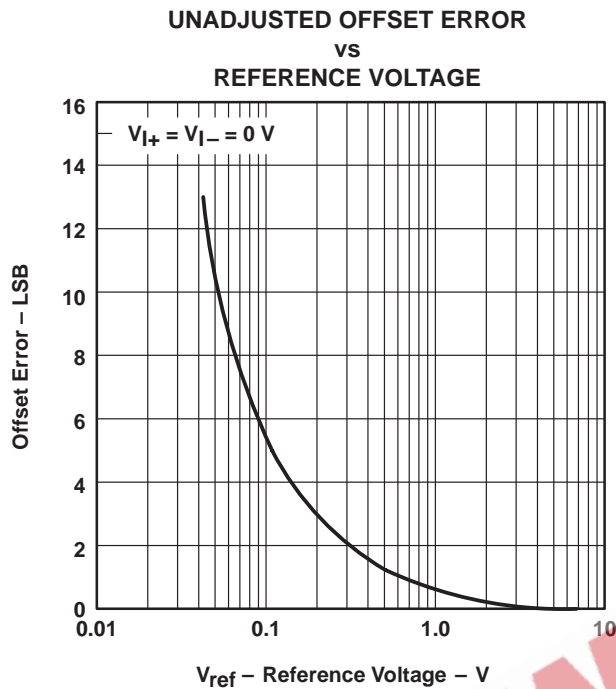


VOLTAGE WAVEFORMS

NOTE A: C_L includes probe and jig capacitance.

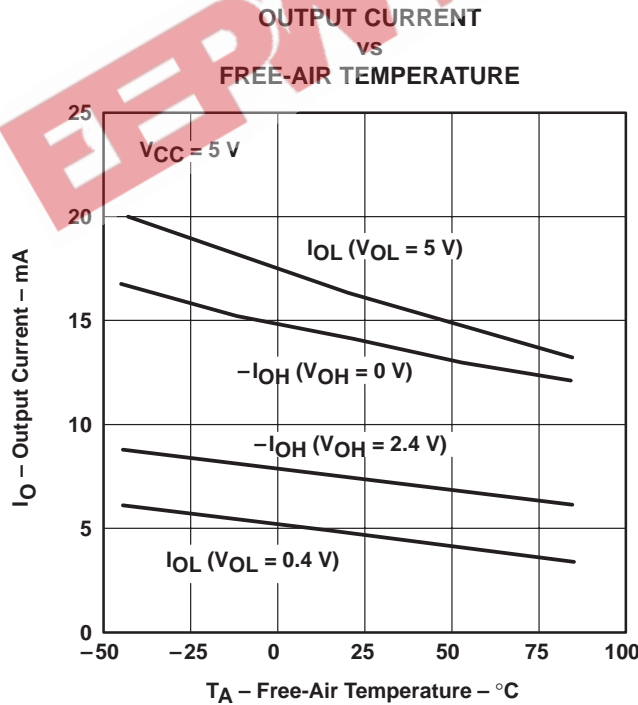
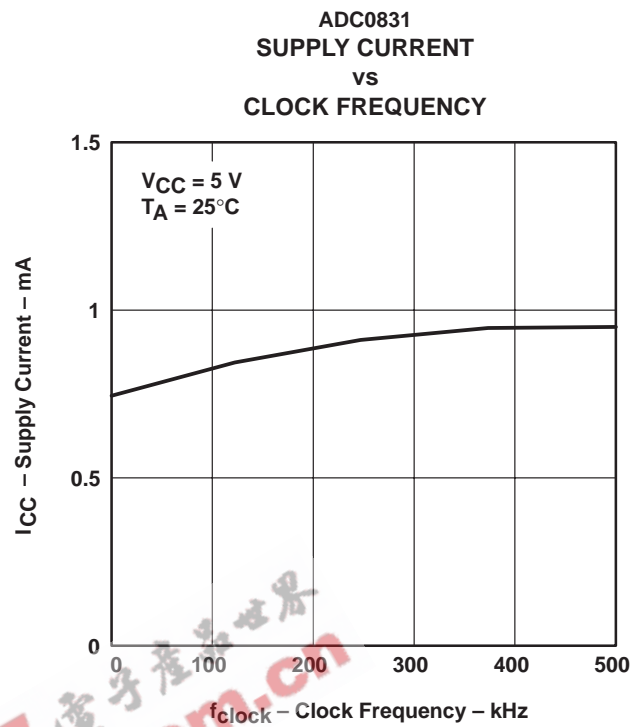
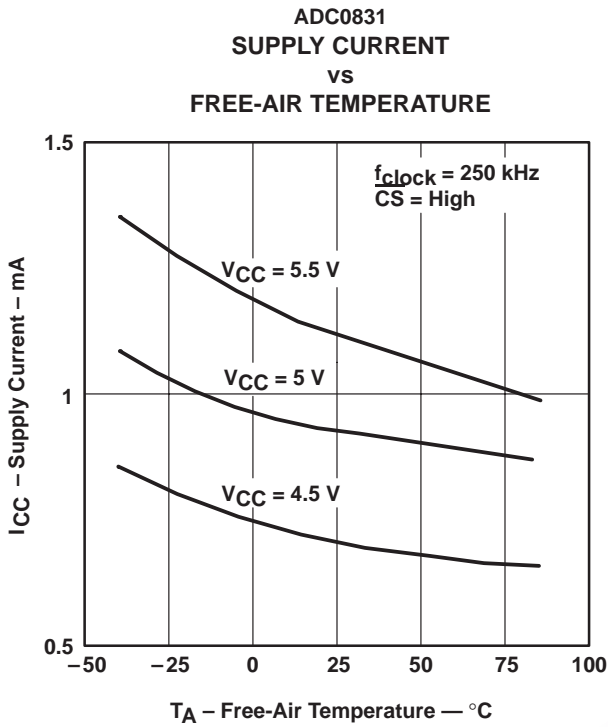
Figure 3. Output Disable Time Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS



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