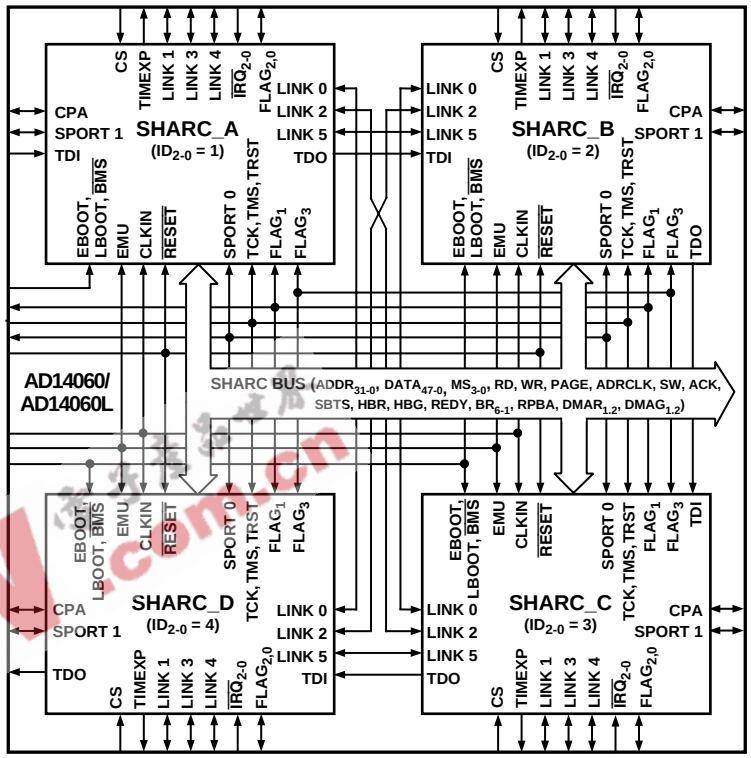
Quad-SHARC® DSP Multiprocessor Family

AD14060/AD14060L

PERFORMANCE FEATURES
ADSP-21060 Core Processor (. . . ×4)
480 MFLOPS Peak, 320 MFLOPS Sustained
25 ns Instruction Rate, Single-Cycle Instruction Execution–Each of Four Processors
16 Mbit Shared SRAM (Internal to SHARCs)
4 Gigawords Addressable Off-Module Memory
Twelve 40 Mbyte/s Link Ports (Three per SHARC)
Four 40 Mbit/s Independent Serial Ports (One from Each SHARC)
One 40 Mbit/s Common Serial Port
5 V and 3.3 V Operation
32-Bit Single Precision and 40-Bit Extended Precision IEEE Floating Point Data Formats, or 32-Bit Fixed Point Data Format
IEEE JTAG Standard 1149.1 Test Access Port and On-Chip Emulation

PACKAGING FEATURES
308-Lead Ceramic Quad Flatpack (CQFP)
2.05" (52 mm) Body Size
Cavity Up or Down, Configurable
Low Profile, 0.160" Height
Hermetic
25 Mil (0.65 mm) Lead Pitch
29 Grams (typical)
θ_{JC} = 0.36°C/W

FUNCTIONAL BLOCK DIAGRAM



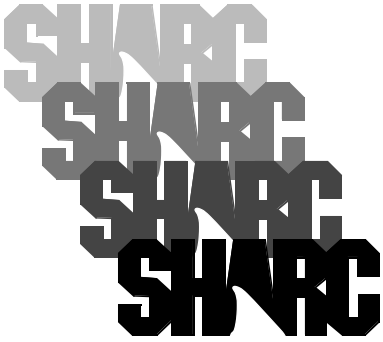
GENERAL DESCRIPTION

The AD14060/AD14060L Quad-SHARC is the first in a family of high performance DSP multiprocessor modules. The core of the multiprocessor is the ADSP-21060 DSP microcomputer. The AD14060/AD14060L modules have the highest performance —density and lowest cost—performance ratios of any in their class. They are ideal for applications requiring higher levels of performance and/or functionality per unit area.

The AD14060/AD14060L takes advantage of the built-in multiprocessing features of the ADSP-21060 to achieve 480 peak MFLOPS with a single chip type, in a single package. The on-chip SRAM of the DSPs provides 16 Mbits of on-module shared SRAM. The complete shared bus (48 data, 32 address) is also brought off-module for interfacing with expansion memory or other peripherals.

The ADSP-21060 link ports are interconnected to provide direct communication among the four SHARCs as well as high speed off-module access. Internally, each SHARC has a direct link port connection. Externally, each SHARC has a total of 120 Mbytes/s link port bandwidth.

Multiprocessor performance is enhanced with embedded power and ground planes, matched impedance interconnect, and optimized signal routing lengths and separation. The fully tested and ready-to-insert multiprocessor also significantly reduces board space.



REV. A

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DETAILED DESCRIPTION

Architectural Features

ADSP-21060 Core

The AD14060/AD14060L is based on the powerful ADSP-21060 (SHARC) DSP chip. The ADSP-21060 SHARC combines a high performance floating-point DSP core with integrated, on-chip system features including a 4 Mbit SRAM memory, host processor interface, DMA controller, serial ports, and both link port and parallel bus connectivity for glueless DSP multiprocessing, (see Figure 1). It is fabricated in a high speed, low power CMOS process, and has a 25 ns instruction cycle time. The arithmetic/ logic unit (ALU), multiplier and shifter all perform single-cycle instructions, and the three units are arranged in parallel, maximizing computational throughput.

The SHARC features an enhanced Harvard architecture in which the data memory (DM) bus transfers data, and the program memory (PM) bus transfers both instructions and data. There is also an on-chip instruction cache which selectively caches only those instructions whose fetches conflict with the PM bus data accesses. This combines with the separate program and data memory buses to enable three-bus operation for fetching an instruction and two operands, all in a single cycle. The SHARC also contains a general purpose data register file, which is a 10-port, 32-register (16 primary, 16 secondary) file. Each SHARC's core also implements two data address generators (DAGs), implementing circular data buffers in hardware. The DAGs contain sufficient registers to allow the creation of up to 32 circular buffers. The 48-bit instruction word accommodates a variety of parallel operations, for concise programming. For example, the ADSP-21060 can conditionally execute a multiply, an add, a subtract, and a branch, all in a single instruction.

The SHARCs contain 4 Mbits of on-chip SRAM each, organized as two blocks of 2 Mbits, which can be configured for different combinations of code and data storage. The memory can be configured as a maximum of 128K words of 32-bit data, 256K words of 16-bit data, 80K words of 48-bit instructions (or 40-bit data), or combinations of different word sizes up to 4 megabits. A 16-bit floating-point storage format is supported which effectively doubles the amount of data that may be stored on chip. Conversion between the 32-bit floating point and 16-bit floating point formats is done in a single instruction. Each memory block is dual-ported for single-cycle, independent accesses by the core processor and I/O processor or DMA controller. The dual-ported memory and separate on-chip buses allow two data transfers from the core and one from I/O, all in a single cycle.

Shared Memory Multiprocessing

The AD14060/AD14060L takes advantage of the powerful multiprocessing features built into the SHARC. The SHARCs are connected to maximize the performance of this cluster-of-four architecture, and still allow for off-module expansion. The AD14060/AD14060L in itself is a complete shared memory multiprocessing system, as shown in Figure 3. The unified address space of the SHARCs allows direct interprocessor accesses of each SHARCs' internal memory. In other words, each SHARC can directly access the internal memory and IOP registers of each of the other SHARCs by simply reading or writing to the appropriate address in multiprocessor memory space (see Figure 2)—this is called a *direct read or direct write.*

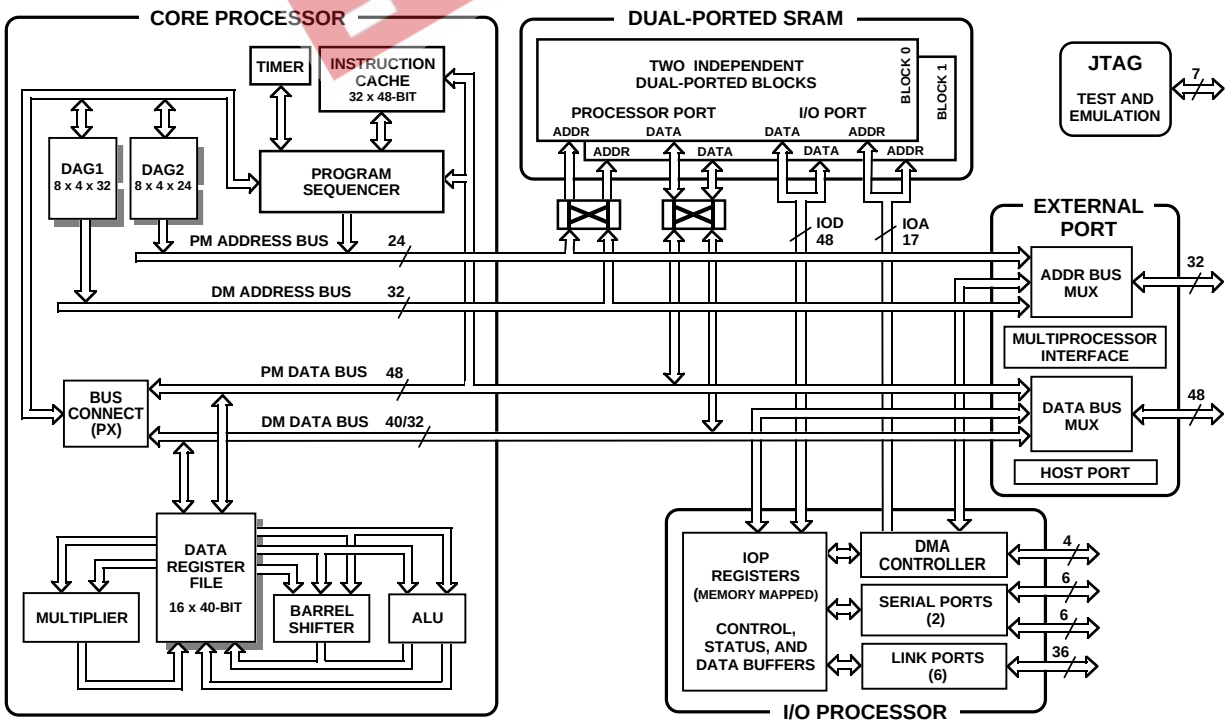

Figure 1. ADSP-21060 Processor Block Diagram (Core of the AD14060)

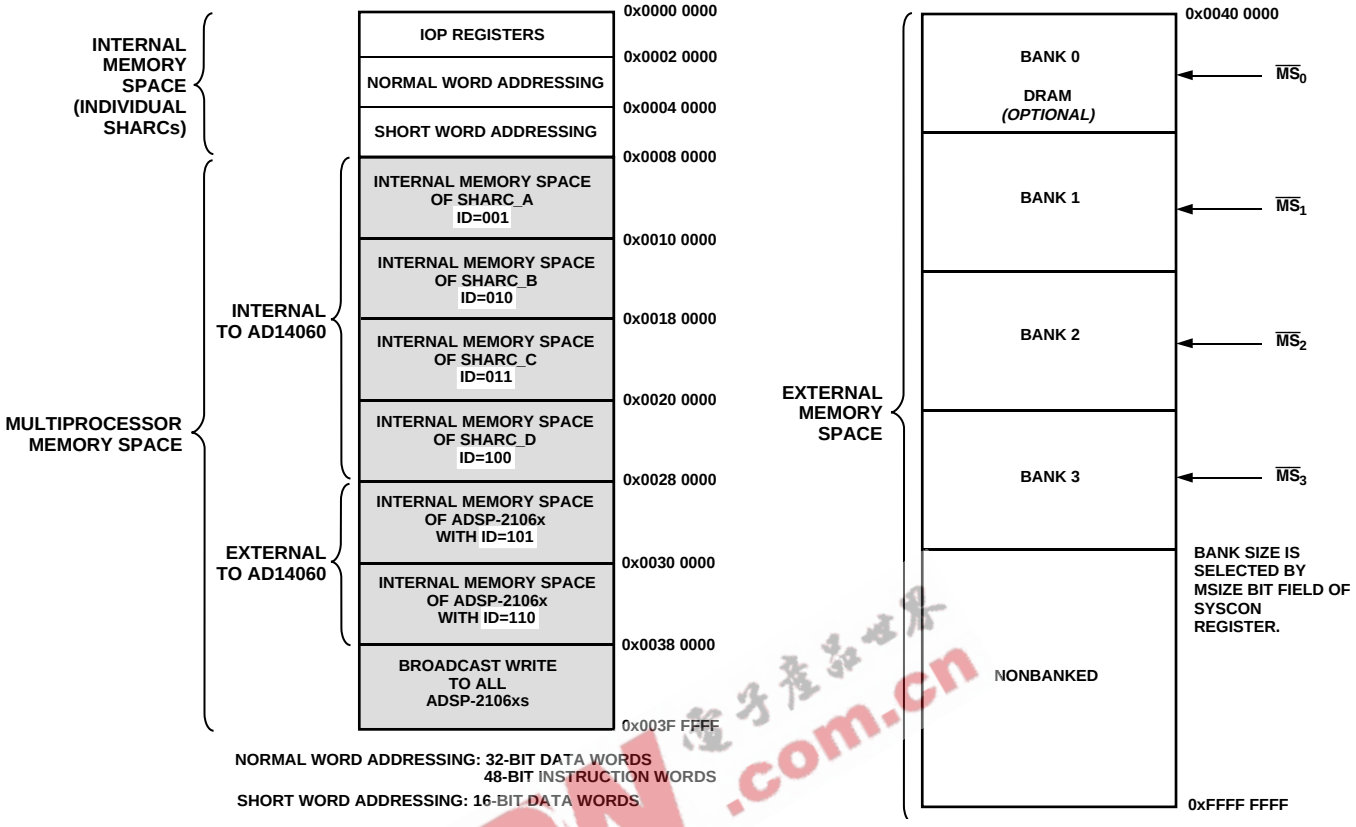

Figure 2. AD14060/AD14060L Memory Map

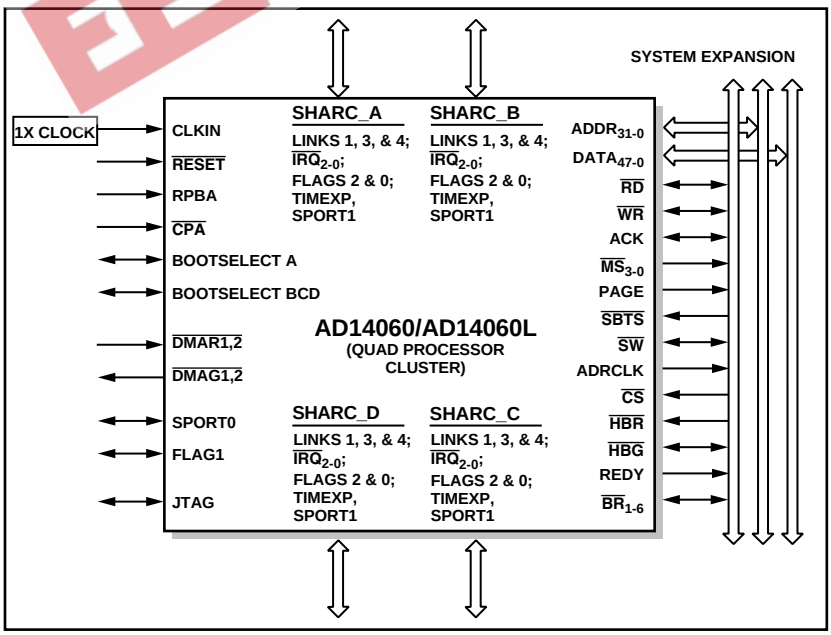

Figure 3. Complete Shared Memory Multiprocessing System

Bus arbitration is accomplished with the on-SHARC arbitration logic. Each SHARC has a unique ID, and drives the Bus-Request (BR) line corresponding to its ID, while monitoring all others. $\overline{BR}$1–$\overline{BR}$4 are used within the AD14060/AD14060L, while $\overline{BR}$5 and $\overline{BR}$6 can be used for expansion. All bus requests ($\overline{BR}$1–$\overline{BR}$6) are included in the module I/O.

Two different priority schemes, fixed and rotating, are available to resolve competing bus requests. The RPBA pin selects which scheme is used: when RPBA is high, rotating priority bus arbitration is selected, and when RPBA is low, fixed priority is selected.

Table I. Rotating Priority Arbitration Example

	Hardware Processor IDs						
Cycle	**ID1**	**ID2**	**ID3**	**ID4**	**ID5**	**ID6**	
1	M	1	2 BR	3	4	5	*Initial Priority Assignments*
2	4	5 BR	M-BR	1	2	3	
3	4	5 BR	M	1	2	3	
4	5 BR	M	1	2	3	4 BR	
5	1 BR	2	3	4	5	M	*Final Priority Assignments*

NOTES
1–5 = Assigned Priority.
M = Bus Mastership (in that cycle).
BR = Requesting Bus Mastership with BRx.

Bus mastership is passed from one SHARC to another during a *bus transition cycle*. A bus transition cycle only occurs when the current bus master deasserts its BR line and one of the slave SHARCs asserts its BR line. The bus master can therefore retain bus mastership by keeping its BR line asserted. When the bus master deasserts its BR line, and no other BR line is asserted, then the master will not lose any bus cycles. When more than one SHARC asserts its BR line, the SHARC with the highest priority request becomes bus master on the following cycle. Each SHARC observes all of the BR lines, and therefore tracks when a bus transition cycle has occurred, and which processor has become the new bus master. Master processor changeover incurs only one cycle of overhead. An example bus transition sequence is shown in Table I.

Bus locking is possible, allowing indivisible read-modify-write sequences for semaphores. In either the fixed or rotating priority scheme, it is also possible to limit the number of cycles the master can control the bus. The AD14060/AD14060L also provides the option of using the Core Priority Access (CPA) mode of the SHARC. Using the CPA signal allows external bus accesses by the core processor of a slave SHARC to take priority over ongoing DMA transfers. Also, each SHARC can broadcast write to all other SHARCs simultaneously, allowing the implementation of reflective semaphores.

The bus master can communicate with slave SHARCs by writing messages to their internal IOP registers. The MSRG0–MSRG7 registers are general-purpose registers that can be used for convenient message passing, semaphores and resource sharing between the SHARCs. For message passing, the master communicates with a slave by writing and/or reading any of the eight message registers on the slave. For vector interrupts, the master can issue a vector interrupt to a slave by writing the address of an interrupt service routine to the slave's VIRPT register. This causes an immediate high priority interrupt on the slave which, when serviced, will cause it to branch to the specified service routine.

Off-Module Memory and Peripherals Interface

The AD14060/AD14060L's external port provides the interface to off-module memory and peripherals (see Figure 5). This port consists of the complete external port bus of the SHARC, bused together in common among the four SHARCs.

The 4-gigaword off-module address space is included in the ADSP-14060's unified address space. Addressing of external memory devices is facilitated by each SHARC internally decoding the high order address lines to generate memory bank select signals. Separate control lines are also generated for simplified addressing of page-mode DRAM. The AD14060/AD14060L also supports programmable memory wait states and external memory acknowledge controls to allow interfacing to DRAM and peripherals with variable access, hold and disable time requirements.

Link Port I/O

Each individual SHARC features six 4-bit link ports that facilitate SHARC-to-SHARC communication and external I/O interfacing. Each link port can be configured for either 1× or 2× operation, allowing each to transfer either 4 or 8 bits per cycle. The link ports can operate independently and simultaneously, with a maximum bandwidth of 40 MBytes/s each, or a total of 240 MBytes/s per SHARC.

The AD14060/AD14060L optimizes the link port connections internally, and brings a total of twelve of the link ports off-module for user-defined system connections. Internally, each SHARC has a connection to the other three SHARCs with a dedicated link port interface. Thus, each SHARC can directly interface with its nearest and next-nearest neighbor. The remaining three link ports from each SHARC are brought out independently from each SHARC. A maximum of 480 MBytes/s link port bandwidth is then available off of the AD14060/AD14060L. The link port connections are detailed in Figure 4.

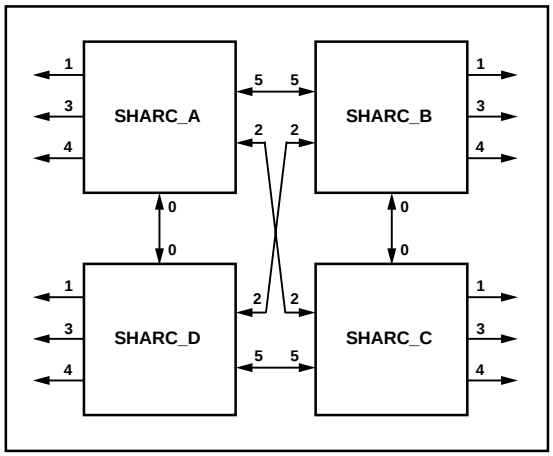

Figure 4. Link Port Connections

Link port 4, the boot link port, is brought off independently from each SHARC. Individual booting is then allowed, or chained link port booting is possible as described under "Link Port Booting."

Link port data is packed into 32-bit or 48-bit words, and can be directly read by the SHARC core processor or DMA-transferred to on-SHARC memory.

Each link port has its own double-buffered input and output registers. Clock/acknowledge handshaking controls link port transfers. Transfers are programmable as either transmit or receive.

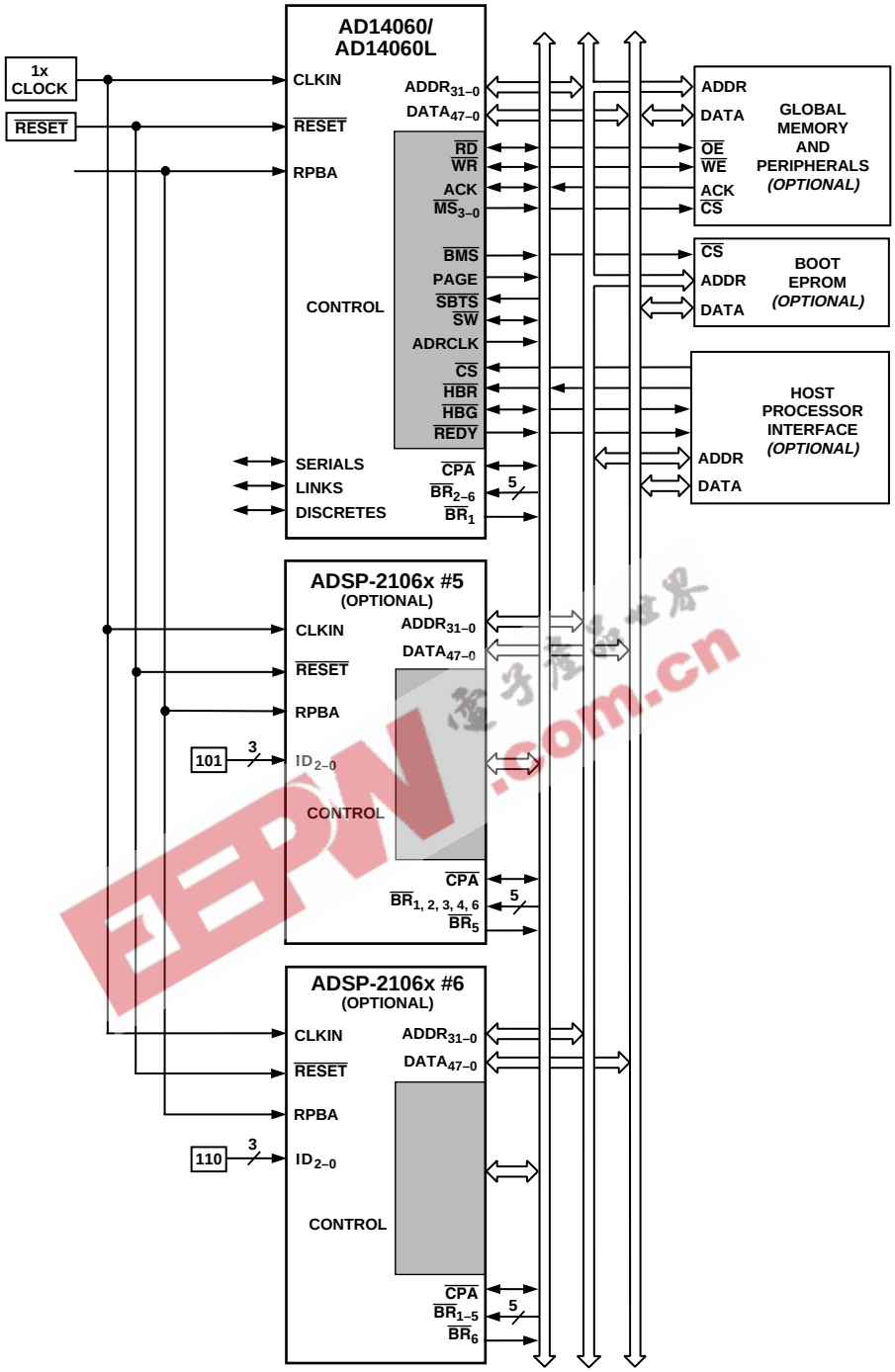

Figure 5. Optional System Interconnections

Serial Ports
The SHARC serial ports provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices. Each SHARC has two serial ports. The AD14060/AD14060L provides direct access to Serial Port 1 of each SHARC. Serial Port 0 is bused together in common to each SHARC, and brought off-module.

The serial ports can operate at the full clock rate of the module, providing each with a maximum data rate of 40 Mbit/s. Independent transmit and receive functions provide more flexible communications. Serial port data can be automatically transferred to and from on-SHARC memory via DMA, and each of the serial ports offers time division multiplexed (TDM) multichannel mode.

The serial ports can operate with little-endian or big-endian transmission formats, with word lengths selectable from 3 bits to 32 bits. They offer selectable synchronization and transmit modes as well as optional µ-law or A-law companding. Serial port clocks and frame syncs can be internally or externally generated.

Program Booting
The AD14060/AD14060L supports automatic downloading of programs following power-up or a software reset. The SHARC offers four options for program booting: 1) from an 8-bit EPROM; 2) from a host processor; 3) through the link ports; and 4) no-boot. In no-boot mode, the SHARC starts executing instructions from address 0x0040 0004 in external memory. The boot mode is selected by the state of the following signals: BMS, EBOOT, and LBOOT.

On the AD14060/AD14060L, SHARC_A's boot mode is separately controlled, while SHARCs B, C, and D are controlled as a group. With this flexibility, the AD14060/AD14060L can be configured to boot in any of the following methods.

Multiprocessor Host Booting
To boot multiple ADSP-21060 processors from a host, each ADSP-21060 must have its EBOOT, LBOOT and BMS pins configured for host booting: EBOOT = 0, LBOOT = 0, and BMS = 1. After system power-up, each ADSP-21060 will be in the idle state and the $\overline{BR}$x bus request lines will be deasserted. The host must assert the $\overline{HBR}$ input and boot each ADSP-21060 by asserting its CS pin and downloading instructions.

Multiprocessor EPROM Booting
There are two methods of booting the multiprocessor system from an EPROM.

SHARC_A Is Booted, Which Then Boots the Others. The EBOOT pin on the SHARC_A must be set high for EPROM booting. All other ADSP-21060s should be configured for host booting (EBOOT = 0, LBOOT = 0, and BMS = 1), which leaves them in the idle state at start-up and allows SHARC_A to become bus master and boot itself. Only the BMS pin of SHARC_A is connected to the chip select of the EPROM. When SHARC_A has finished booting, it can boot the remaining ADSP-21060s by writing to their external port DMA buffer 0 (EPB0) via multiprocessor memory space.

All ADSP-21060s Boot in Turn From a Single EPROM.
The BMS signals from each ADSP-21060 may be wire-ORed together to drive the chip select pin of the EPROM. Each ADSP-21060 can boot in turn, according to its priority. When the last one has finished booting, it must inform the others (which may be in the idle state) that program execution can begin.

Multiprocessor Link Port Booting
Booting can also be accomplished from a single source through the link ports. Link Buffer 4 must always be used for booting. To simultaneously boot all of the ADSP-21060s, a parallel common connection is available through Link Port 4 on each of the processors. Or, using the daisy chain connection that exists between the processors' link ports, each ADSP-21060 can boot the next one in turn. In this case, the Link Assignment Register (LAR) must be programmed to configure the internal link ports with Link Buffer 4.

Multiprocessor Booting From External Memory
If external memory contains a program after reset, then SHARC_A should be set up for *no boot* mode; it will begin executing from address 0x0040 0004 in external memory. When booting has completed, the other ADSP-21060s may be booted by SHARC_A if they are set up for host booting, or they can begin executing out of external memory if they are set up for *no boot* mode. Multiprocessor bus arbitration will allow this booting to occur in an orderly manner.

Host Processor Interface
The AD14060/AD14060L's host interface allows for easy connection to standard microprocessor buses, both 16-bit and 32-bit, with little additional hardware required. Asynchronous transfers at speeds up to the full clock rate of the module are supported. The host interface is accessed through the AD14060/AD14060L external port and is memory-mapped into the unified address space. Four channels of DMA are available for the host interface; code and data transfers are accomplished with low software overhead.

The host processor requests the AD14060/AD14060L's external bus with the host bus request ($\overline{HBR}$), host bus grant ($\overline{HBG}$), and ready (REDY) signals. The host can directly read and write the internal memory of the SHARCs, and can access the DMA channel setup and mailbox registers. Vector interrupt support is provided for efficient execution of host commands.

Direct Memory Access (DMA) Controller
The SHARCs on-chip DMA control logic allows zero-overhead data transfers without processor intervention. The DMA controller operates independently and invisibly to each SHARCs processor core, allowing DMA operations to occur while the core is simultaneously executing its program instructions.

DMA transfers can occur between SHARC internal memory and either external memory, external peripherals, or a host processor. DMA transfers can also occur between the SHARC's internal memory and its serial ports or link ports. DMA transfers between external memory and external peripheral devices are another option. External bus packing to 16-, 32- or 48-bit words is performed during DMA transfers.

Ten channels of DMA are available on the SHARCs—two via the link ports, four via the serial ports, and four via the processor's external port (for either host processor, other SHARCs, memory, or I/O transfers). Four additional link port DMA channels are shared with serial port 1 and the external port. Programs can be downloaded to the SHARCs using DMA transfers. Asynchronous off-module peripherals can control two DMA channels using DMA Request/Grant lines ($\overline{DMAR1\text{-}2}$, $\overline{DMAG1\text{-}2}$). Other DMA features include interrupt generation upon completion of DMA transfers and DMA chaining for automatic linked DMA transfers.

Development Tools

The ADSP-14060 is supported with a complete set of software and hardware development tools, including an EZ-LAB® In-Circuit Emulator, and development software.

Analog Devices' ADSP-21000 Family Development Software includes an easy to use Assembler based on an algebraic syntax, an Assembly Library/Librarian, a Linker, an Instruction-Level Simulator, an ANSI C optimizing Compiler, the CBug™ C Source-Level Debugger, and a C Runtime Library including DSP and mathematical functions. The Optimizing Compiler includes Numerical C extensions based on the work of the ANSI Numerical C Extensions Group. Numerical C provides extensions to the C language for array selection, vector math operations, complex data types, circular pointers and variably dimensioned arrays. The ADSP-21000 Family Development Software is available for both the PC and Sun platforms.

The SHARC EZ-KIT combines the ADSP-21000 Family Development Software for the PC and the EZ-LAB Development Board in one package.

The ADSP-2106x EZ-ICE® Emulator uses the IEEE 1149.1 JTAG test access port of the ADSP-2106x processor to monitor and control the target board processor during emulation. The EZ-ICE provides full-speed emulation, allowing inspection and modification of memory, registers and processor stacks.

Nonintrusive in-circuit emulation is assured by the use of the processor's JTAG interface—the emulator does not affect target system loading or timing.

Further details and ordering information are available in the *ADSP-21000 Family Hardware & Software Development Tools* data sheet (ADDS-2100xx-TOOLS). This data sheet can be requested from any Analog Devices sales office or distributor, or from the Literature Center.

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CBug is a trademark of Analog Devices, Inc.

In addition to the software and hardware development tools available from Analog Devices, third parties provide a wide range of tools supporting the SHARC processor family. Hardware tools include SHARC PC plug-in cards, multiprocessor SHARC VME boards, and daughter card modules with multiple SHARCs and additional memory. These modules are based on the SHARCPAC module specification. Third party software tools include an Ada compiler, DSP libraries, operating systems and block diagram design tools.

Quad-SHARC Development Board

The BlackTip-MCM, AD14060 development board and software, is available from Bittware Research Systems, Inc. This board has one AD14060 BITSI interface, PROM and SRAM expansion options on an ISA card. It is supported by Bittware's SHARC software development package. Bittware can be contacted at 1-800-848-0436.

Other Package Details

The AD14060/AD14060L contains 16 on-module 0.018 microfarad bypass capacitors. It is recommended that in the target system at least four additional capacitors, of 0.018 microfarad value, be placed around the module—one near each of the four corners.

The top surface, lid, of the AD14060/AD14060L is electrically connected to GND on the industrial and military grade parts.

Additional Information

This data sheet provides a general overview of the AD14060/AD14060L architecture and functionality. For detailed information on the ADSP-2106x SHARC and the ADSP-21000 Family core architecture and instruction set, refer to the ADSP-2106x SHARC *User's Manual.*

PIN FUNCTION DESCRIPTIONS

AD14060/AD14060L pin definitions are listed below. Inputs identified as synchronous (S) must meet timing requirements with respect to CLKIN (or with respect to TCK for TMS, TDI). Inputs identified as asynchronous (A) can be asserted asynchronously to CLKIN (or to TCK for $\overline{\text{TRST}}$).

Unused inputs should be tied or pulled to V_{DD} or GND, except for $ADDR_{31-0}$, $DATA_{47-0}$, $FLAG_{2-0}$, $\overline{\text{SW}}$, and inputs that have internal pull-up or pull-down resistors (CPA, ACK, DTx, DRx, TCLKx, RCLKx, $LxDAT_{3-0}$, LxCLK, LxACK, TMS and TDI)—these pins can be left floating. These pins have a logic-level hold circuit that prevents the input from floating internally.

I = Input P = Power Supply (A/D) = Active Drive
O = Output S = Synchronous (O/D) = Open Drain
G = Ground A = Asynchronous
T = Three-State (when $\overline{\text{SBTS}}$ is asserted, or when the AD14060/AD14060L is a bus slave)

Pin	Type	Function
$ADDR_{31-0}$	I/O/T	**External Bus Address.** (Common to all SHARCs) The AD14060/AD14060L outputs addresses for external memory and peripherals on these pins. In a multiprocessor system, the bus master outputs addresses for read/writes on the internal memory or IOP registers of slave ADSP-2106xs. The AD14060/AD14060L inputs addresses when a host processor or multiprocessing bus master is reading or writing the internal memory or IOP registers of internal ADSP-21060s.
$DATA_{47-0}$	I/O/T	**External Bus Data**. (Common to all SHARCs) The AD14060/AD14060L inputs and outputs data and instructions on these pins. 32-bit single-precision floating-point data and 32-bit fixed-point data is transferred over bits 47-16 of the bus. 40-bit extended-precision floating-point data is transferred over bits 47-8 of the bus. 16-bit short word data is transferred over bits 31-16 of the bus. In PROM boot mode, 8-bit data is transferred over bits 23-16. Pull-up resistors on unused DATA pins are not necessary.
$\overline{\text{MS}}_{3-0}$	O/T	**Memory Select Lines.** (Common to all SHARCs) These lines are asserted (low) as chip selects for the corresponding banks of external memory. Memory bank size must be defined in the individual ADSP-21060's system control registers (SYSCON). The $\overline{\text{MS}}_{3-0}$ lines are decoded memory address lines that change at the same time as the other address lines. When no external memory access is occurring the $\overline{\text{MS}}_{3-0}$ lines are inactive; they are active, however, when a conditional memory access instruction is executed, whether or not the condition is true. $\overline{\text{MS}}_0$ can be used with the PAGE signal to implement a bank of DRAM memory (Bank 0). In a multiprocessing system, the $\overline{\text{MS}}_{3-0}$ lines are output by the bus master.
$\overline{\text{RD}}$	I/O/T	**Memory Read Strobe.** (Common to all SHARCs) This pin is asserted (low) when the AD14060/AD14060L reads from external devices or when the internal memory of internal ADSP-2106xs is being accessed. External devices (including other ADSP-2106xs) must assert $\overline{\text{RD}}$ to read from the AD14060/AD14060L's internal memory. In a multiprocessing system, $\overline{\text{RD}}$ is output by the bus master and is input by all other ADSP-2106xs.
$\overline{\text{WR}}$	I/O/T	**Memory Write Strobe.** (Common to all SHARCs) This pin is asserted (low) when the AD14060/AD14060L writes to external devices or when the internal memory of internal ADSP-2106xs is being accessed. External devices (including other ADSP-2106xs) must assert $\overline{\text{WR}}$ to write to the AD14060/AD14060L's internal memory. In a multiprocessing system $\overline{\text{WR}}$ is output by the bus master and is input by all other ADSP-2106xs.
PAGE	O/T	**DRAM Page Boundary.** (Common to all SHARCs) The AD14060/AD14060L asserts this pin to signal that an external DRAM page boundary has been crossed. DRAM page size must be defined in the individual ADSP-21060's memory control register (WAIT). DRAM can only be implemented in external memory Bank 0; the PAGE signal can only be activated for Bank 0 accesses. In a multiprocessing system, PAGE is output by the bus master.
ADRCLK	O/T	**Clock Output Reference.** (Common to all SHARCs) In a multiprocessing system, ADRCLK is output by the bus master.
$\overline{\text{SW}}$	I/O/T	**Synchronous Write Select.** (Common to all SHARCs) This signal is used to interface the AD14060/AD14060L to synchronous memory devices (including other ADSP-2106xs). The AD14060/AD14060L asserts $\overline{\text{SW}}$ (low) to provide an early indication of an impending write cycle, which can be aborted if $\overline{\text{WR}}$ is not later asserted (e.g., in a conditional write instruction). In a multiprocessing system, $\overline{\text{SW}}$ is output by the bus master and is input by all other ADSP-2106xs to determine if the multiprocessor memory access is a read or write. $\overline{\text{SW}}$ is asserted at the same time as the address output. A host processor using synchronous writes must assert this pin when writing to the AD14060/AD14060L.
ACK	I/O/S	**Memory Acknowledge.** (Common to all SHARCs) External devices can deassert ACK (low) to add wait states to an external memory access. ACK is used by I/O devices, memory controllers, or other peripherals to hold off completion of an external memory access. The AD14060/AD14060L deasserts ACK, as an output, to add wait states to a synchronous access of its internal memory. In a multiprocessing system, a slave ADSP-2106x deasserts the bus master's ACK input to add wait state(s) to an access of its internal memory. The bus master has a keeper latch on its ACK pin that maintains the input at the level it was last driven to.

Pin	Type	Function
$\overline{\text{SBTS}}$	I/S	**Suspend Bus Three-State.** (Common to all SHARCs) External devices can assert $\overline{\text{SBTS}}$ (low) to place the external bus address, data, selects, and strobes in a high impedance state for the following cycle. If the AD14060/AD14060L attempts to access external memory while $\overline{\text{SBTS}}$ is asserted, the processor will halt and the memory access will not be completed until $\overline{\text{SBTS}}$ is deasserted. $\overline{\text{SBTS}}$ should only be used to recover from host processor/AD14060/AD14060L deadlock, or used with a DRAM controller.
$\overline{\text{HBR}}$	I/A	**Host Bus Request.** (Common to all SHARCs) Must be asserted by a host processor to request control of the AD14060/AD14060L's external bus. When $\overline{\text{HBR}}$ is asserted in a multiprocessing system, the ADSP-2106x that is bus master will relinquish the bus and assert $\overline{\text{HBG}}$. To relinquish the bus, the ADSP-2106x places the address, data, select, and strobe lines in a high impedance state. $\overline{\text{HBR}}$ has priority over all ADSP-2106x bus requests ($\overline{\text{BR}}_{6-1}$) in a multiprocessing system.
$\overline{\text{HBG}}$	I/O	**Host Bus Grant.** (Common to all SHARCs) Acknowledges an $\overline{\text{HBR}}$ bus request, indicating that the host processor may take control of the external bus. $\overline{\text{HBG}}$ is asserted (held low) by the AD14060/AD14060L until $\overline{\text{HBR}}$ is released. In a multiprocessing system, $\overline{\text{HBG}}$ is output by the ADSP-2106x bus master and is monitored by all others.
$\overline{\text{CSA}}$	I/A	**Chip Select.** Asserted by host processor to select SHARC_A.
$\overline{\text{CSB}}$	I/A	**Chip Select.** Asserted by host processor to select SHARC_B.
$\overline{\text{CSC}}$	I/A	**Chip Select.** Asserted by host processor to select SHARC_C.
$\overline{\text{CSD}}$	I/A	**Chip Select.** Asserted by host processor to select SHARC_D.
REDY (O/D)	O	**Host Bus Acknowledge.** (Common to all SHARCs) The AD14060/AD14060L deasserts REDY (low) to add wait states to an asynchronous access of its internal memory or IOP registers by a host. Open drain output (O/D) by default; can be programmed in ADREDY bit of SYSCON register of individual ADSP-21060s to be active drive (A/D). REDY will only be output if the CS and $\overline{\text{HBR}}$ inputs are asserted.
$\overline{\text{BR}}_{6-1}$	I/O/S	**Multiprocessing Bus Requests.** (Common to all SHARCs) Used by multiprocessing ADSP-2106xs to arbitrate for bus mastership. An ADSP-2106x only drives its own $\overline{\text{BR}}$x line (corresponding to the value of its ID2-0 inputs) and monitors all others. In a multiprocessor system with less than six ADSP-2106xs, the unused $\overline{\text{BR}}$x pins should be pulled high; $\overline{\text{BR}}_{4-1}$ must not be pulled high or low because they are outputs.
RPBA	I/S	**Rotating Priority Bus Arbitration Select.** (Common to all SHARCs) When RPBA is high, rotating priority for multiprocessor bus arbitration is selected. When RPBA is low, fixed priority is selected. This signal is a system configuration selection that must be set to the same value on every ADSP-2106x. If the value of RPBA is changed during system operation, it must be changed in the same CLKIN cycle on every ADSP-2106x.
$\overline{\text{CPA}}$y (O/D)	I/O	**Core Priority Access.** (y = SHARC_A, B, C, D) Asserting its CPA pin allows the core processor of an ADSP-2106x bus slave to interrupt background DMA transfers and gain access to the external bus. CPA is an open drain output that is connected to all ADSP-2106x in the system if this function is required. The CPA pin of each internal ADSP-21060 is brought out individually. The CPA pin has an internal 5 kΩ pull-up resistor. If core access priority is not required in a system, the CPA pin should be left unconnected.
DT0	O/T	**Data Transmit** (Common Serial Ports 0 to all SHARCs, TDM). DT pin has a 50 kΩ internal pull-up resistor.
DR0	I	**Data Receive** (Common Serial Ports 0 to all SHARCs, TDM). DR pin has a 50 kΩ internal pull-up resistor.
TCLK0	I/O	**Transmit Clock** (Common Serial Ports 0 to all SHARCs, TDM). TCLK pin has a 50 kΩ internal pull-up resistor.
RCLK0	I/O	**Receive Clock** (Common Serial Ports 0 to all SHARCs, TDM). RCLK pin has a 50 kΩ internal pull-up resistor.
TFS0	I/O	**Transmit Frame Sync** (Common Serial Ports 0 to all SHARCs, TDM).
RFS0	I/O	**Receive Frame Sync** (Common Serial Ports 0 to all SHARCs, TDM).
DTy1	O/T	**Data Transmit** (Serial Port 1 individual from SHARC_A, SHARC_B, SHARC_C, SHARC_D) DT pin has a 50 kΩ internal pull-up resistor.
DRy1	I	**Data Receive** (Serial Port 1 individual from SHARC_A, SHARC_B, SHARC_C, SHARC_D) DR pin has a 50 kΩ internal pull-up resistor.

Pin	Type	Function
TCLKy1	I/O	**Transmit Clock** (Serial Port 1 individual from SHARC_A, SHARC_B, SHARC_C, SHARC_D) TCLK pin has a 50 kΩ internal pull-up resistor.
RCLKy1	I/O	**Receive Clock** (Serial Port 1 individual from SHARC_A, SHARC_B, SHARC_C, SHARC_D) RCLK pin has a 50 kΩ internal pull-up resistor.
TFSy1	I/O	**Transmit Frame Sync** (Serial Port 1 individual from SHARC_A, SHARC_B, SHARC_C, SHARC_D)
RFSy1	I/O	**Receive Frame Sync** (Serial Port 1 individual from SHARC_A, SHARC_B, SHARC_C, SHARC_D)
FLAGy0	I/O/A	**Flag Pins.** (FLAG0 individual from SHARC_A, SHARC_B, SHARC_C, SHARC_D) Each is configured via control bits as either an input or output. As an input, it can be tested as a condition. As an output, it can be used to signal external peripherals.
FLAG1	I/O/A	**Flag Pins.** (FLAG1 common to all SHARCs) Configured via control bits internal to individual ADSP-21060s as either an input or output. As an input, it can be tested as a condition. As an output, it can be used to signal external peripherals.
FLAGy2	I/O/A	**Flag Pins.** (FLAG2 individual from SHARC_A, SHARC_B, SHARC_C, SHARC_D) Each is configured via control bits as either an input or output. As an input, it can be tested as a condition. As an output, it can be used to signal external peripherals.
$\overline{\text{IRQ}}$y2-0	I/A	**Interrupt Request Lines.** (Individual $\overline{\text{IRQ}}$2-0 from y = SHARC_A, SHARC_B, SHARC_C, SHARC_D) May be either edge-triggered or level-sensitive.
$\overline{\text{DMAR1}}$	I/A	**DMA Request 1** (DMA Channel 7). Common to SHARC_A, SHARC_B, SHARC_C, SHARC_D.
$\overline{\text{DMAR2}}$	I/A	**DMA Request 2** (DMA Channel 8). Common to SHARC_A, SHARC_B, SHARC_C, SHARC_D.
$\overline{\text{DMAG1}}$	O/T	**DMA Grant 1** (DMA Channel 7). Common to SHARC_A, SHARC_B, SHARC_C, SHARC_D.
$\overline{\text{DMAG2}}$	O/T	**DMA Grant 2** (DMA Channel 8). Common to SHARC_A, SHARC_B, SHARC_C, SHARC_D.
LyxCLK	I/O	**Link Port Clock** (y = SHARC_A, B, C, D; x = Link Ports 1, 3, 4)[1]. Each LyxCLK pin has a 50 kΩ internal pull-down resistor which is enabled or disabled by the LPDRD bit of the LCOM register, of the ADSP-20160.
LyxDAT3-0	I/O	**Link Port Data** (y = SHARC_A, B, C, D; x = Link Ports 1, 3, 4)[1]. Each LyxDAT pin has a 50 kΩ internal pull-down resistor which is enabled or disabled by the LPDRD bit of the LCOM register, of the ADSP-21060.
LyxACK	I/O	**Link Port Acknowledge** (y = SHARC_A, B, C, D; x = Link Ports 1, 3, 4)[1]. Each LyxACK pin has a 50 kΩ internal pull-down resistor which is enabled or disabled by the LPDRD bit of the LCOM register, of the ADSP-21060.
EBOOTA	I	**EPROM Boot Select.** (SHARC_A) When EBOOTA is high, SHARC_A is configured for booting from an 8-bit EPROM. When EBOOTA is low, the LBOOTA and $\overline{\text{BMSA}}$ inputs determine booting mode for SHARC_A. See the following table. This signal is a system configuration selection which should be hardwired.
LBOOTA	I	**Link Boot.** When LBOOTA is high, SHARC_A is configured for link port booting. When LBOOTA is low, SHARC_A is configured for host processor booting or no booting. See the following table. This signal is a system configuration selection which should be hardwired.
$\overline{\text{BMSA}}$	I/O/T[2]	**Boot Memory Select.** *Output:* Used as chip select for boot EPROM devices (when EBOOTA = 1, LBOOTA = 0). In a multiprocessor system, $\overline{\text{BMS}}$ is output by the bus master. *Input:* When low, indicates that no booting will occur and that SHARC_A will begin executing instructions from external memory. See the following table. This input is a system configuration selection which should be hardwired.
EBOOTBCD	I	**EPROM Boot Select.** (Common to SHARC_B, SHARC_C, SHARC_D) When EBOOTBCD is high, SHARC_B, C, D are configured for booting from an 8-bit EPROM. When EBOOTBCD is low, the LBOOTBCD and BMSBCD inputs determine booting mode for SHARC_B, C and D. See the following table. This signal is a system configuration selection which should be hardwired.
LBOOTBCD	I	**LINK Boot.** (Common to SHARC_B, SHARC_C, SHARC_D) When LBOOTBCD is high, SHARC_B, C, D are configured for link port booting. When LBOOTBCD is low, SHARC_B, C, D are configured for host processor booting or no booting. See the following table. This signal is a system configuration selection which should be hardwired.

Pin	Type	Function
$\overline{\text{BMSBCD}}$	I/O/T[2]	**Boot Memory Select.** *Output:* Used as chip select for boot EPROM devices (when EBOOTBCD = 1, LBOOTBCD = 0). In a multiprocessor system, $\overline{\text{BMS}}$ is output by the bus master. *Input:* When low, indicates that no booting will occur and that SHARC_B, C, D will begin executing instructions from external memory. See table below. This input is a system configuration selection which should be hardwired.
TIMEXPy	O	**Timer Expired.** (Individual TIMEXP from y = SHARC_A, SHARC_B, SHARC_C, SHARC_D) Asserted for four cycles when the timer is enabled and TCOUNT decrements to zero.
CLKIN	I	**Clock In.** (Common to all SHARCs) External clock input to the AD14060/AD14060L. The instruction cycle rate is equal to CLKIN. CLKIN may not be halted, changed, or operated below the minimum specified frequency.
$\overline{\text{RESET}}$	I/A	**Module Reset.** (Common to all SHARCs) Resets the AD14060/AD14060L to a known state. This input must be asserted (low) at power-up.
TCK	I	**Test Clock (JTAG).** (Common to all SHARCs) Provides an asynchronous clock for JTAG boundary scan.
TMS	I/S	**Test Mode Select (JTAG).** (Common to all SHARCs) Used to control the test state machine. TMS has a 20 kΩ internal pull-up resistor.
TDI	I/S	**Test Data Input (JTAG).** Provides serial data for the boundary scan logic chain starting at SHARC_A. TDI has a 20 kΩ internal pull-up resistor.
TDO	O	**Test Data Output (JTAG).** Serial scan output of the boundary scan chain path, from SHARC_D.
$\overline{\text{TRST}}$	I/A	**Test Reset (JTAG).** (Common to all SHARCs) Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) after power-up or held low for proper operation of the AD14060/AD14060L. $\overline{\text{TRST}}$ has a 20 kΩ internal pull-up resistor.
$\overline{\text{EMU}}$ (O/D)	O	**Emulation Status.** (Common to all SHARCs) Must be connected to the ADSP-2106x EZ-ICE target board connector *only*.
V_{DD}	P	**Power Supply.** Nominally +5.0 V dc for 5 V devices or +3.3 V dc for 3.3 V devices (26 pins).
GND	G	**Power Supply Return.** (28 pins).

EBOOT	LBOOT	$\overline{\text{BMS}}$	Booting Mode
1	0	Output	EPROM (Connect BMS to EPROM chip select)
0	0	1 (Input)	Host Processor
0	1	1 (Input)	Link Port
0	0	0 (Input)	No Booting. Processor executes from external memory.
0	1	0 (Input)	Reserved
1	1	x (Input)	Reserved

NOTES
FLAG3 is connected internally, common to SHARC_A, B, C, and D.
ID pins are hardwired internally as depicted in the block diagram.
[1]LINK PORTS 0, 2 and 5 are connected internally as described earlier in Link Port I/O.
[2]Three-statable only in EPROM boot mode (when $\overline{\text{BMS}}$ is an output).

TARGET BOARD CONNECTOR FOR EZ-ICE PROBE

The ADSP-2106x EZ-ICE Emulator uses the IEEE 1149.1 JTAG test access port of the ADSP-2106x to monitor and control the target board processor during emulation. The EZ-ICE probe requires that the AD14060/AD14060L's CLKIN (optional), TMS, TCK, $\overline{\text{TRST}}$, TDI, TDO, $\overline{\text{EMU}}$ and GND signals be made accessible on the target system via a 14-pin connector (a pin strip header) such as that shown in Figure 6. The EZ-ICE probe plugs directly onto this connector for chip-on-board emulation. You must add this connector to your target board design if you intend to use the ADSP-2106x EZ-ICE. The length of the traces between the connector and the AD14060/AD14060L's JTAG pins should be as short as possible.

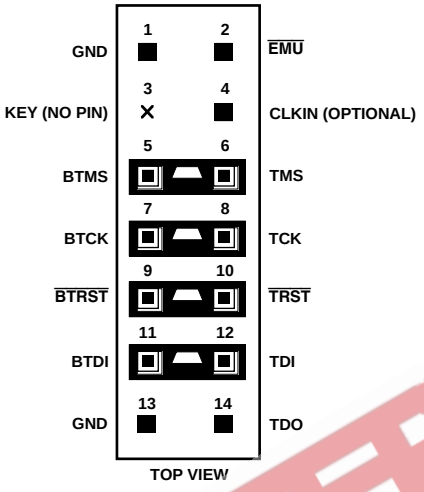


Figure 6. Target Board Connector for ADSP-2106x EZ-ICE Emulator (Jumpers in Place)

The 14-pin, 2-row pin strip header is keyed at the Pin 3 location; Pin 3 must be removed from the header. The pins must be 0.025 inch square and at least 0.20 inch in length. Pin spacing should be 0.1 × 0.1 inches. Pin strip headers are available from vendors such as 3M, McKenzie and Samtec.

The BTMS, BTCK, $\overline{\text{BTRST}}$ and BTDI signals are provided so that the test access port can also be used for board-level testing. When the connector is not being used for emulation, place jumpers between the Bxxx pins and the xxx pins as shown in Figure 6. If you are not going to use the test access port for board testing, tie $\overline{\text{BTRST}}$ to GND and tie or pull up BTCK to V_{DD}. The $\overline{\text{TRST}}$ pin must be asserted after power-up (through $\overline{\text{BTRST}}$ on the connector) or held low for proper operation of the AD14060/AD14060L. None of the Bxxx pins (Pins 5, 7, 9, 11) are connected on the EZ-ICE probe.

The JTAG signals are terminated on the EZ-ICE probe as follows:

Signal	Termination
TMS	Driven through 22 Ω Resistor (16 µA–3.2 µA Driver)
TCK	Driven at 10 MHz through 22 Ω Resistor (16 µA–3.2 µA Driver)
$\overline{\text{TRST}}$	Driven by Open-Drain Driver* (Pulled Up by On-Chip 20 kΩ resistor)
TDI	Driven by 16 µA–3.2 µA Driver
TDO	One TTL Load, No Termination
CLKIN	One TTL Load, No Termination (Optional Signal)
$\overline{\text{EMU}}$	4.7 kΩ Pull-Up Resistor, One TTL Load (Open-Drain Output from ADSP-2106x)

*$\overline{\text{TRST}}$ is driven low until the EZ-ICE probe is turned on by the EZ-ICE software (after the invocation command).

Figure 7 shows JTAG scan path connections for the multiprocessor system.

Connecting CLKIN to Pin 4 of the EZ-ICE header is optional. The emulator only uses CLKIN when directed to perform

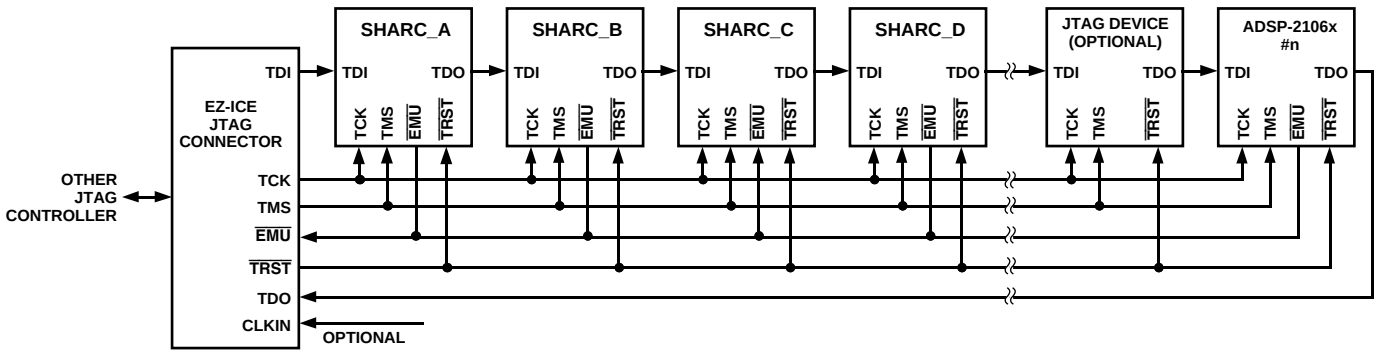


Figure 7. JTAG Scan Path Connections for the AD14060/AD14060L

operations such as starting, stopping and single-stepping multiple ADSP-2106xs in a synchronous manner. If you do not need these operations to occur synchronously on the multiple processors, simply tie Pin 4 of the EZ-ICE header to ground.

If synchronous multiprocessor operations are needed and CLKIN is connected, clock skew between the AD14060/AD14060L and the CLKIN pin on the EZ-ICE header must be minimal. If the skew is too large, synchronous operations may be off by one cycle between processors. For synchronous multiprocessor operation TCK, TMS, CLKIN and $\overline{\text{EMU}}$ should be treated as critical signals in terms of skew, and should be laid out as short as possible on your board. If TCK, TMS and CLKIN are driving a large number of ADSP-2106xs (more than eight) in your system, then treat them as a "clock tree" using multiple drivers to minimize skew. (See Figure 8 JTAG Clock Tree and Clock Distribution in the "High Frequency Design Considerations" section of the *ADSP-2106x User's Manual)*.

If synchronous multiprocessor operations are not needed (i.e., CLKIN is not connected), just use appropriate parallel termination on TCK and TMS. TDI, TDO, $\overline{\text{EMU}}$ and $\overline{\text{TRST}}$ are not critical signals in terms of skew.

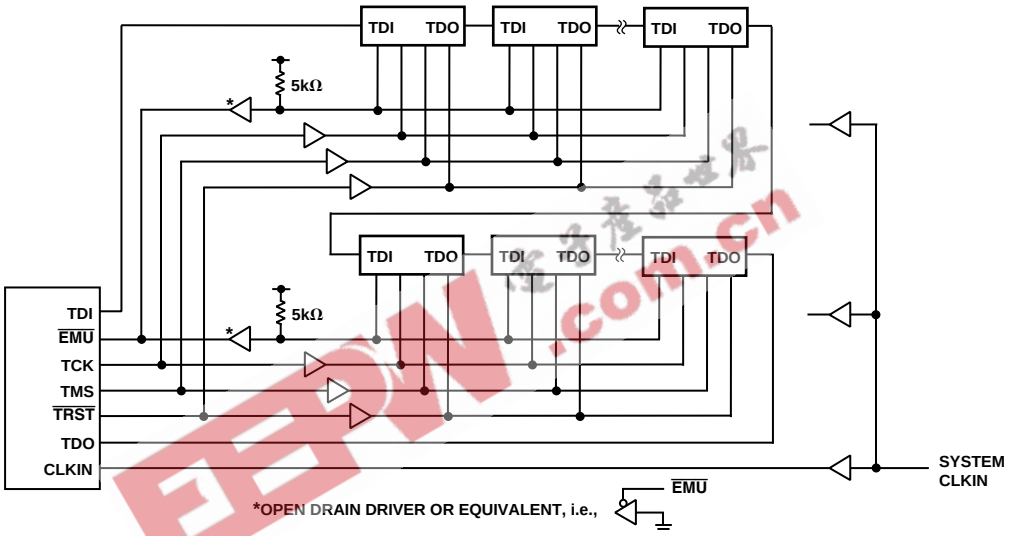


Figure 8. JTAG Clocktree for Multiple ADSP-2106x Systems

AD14060/AD14060L–SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Parameter		B Grade Min	B Grade Max	K Grade Min	K Grade Max	Units
V_{DD}	Supply Voltage (5 V)	4.75	5.25	4.75	5.25	V
	Supply Voltage (3.3 V)	3.15	3.6	3.15	3.6	V
T_{CASE}	Case Operating Temperature	–40	+100	0	+85	°C

ELECTRICAL CHARACTERISTICS (3.3 V, 5 V SUPPLY)

Parameter		Case Temp	Test Level	Test Condition	5 V Min	5 V Typ	5 V Max	3.3 V Min	3.3 V Typ	3.3 V Max	Units
V_{IH1}	High Level Input Voltage[1]	Full	I	@ V_{DD} = max	2.0		V_{DD} + 0.5	2.0		V_{DD} + 0.5	V
V_{IH2}	High Level Input Voltage[2]	Full	I	@ V_{DD} = max	2.2		V_{DD} + 0.5	2.2		V_{DD} + 0.5	V
V_{IL}	Low Level Input Voltage[1, 2]	Full	I	@ V_{DD} = min			0.8			0.8	V
V_{OH}	High Level Output Voltage[3, 4]	Full	I	@ V_{DD} = min, I_{OH} = –2.0 mA[4]	4.1			2.4			V
V_{OL}	Low Level Output Voltage[3, 4]	Full	I	@ V_{DD} = min, I_{OL} = 4.0 mA[4]			0.4			0.4	V
I_{IH}	High Level Input Current[5, 6, 7]	Full	I	@ V_{DD} = max, V_{IN} = V_{DD} max			10			10	µA
I_{IL}	Low Level Input Current[5]	Full	I	@ V_{DD} = max, V_{IN} = 0 V			10			10	µA
I_{ILP}	Low Level Input Current[6]	Full	I	@ V_{DD} = max, V_{IN} = 0 V			150			150	µA
I_{ILPX4}	Low Level Input Current[7]	Full	I	@ V_{DD} = max, V_{IN} = 0 V			600			600	µA
I_{OZH}	Three-State Leakage Current[8, 9, 10, 14]	Full	I	@ V_{DD} = max, V_{IN} = V_{DD} max			10			10	µA
I_{OZL}	Three-State Leakage Current[8, 11]	Full	I	@ V_{DD} = max, V_{IN} = 0 V			10			10	µA
I_{OZHP}	Three-State Leakage Current[11]	Full	I	@ V_{DD} = max, V_{IN} = V_{DD} max			350			350	µA
I_{OZLC}	Three-State Leakage Current[12]	Full	I	@ V_{DD} = max, V_{IN} = 0 V			1.5			1.5	mA
I_{OZLA}	Three-State Leakage Current[13]	Full	I	@ V_{DD} = max, V_{IN} = 1.5 V (5 V), 2 V (3.3 V)			350			350	µA
I_{OZLAR}	Three-State Leakage Current[10]	Full	I	@ V_{DD} = max, V_{IN} = 0 V			4.2			4.2	mA
I_{OZLS}	Three-State Leakage Current[9]	Full	I	@ V_{DD} = max, V_{IN} = 0 V			150			150	µA
I_{OZLSX4}	Three-State Leakage Current[14]	Full	I	@ V_{DD} = max, V_{IN} = 0 V			600			600	µA
I_{DDIN}	Supply Current (Internal)[15]	Full	IV	t_{CK} = 25 ns, V_{DD} = max		1.4	3.4		1.0	2.2	A
I_{DDIDLE}	Supply Current (Idle)[16]	Full	I	V_{DD} = max			800			760	mA
C_{IN}	Input Capacitance[17, 18]	+25°C	V			15			15		pF

EXPLANATION OF TEST LEVELS

Test Level

I 100% Production Tested[19].
II 100% Production Tested at +25°C, and Sample Tested at Specified Temperatures.
III Sample Tested Only.
IV Parameter is guaranteed by design and analysis, and characterization testing on discrete SHARCs.
V Parameter is typical value only.
VI All devices are 100% production tested at +25°C; sample tested at temperature extremes.

NOTES

[1] Applies to input and bidirectional pins: $DATA_{47-0}$, $ADDR_{31-0}$, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, ACK, $\overline{SBTS}$, $\overline{IRQy_{2-0}}$, FLAGy0, FLAG1, FLAGy2, $\overline{HBG}$, $\overline{CSy}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{BR_{6-1}}$, RPBA, $\overline{CPA}$y, TFS0, TFSy1, RFS0, RFSy1, $LyxDAT_{3-0}$, LyxCLK, LyxACK, EBOOTA, LBOOTA, EBOOTBCD, LBOOTBCD, $\overline{BMSA}$, $\overline{BMSBCD}$, TMS, TDI, TCK, $\overline{HBR}$, DR0, DRy1, TCLK0, TCLKy1, RCLK0, RCLKy1.
[2] Applies to input pins: CLKIN, $\overline{RESET}$, $\overline{TRST}$.
[3] Applies to output and bidirectional pins: $DATA_{47-0}$, $ADDR_{31-0}$, $\overline{MS_{3-0}}$ $\overline{RD}$, $\overline{WR}$, PAGE, ADRCLK, $\overline{SW}$, ACK, FLAGy0, FLAG1, FLAGy2, TIMEXPy, $\overline{HBG}$, $\overline{REDY}$, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BR_{6-1}}$, $\overline{CPA}$y, DTO, DTy1, TCLK0, TCLKy1, RCLK0, RCLKy1, TFS0, TFSy1, RFS0, RFSy1 $LyxDAT_{3-0}$, LyxCLK, LyxACK, $\overline{BMSA}$, $\overline{BMSBCD}$, TDO, $\overline{EMU}$.
[4] See Output Drive Currents for typical drive current capabilities.
[5] Applies to input pins: $\overline{SBTS}$, $\overline{IRQy_{2-0}}$, $\overline{HBR}$, $\overline{CSy}$, $\overline{DMAR1}$, $\overline{DMAR2}$, RPBA, EBOOTA, LBOOTA, EBOOTBCD, LBOOTBCD, CLKIN, $\overline{RESET}$, TCK.
[6] Applies to input pins with internal pull-ups: DR0, DRy1, TDI.
[7] Applies to bussed input pins with internal pull-ups: $\overline{TRST}$, TMS.
[8] Applies to three-statable pins: $DATA_{47-0}$, $ADDR_{31-0}$, $\overline{MS_{3-0}}$, $\overline{RD}$, $\overline{WR}$, PAGE, ADRCLK, $\overline{SW}$, ACK, FLAGy0, FLAG1, FLAGy2, REDY, $\overline{HBG}$, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BMSA}$, $\overline{BMSBCD}$, TDO, $\overline{EMU}$. (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when ID_{2-0} = 001 and another ADSP-2106x is not requesting bus mastership. $\overline{HBG}$ AND $\overline{EMU}$ are not tested for leakage current.)
[9] Applies to three-statable pins with internal pull-ups: DTy1, TCLKy1, RCLKy1.
[10] Applies to ACK pin when pulled up. (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when ID_{2-0} = 001 and another ADSP-2106x is not requesting bus mastership.)
[11] Applies to three-statable pins with internal pull-downs: $LyxDAT_{3-0}$, LyxCLK, LyxACK.
[12] Applies to $\overline{CPA}$y pin.
[13] Applies to ACK pin when keeper latch enabled.
[14] Applies to bused three-statable pins with internal pull-ups: DT0, TCLK0, RCLK0.
[15] Applies to V_{DD} pins. Conditions of operation: each processor executing radix-2 FFT butterfly with instruction in cache, one data operand fetched from each internal memory block, and one DMA transfer occurring from/to internal memory at t_{CK} = 25 ns.
[16] Applies to V_{DD} pins. Idle denotes AD14060/AD14060L state during execution of IDLE instruction.
[17] Applies to all signal pins.
[18] Guaranteed but not tested.
[19] Link and Serial Ports: All are 100% tested at die level prior to assembly. All are 100% ac tested at module level; Link-4 and Serial-0 are also dc tested at the module level. See Timing Specifications.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage (5 V) . . . . . –0.3 V to +7 V
Supply Voltage (3.3 V) . . . . . –0.3 V to +4.6 V
Input Voltage . . . . . –0.5 V to V_{DD} + 0.5 V
Output Voltage Swing . . . . . –0.5 V to V_{DD} + 0.5 V
Load Capacitance . . . . . 200 pF
Junction Temperature Under Bias . . . . . 130°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (5 seconds) . . . . . +280°C

*Stresses greater than those listed above may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD SENSITIVITY

The AD14060/AD14060L modules are ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur to devices subjected to high energy electrostatic discharges.

The ADSP-21060 processors include proprietary ESD protection circuitry to dissipate high energy discharges. Per method 3015 of MIL-STD-883, the ADSP-21060 processors have been classified as a Class 2 device.

Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Unused devices must be stored in conductive foam or shunts, and the foam should be discharged to the destination socket before devices are removed.

TIMING SPECIFICATIONS

GENERAL NOTES

This data sheet represents production released specifications for the AD14060 (5 V), and for the AD14060L (3.3 V). The ADSP-21060 die components are 100% tested, and the assembled AD14060/AD14060L units are again extensively tested at-speed, and across-temperature. Parametric limits were established from the ADSP-21060 characterization followed by further design/analysis of the AD14060/AD14060L package characteristics. The specifications shown are based on a CLKIN frequency of 40 MHz (t_{CK} = 25 ns). The DT derating allows specifications at other CLKIN frequencies (within the min-max range of the t_{CK} specification; see "Clock Input" below). DT is the difference between the actual CLKIN period and a CLKIN period of 25 ns:

$$DT = t_{CK} - 25\ ns$$

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, you cannot meaningfully add parameters to derive longer times.

Switching Characteristics specify how the processor changes its signals. You have no control over this timing—circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics tell you what the processor will do in a given circumstance. You can also use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing Requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

(O/D) = Open Drain
(A/D) = Active Drain

Parameter		40 MHz–5 V Min	40 MHz–5 V Max	40 MHz–3.3 V Min	40 MHz–3.3 V Max	Units
Clock Input						
Timing Requirements:						
t_{CK}	CLKIN Period	25	100	25	100	ns
t_{CKL}	CLKIN Width Low	7		8.75		ns
t_{CKH}	CLKIN Width High	5		5		ns
t_{CKRF}	CLKIN Rise/Fall (0.4 V–2.0 V)		3		3	ns

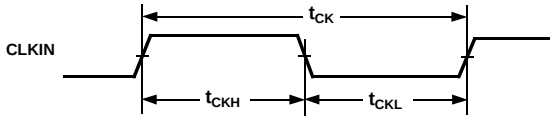


Figure 9. Clock Input

Parameter		5 V Min	5 V Max	3.3 V Min	3.3 V Max	Units
Reset						
Timing Requirements:						
t_{WRST}	$\overline{\text{RESET}}$ Pulsewidth Low[1]	$4t_{CK}$		$4t_{CK}$		ns
t_{SRST}	$\overline{\text{RESET}}$ Setup Before CLKIN High[2]	14 + DT/2	t_{CK}	14 + DT/2	t_{CK}	ns

NOTES
[1]Applies after the power-up sequence is complete. At power-up, the processor's internal phase-locked loop requires no more than 2000 CLKIN cycles while $\overline{\text{RESET}}$ is low, assuming stable V_{DD} and CLKIN (not including start-up time of external clock oscillator).
[2]Only required if multiple ADSP-2106xs must come out of reset synchronous to CLKIN with program counters (PC) equal (i.e., for a SIMD system). Not required for multiple ADSP-2106xs communicating over the shared bus (through the external port), because the bus arbitration logic automatically synchronizes itself after reset.

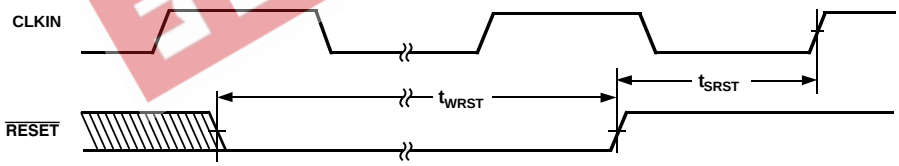


Figure 10. Reset

Parameter		5 V Min	5 V Max	3.3 V Min	3.3 V Max	Units
Interrupts						
Timing Requirements:						
t_{SIR}	$\overline{\text{IRQ2-0}}$ Setup Before CLKIN High[1]	18 + 3DT/4		18 + 3DT/4		ns
t_{HIR}	$\overline{\text{IRQ2-0}}$ Hold Before CLKIN High[1]		11.5 + 3DT/4		11.5 + 3DT/4	ns
t_{IPW}	$\overline{\text{IRQ2-0}}$ Pulsewidth[2]	2 + t_{CK}		2 + t_{CK}		ns

NOTES
[1]Only required for $\overline{\text{IRQx}}$ recognition in the following cycle.
[2]Applies only if t_{SIR} and t_{HIR} requirements are not met.

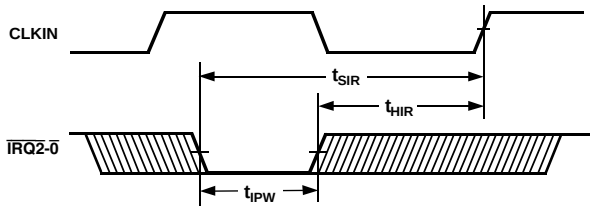


Figure 11. Interrupts

Parameter		5 V Min	5 V Max	3.3 V Min	3.3 V Max	Units
Timer						
Switching Characteristic:						
t_{DTEX}	CLKIN High to TIMEXP		16		16	ns

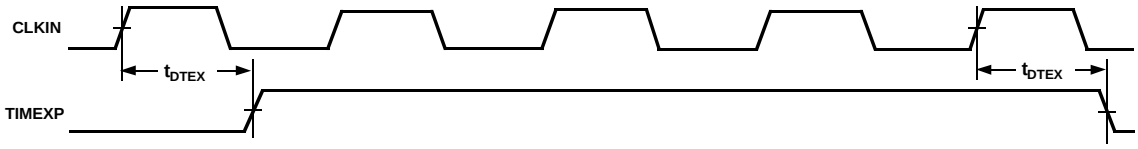


Figure 12. Timer

Parameter		5 V Min	5 V Max	3.3 V Min	3.3 V Max	Units
Flags						
Timing Requirements:						
t_{SFI}	FLAG2-0$_{IN}$ Setup Before CLKIN High[1]	8 + 5DT/16		8 + 5DT/16		ns
t_{HFI}	FLAG2-0$_{IN}$ Hold After CLKIN High[1]	0.5 – 5DT/16		0.5 – 5DT/16		ns
t_{DWRFI}	FLAG2-0$_{IN}$ Delay After $\overline{RD}$/$\overline{WR}$ Low[1]		4.5 + 7DT/16		4.5 + 7DT/16	ns
t_{HFIWR}	FLAG2-0$_{IN}$ Hold After $\overline{RD}$/$\overline{WR}$ Deasserted[1]	0.5		0.5		ns
Switching Characteristics:						
t_{DFO}	FLAG2-0$_{OUT}$ Delay After CLKIN High		17		17	ns
t_{HFO}	FLAG2-0$_{OUT}$ Hold After CLKIN High	4		4		ns
t_{DFOE}	CLKIN High to FLAG2-0$_{OUT}$ Enable	3		3		ns
t_{DFOD}	CLKIN High to FLAG2-0$_{OUT}$ Disable		15		15	ns

NOTE
[1]Flag inputs meeting these setup and hold times will affect conditional instructions in the following instruction cycle.

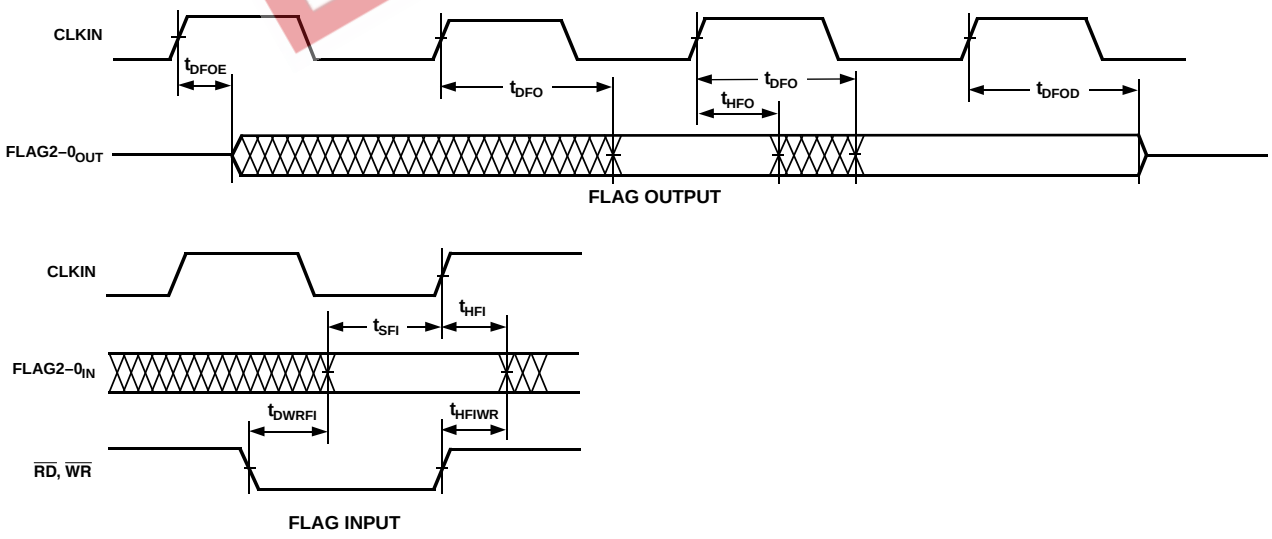


Figure 13. Flags

Memory Read—Bus Master

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) without reference to CLKIN. These specifications apply when the AD14060/AD14060L is the bus master accessing external memory space.

These switching characteristics also apply for bus master synchronous read/write timing (see Synchronous Read/Write – Bus Master below). If these timing requirements are met, the synchronous read/write timing can be ignored (and vice versa).

Parameter		5 V Min	5 V Max	3.3 V Min	3.3 V Max	Units
Timing Requirements:						
t_{DAD}	Address, Delay to Data Valid[1, 4]		17.5 + DT + W		17.5 + DT + W	ns
t_{DRLD}	$\overline{RD}$ Low to Data Valid[1]		11.5 + 5DT/8 + W		11.5 + 5DT/8 + W	ns
t_{HDA}	Data Hold from Address[2]	1		1		ns
t_{HDRH}	Data Hold from $\overline{RD}$ High[2]	2.5		2.5		ns
t_{DAAK}	ACK Delay from Address[3, 4]		13.5 + 7DT/8 + W		13.5 + 7DT/8 + W	ns
t_{DSAK}	ACK Delay from $\overline{RD}$ Low[3]		7.5 + DT/2 + W		7.5 + DT/2 + W	ns
Switching Characteristics:						
t_{DRHA}	Address Hold After $\overline{RD}$ High	–0.5 + H		–0.5 + H		ns
t_{DARL}	Address to $\overline{RD}$ Low[4]	1.5 + 3DT/8		1.5 + 3DT/8		ns
t_{RW}	$\overline{RD}$ Pulsewidth	12.5 + 5DT/8 + W		12.5 + 5DT/8 + W		ns
t_{RWR}	$\overline{RD}$ High to $\overline{WR}$, $\overline{RD}$, $\overline{DMAGx}$ Low	8 + 3DT/8 + HI		8 + 3DT/8 + HI		ns
t_{SADADC}	Address Setup Before ADRCLK High[4]	–0.5 + DT/4		–0.5 + DT/4		ns

W = (number of wait states specified in WAIT register) × t_{CK}.
HI = t_{CK} (if an address hold cycle or bus idle cycle occurs, as specified in WAIT register; otherwise HI = 0).
H = t_{CK} (if an address hold cycle occurs as specified in WAIT register; otherwise H = 0).

NOTES
[1]Data Delay/Setup: User must meet t_{DAD} or t_{DRLD} or synchronous spec t_{SSDATI}.
[2]Data Hold: User must meet t_{HDA} or t_{HDRH} or synchronous spec t_{HDATI}. See System Hold Time Calculation under Test Conditions for the calculation of hold times given capacitive and dc loads.
[3]ACK Delay/Setup: User must meet t_{DSAK} or t_{DAAK} or synchronous specification t_{SACKC}.
[4]For $\overline{MS}$x, $\overline{SW}$, $\overline{BMS}$, the falling edge is referenced.

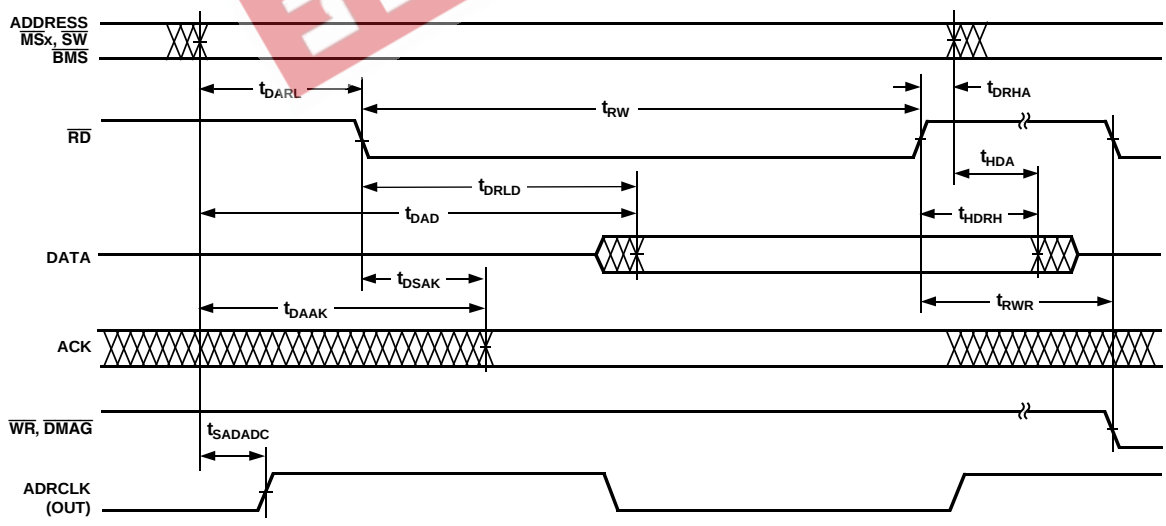


Figure 14. Memory Read—Bus Master

Memory Write—Bus Master

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) without reference to CLKIN. These specifications apply when the AD14060/AD14060L is the bus master accessing external memory space.

These switching characteristics also apply for bus master synchronous read/write timing (see Synchronous Read/Write–Bus Master). If these timing requirements are met, the synchronous read/write timing can be ignored (and vice versa).

Parameter		5 V Min	5 V Max	3.3 V Min	3.3 V Max	Units
Timing Requirements:						
t_{DAAK}	ACK Delay from Address, Selects[1, 2]		13.5 + 7DT/8 + W		13.5 + 7DT/8 + W	ns
t_{DSAK}	ACK Delay from $\overline{WR}$ Low[1]		7.5 + DT/2 + W		7.5 + DT/2 + W	ns
Switching Characteristics:						
t_{DAWH}	Address, Selects to $\overline{WR}$ Deasserted[2]	16.5 + 15DT/16 + W		16.5 + 15DT/16 + W		ns
t_{DAWL}	Address, Selects to $\overline{WR}$ Low[2]	2.5 + 3DT/8		2.5 + 3DT/8		ns
t_{WW}	$\overline{WR}$ Pulsewidth	12 + 9DT/16 + W		12 + 9DT/16 + W		ns
t_{DDWH}	Data Setup before $\overline{WR}$ High	6.5 + DT/2 + W		6.5 + DT/2 + W		ns
t_{DWHA}	Address Hold after $\overline{WR}$ Deasserted	–1 + DT/16 + H		–1 + DT/16 + H		ns
t_{DATRWH}	Data Disable after $\overline{WR}$ Deasserted[3]	0.5 + DT/16 + H	6.5 + DT/16 + H	0.5 + DT/16 + H	6.5 + DT/16 + H	ns
t_{WWR}	$\overline{WR}$ High to $\overline{WR}$, $\overline{RD}$, $\overline{DMAGx}$ Low	7.5 + 7DT/16 + H		7.5 + 7DT/16 + H		ns
t_{DDWR}	Data Disable before $\overline{WR}$ or $\overline{RD}$ Low	4.5 + 3DT/8 + I		4.5 + 3DT/8 + I		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	–1.5 + DT/16		–1.5 + DT/16		ns
t_{SADADC}	Address, Selects to ADRCLK High[2]	–0.5 + DT/4		–0.5 + DT/4		ns

W = (number of wait states specified in WAIT register) × t_{CK}.
H = t_{CK} (if an address hold cycle occurs, as specified in WAIT register; otherwise H = 0).
I = t_{CK} (if a bus idle cycle occurs, as specified in WAIT register; otherwise I = 0).

NOTES

[1]ACK Delay/Setup: User must meet t_{DAAK} or t_{DSAK} or synchronous specification t_{SACKC}.

[2]For MSx, SW, BMS, the falling edge is referenced.

[3]See System Hold Time Calculation under Test Conditions for calculation of hold times given capacitive and dc loads.

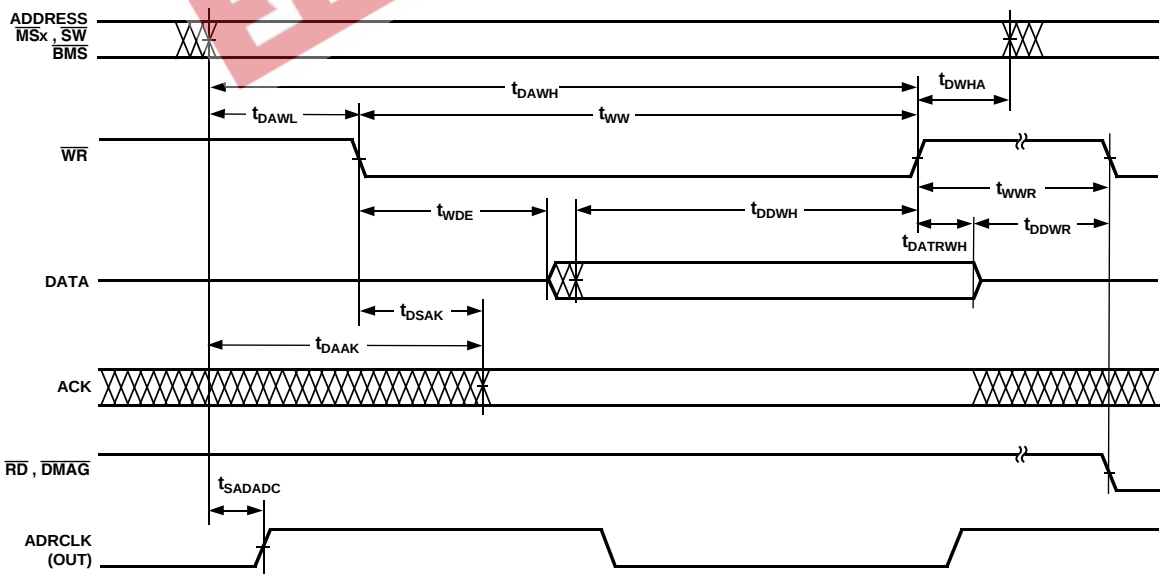


Figure 15. Memory Write—Bus Master

Synchronous Read/Write—Bus Master

Use these specifications for interfacing to external memory systems that require CLKIN—relative timing or for accessing a slave ADSP-2106x (in multiprocessor memory space). These synchronous switching characteristics are also valid during asynchronous memory reads and writes (see Memory Read—Bus Master and Memory Write—Bus Master).

When accessing a slave ADSP-2106x, these switching characteristics must meet the slave's timing requirements for synchronous read/writes (see Synchronous Read/Write—Bus Slave). The slave ADSP-2106x must also meet these (bus master) timing requirements for data and acknowledge setup and hold times.

Parameter		5 V Min	5 V Max	3.3 V Min	3.3 V Max	Units
Timing Requirements:						
t_{SSDATI}	Data Setup Before CLKIN	3 + DT/8		3 + DT/8		ns
t_{HSDATI}	Data Hold After CLKIN	4 – DT/8		4 – DT/8		ns
t_{DAAK}	ACK Delay After Address, $\overline{MS}$x, $\overline{SW}$, $\overline{BMS}$[1, 2]		13.5 + 7 DT/8 + W		13.5 + 7 DT/8 + W	ns
t_{SACKC}	ACK Setup Before CLKIN[2]	6.5 + DT/4		6.5 + DT/4		ns
t_{HACKC}	ACK Hold After CLKIN	–0.5 – DT/4		–0.5 – DT/4		ns
Switching Characteristics:						
t_{DADRO}	Address, $\overline{MS}$x, $\overline{BMS}$, $\overline{SW}$ Delay After CLKIN[1]		8 – DT/8		8 – DT/8	ns
t_{HADRO}	Address, $\overline{MS}$x, $\overline{BMS}$, $\overline{SW}$ Hold After CLKIN	–1 – DT/8		–1 – DT/8		ns
t_{DPGC}	PAGE Delay After CLKIN	9 + DT/8	17 + DT/8	9 + DT/8	17 + DT/8	ns
t_{DRDO}	$\overline{RD}$ High Delay After CLKIN	–2 – DT/8	5 – DT/8	–2 – DT/8	5 – DT/8	ns
t_{DWRO}	$\overline{WR}$ High Delay After CLKIN	–3 – 3DT/16	5 – 3DT/16	–3 – 3DT/16	5 – 3DT/16	ns
t_{DRWL}	$\overline{RD}$/$\overline{WR}$ Low Delay After CLKIN	8 + DT/4	13.5 + DT/4	8 + DT/4	13.5 + DT/4	ns
t_{SDDATO}	Data Delay After CLKIN		20 + 5DT/16		20 + 5DT/16	ns
t_{DATTR}	Data Disable After CLKIN[3]	0 – DT/8	8 – DT/8	0 – DT/8	8 – DT/8	ns
t_{DADCCK}	ADRCLK Delay After CLKIN	4 + DT/8	11 + DT/8	4 + DT/8	11 + DT/8	ns
t_{ADRCK}	ADRCLK Period	t_{CK}		t_{CK}		ns
t_{ADRCKH}	ADRCLK Width High	(t_{CK}/2 – 2)		(t_{CK}/2 – 2)		ns
t_{ADRCKL}	ADRCLK Width Low	(t_{CK}/2 – 2)		(t_{CK}/2 – 2)		ns

W = (number of Wait states specified in WAIT register) × t_{CK}.

NOTES

[1]For $\overline{MS}$x, $\overline{SW}$, $\overline{BMS}$, the falling edge is referenced.

[2]ACK Delay/Setup: User must meet t_{DAAK} or t_{DSAK} or synchronous specification t_{SACKC}.

[3]See System Hold Time Calculation under Test Conditions for calculation of hold times given capacitive and dc loads.

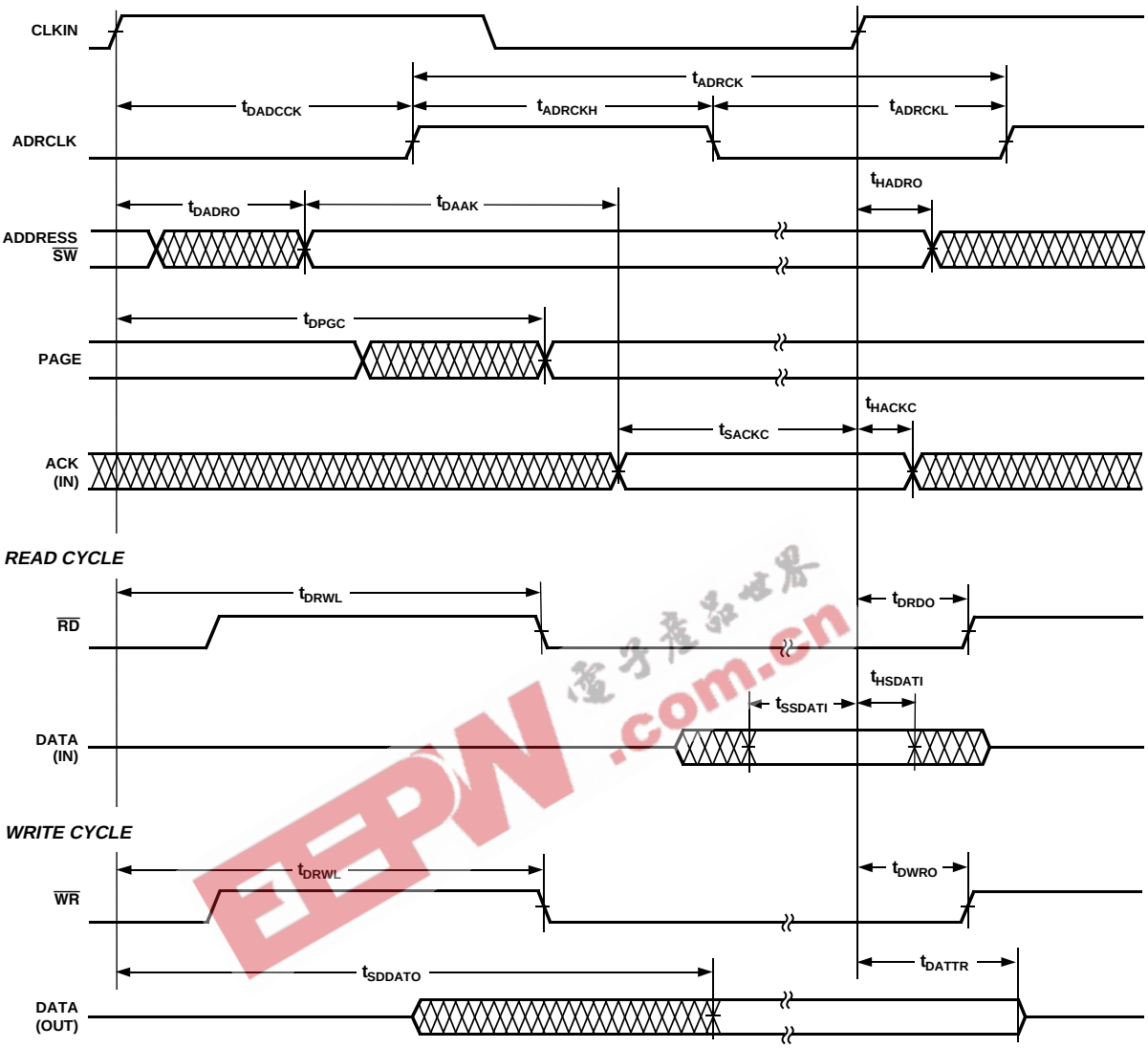


Figure 16. Synchronous Read/Write—Bus Master

Synchronous Read/Write—Bus Slave

Use these specifications for bus master accesses of a slave's IOP registers or internal memory (in multiprocessor memory space). The bus master must meet these (bus slave) timing requirements.

Parameter		5 V Min	5 V Max	3.3 V Min	3.3 V Max	Units
Timing Requirements:						
t_{SADRI}	Address, $\overline{SW}$ Setup Before CLKIN	15.5 + DT/2		15.5 + DT/2		ns
t_{HADRI}	Address, $\overline{SW}$ Hold Before CLKIN		4.5 + DT/2		4.5 + DT/2	ns
t_{SRWLI}	$\overline{RD}/\overline{WR}$ Low Setup Before CLKIN[1]	9.5 + 5DT/16		9.5 + 5DT/16		ns
t_{HRWLI}	$\overline{RD}/\overline{WR}$ Low Hold After CLKIN	–3.5 – 5DT/16	8 + 7DT/16	–3.5 – 5DT/16	8 + 7DT/16	ns
t_{RWHPI}	$\overline{RD}/\overline{WR}$ Pulse High	3		3		ns
t_{SDATWH}	Data Setup Before $\overline{WR}$ High	5.5		5.5		ns
t_{HDATWH}	Data Hold After $\overline{WR}$ High	1.5		1.5		ns
Switching Characteristics:						
t_{SDDATO}	Data Delay After CLKIN		20 + 5DT/16		20 + 5DT/16	ns
t_{DATTR}	Data Disable After CLKIN[2]	0 – DT/8	8 – DT/8	0 – DT/8	8 – DT/8	ns
t_{DACKAD}	ACK Delay After Address, $\overline{SW}$[3]		10		10	ns
t_{ACKTR}	ACK Disable After CLKIN[3]	–1 – DT/8	7 – DT/8	–1 – DT/8	7 – DT/8	ns

NOTES

[1]t_{SRWLI} (min) = 9.5 + 5DT/16 when Multiprocessor Memory Space Wait State (MMSWS bit in WAIT register) is disabled; when MMSWS is enabled, t_{SRWLI} (min) = 4 + DT/8.

[2]See System Hold Time Calculation under Test Conditions for calculation of hold times given capacitive and dc loads.

[3]t_{DACKAD} is true only if the address and $\overline{SW}$ inputs have setup times (before CLKIN) greater than 10.5 + DT/8 and less than 18.5 + 3DT/4. If the address and $\overline{SW}$ inputs have setup times greater than 19 + 3DT/4, then ACK is valid 15 + DT/4 (max) after CLKIN. A slave that sees an address with an M field match will respond with ACK regardless of the state of MMSWS or strobes. A slave will three-state ACK every cycle with t_{ACKTR}.

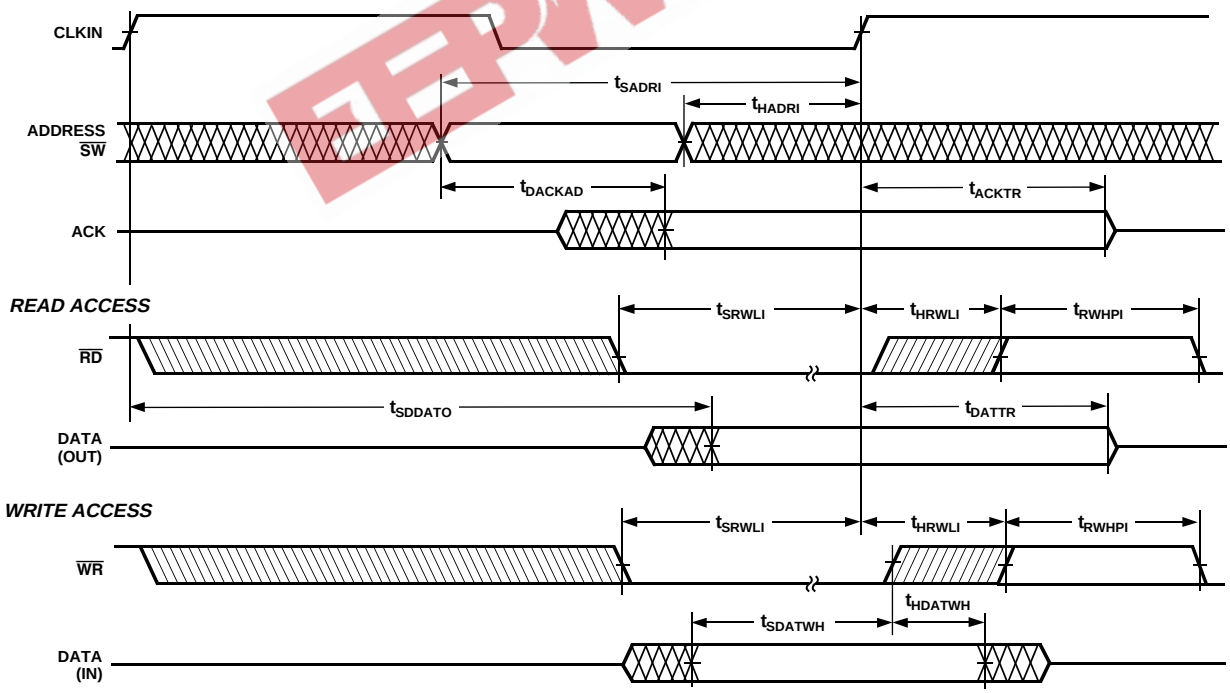
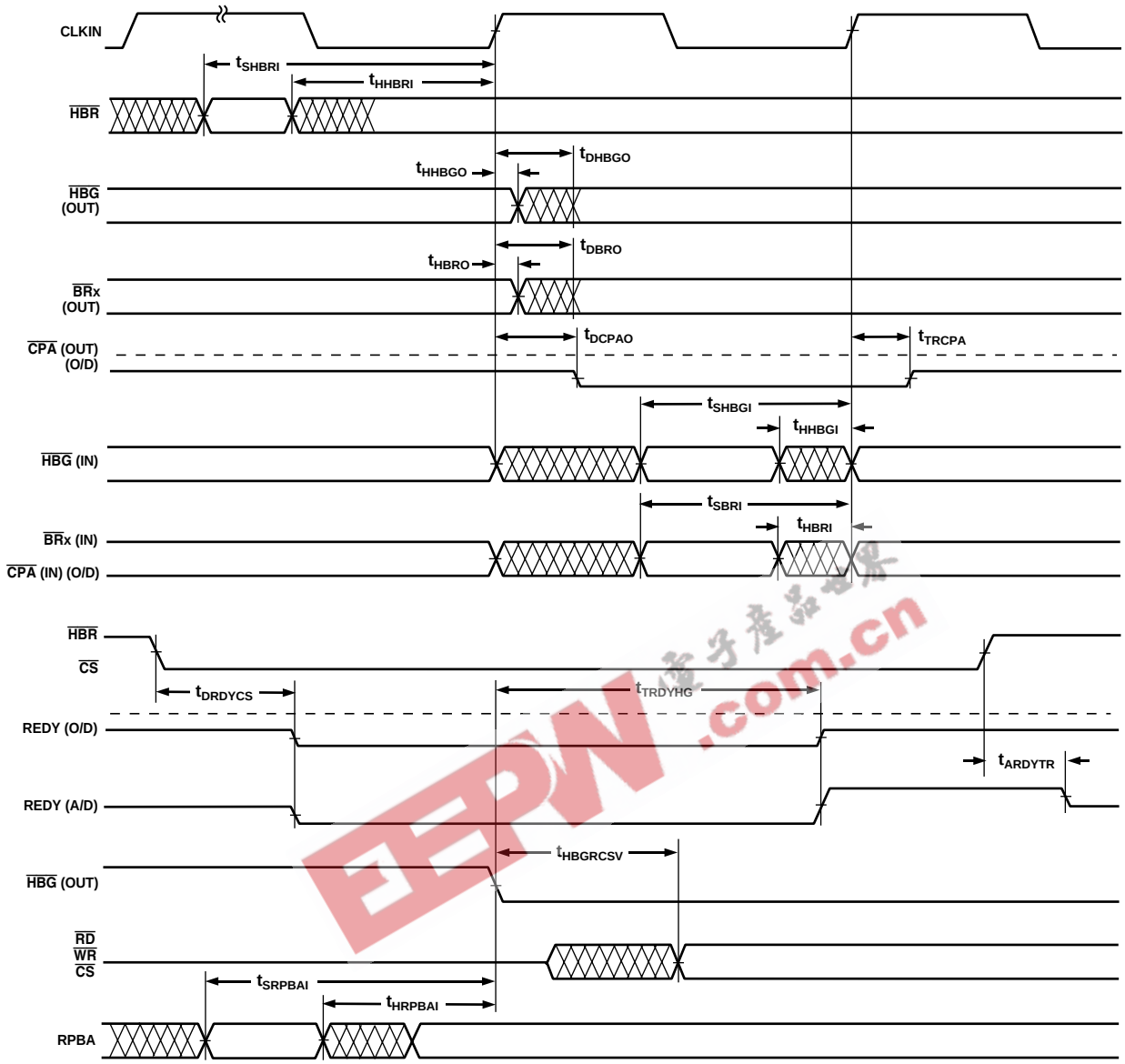


Figure 17. Synchronous Read/Write—Bus Slave

Multiprocessor Bus Request and Host Bus Request
Use these specifications for passing of bus mastership between multiprocessing ADSP-2106x's ($\overline{BR}$x) or a host processor ($\overline{HBR}$, $\overline{HBG}$).

Parameter		5 V Min	5 V Max	3.3 V Min	3.3 V Max	Units
Timing Requirements:						
$t_{HBGRCSV}$	$\overline{HBG}$ Low to $\overline{RD}$/$\overline{WR}$/$\overline{CS}$ Valid[1]		19.5 + 5DT/4		19.5 + 5DT/4	ns
t_{SHBRI}	$\overline{HBR}$ Setup Before CLKIN[2]	20 + 3DT/4		20 + 3DT/4		ns
t_{HHBRI}	$\overline{HBR}$ Hold Before CLKIN[2]		13.5 + 3DT/4		13.5 + 3DT/4	ns
t_{SHBGI}	$\overline{HBG}$ Setup Before CLKIN	13 + DT/2		13 + DT/2		ns
t_{HHBGI}	$\overline{HBG}$ Hold Before CLKIN High		5.5 + DT/2		5.5 + DT/2	ns
t_{SBRI}	$\overline{BR}$x, $\overline{CPA}$ Setup Before CLKIN[3]	13 + DT/2		13 + DT/2		ns
t_{HBRI}	$\overline{BR}$x, $\overline{CPA}$ Hold Before CLKIN High		5.5 + DT/2		5.5 + DT/2	ns
t_{SRPBAI}	RPBA Setup Before CLKIN	20 + 3DT/4		20 + 3DT/4		ns
t_{HRPBAI}	RPBA Hold Before CLKIN		11.5 + 3DT/4		11.5 + 3DT/4	ns
Switching Characteristics:						
t_{DHBGO}	$\overline{HBG}$ Delay After CLKIN		8 – DT/8		8 – DT/8	ns
t_{HHBGO}	$\overline{HBG}$ Hold After CLKIN	–2 – DT/8		–2 – DT/8		ns
t_{DBRO}	$\overline{BR}$x Delay After CLKIN		8 – DT/8		8 – DT/8	ns
t_{HBRO}	$\overline{BR}$x Hold After CLKIN	–2 – DT/8		–2 – DT/8		ns
t_{DCPAO}	$\overline{CPA}$ Low Delay After CLKIN		9 – DT/8		9 – DT/8	ns
t_{TRCPA}	$\overline{CPA}$ Disable After CLKIN	–2 – DT/8	5.5 – DT/8	–2 – DT/8	5.5 – DT/8	ns
t_{DRDYCS}	REDY (O/D) or (A/D) Low from $\overline{CS}$ and $\overline{HBR}$ Low[4]		9.5		10.25	ns
t_{TRDYHG}	REDY (O/D) Disable or REDY (A/D) High from $\overline{HBG}$[4]	44 + 27DT/16		44 + 27DT/16		ns
t_{ARDYTR}	REDY (A/D) Disable from $\overline{CS}$ or $\overline{HBR}$ High[4]		11		11	ns

NOTES
[1]For first asynchronous access after $\overline{HBR}$ and $\overline{CS}$ asserted, $ADDR_{31-0}$ must be a non-MMS value 1/2 t_{CK} before $\overline{RD}$ or $\overline{WR}$ goes low or by $t_{HBGRCSV}$ after HBG goes low. This is easily accomplished by driving an upper address signal high when $\overline{HBG}$ is asserted.
[2]Only required for recognition in the current cycle.
[3]$\overline{CPA}$ assertion must meet the setup to CLKIN; deassertion does not need to meet the setup to CLKIN.
[4](O/D) = open drain, (A/D) = active drive.



O/D = OPEN DRAIN, A/D = ACTIVE DRIVE
HBG WILL BE DELAYED BY n CLOCK CYCLES WHEN WAIT STATES OR BUS LOCK ARE IN EFFECT.

Figure 18. Multiprocessor Bus Request and Host Bus Request

Asynchronous Read/Write—Host to AD14060/AD14060L
Use these specifications for asynchronous host processor accesses of an AD14060/AD14060L, after the host has asserted $\overline{CS}$ and $\overline{HBR}$ (low). After $\overline{HBG}$ is returned by the AD14060/AD14060L, the host can drive the $\overline{RD}$ and $\overline{WR}$ pins to access the AD14060/AD14060L's internal memory or IOP registers. $\overline{HBR}$ and $\overline{HBG}$ are assumed low for this timing.

Parameter		5 V Min	5 V Max	3.3 V Min	3.3 V Max	Units
Read Cycle						
Timing Requirements:						
t_{SADRDL}	Address Setup/$\overline{CS}$ Low Before $\overline{RD}$ Low[1]	0.5		0.5		ns
t_{HADRDH}	Address Hold/$\overline{CS}$ Hold Low After $\overline{RD}$	0.5		0.5		ns
t_{WRWH}	$\overline{RD}$/$\overline{WR}$ High Width	6		6		ns
$t_{DRDHRDY}$	$\overline{RD}$ High Delay After REDY (O/D) Disable	0.5		0.5		ns
$t_{DRDHRDY}$	$\overline{RD}$ High Delay After REDY (A/D) Disable	0.5		0.5		ns
Switching Characteristics:						
$t_{SDATRDY}$	Data Valid Before REDY Disable from Low	1.5		1.5		ns
$t_{DRDYRDL}$	REDY (O/D) or (A/D) Low Delay After $\overline{RD}$ Low		11		11.5	ns
t_{RDYPRD}	REDY (O/D) or (A/D) Low Pulsewidth for Read	45 + DT		45 + DT		ns
t_{HDARWH}	Data Disable After $\overline{RD}$ High	1.5	9	1.5	9.5	ns
Write Cycle						
Timing Requirements:						
t_{SCSWRL}	$\overline{CS}$ Low Setup Before $\overline{WR}$ Low	0.5		0.5		ns
t_{HCSWRH}	$\overline{CS}$ Low Hold After $\overline{WR}$ High	0.5		0.5		ns
t_{SADWRH}	Address Setup Before $\overline{WR}$ High	5.5		5.5		ns
t_{HADWRH}	Address Hold After $\overline{WR}$ High	2.5		2.5		ns
t_{WWRL}	$\overline{WR}$ Low Width	7		7		ns
t_{WRWH}	$\overline{RD}$/$\overline{WR}$ High Width	6		6		ns
$t_{DWRHRDY}$	$\overline{WR}$ High Delay After REDY (O/D) or (A/D) Disable	0.5		0.5		ns
t_{SDATWH}	Data Setup Before $\overline{WR}$ High	5.5		5.5		ns
t_{HDATWH}	Data Hold After $\overline{WR}$ High	1.5		1.5		ns
Switching Characteristics:						
$t_{DRDYWRL}$	REDY (O/D) or (A/D) Low Delay After $\overline{WR}$/$\overline{CS}$ Low		11		11.5	ns
t_{RDYPWR}	REDY (O/D) or (A/D) Low Pulsewidth for Write	15		15		ns
t_{SRDYCK}	REDY (O/D) or (A/D) Disable to CLKIN	1 + 7DT/16	9 + 7DT/16	0 + 7DT/16	8 + 7DT/16	ns

NOTE
[1]Not required if $\overline{RD}$ and address are valid $t_{HBGRCSV}$ after $\overline{HBG}$ goes low. For first access after $\overline{HBR}$ asserted, $ADDR_{31-0}$ must be a non-MMS value 1/2 t_{CLK} before $\overline{RD}$ or $\overline{WR}$ goes low or by $t_{HBGRCSV}$ after $\overline{HBG}$ goes low. This is easily accomplished by driving an upper address signal high when $\overline{HBG}$ is asserted. For address bits to be driven during asynchronous host accesses, see Table 8.2 of the *ADSP-2106x SHARC User's Manual*.

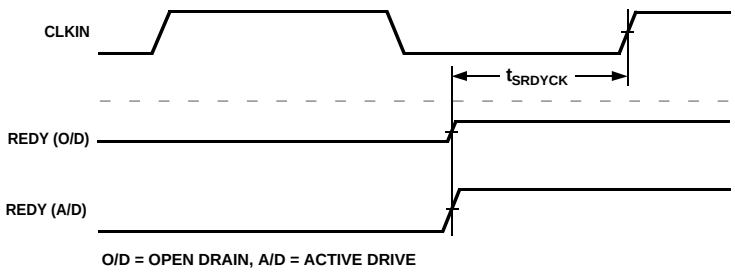


Figure 19a. Synchronous REDY Timing

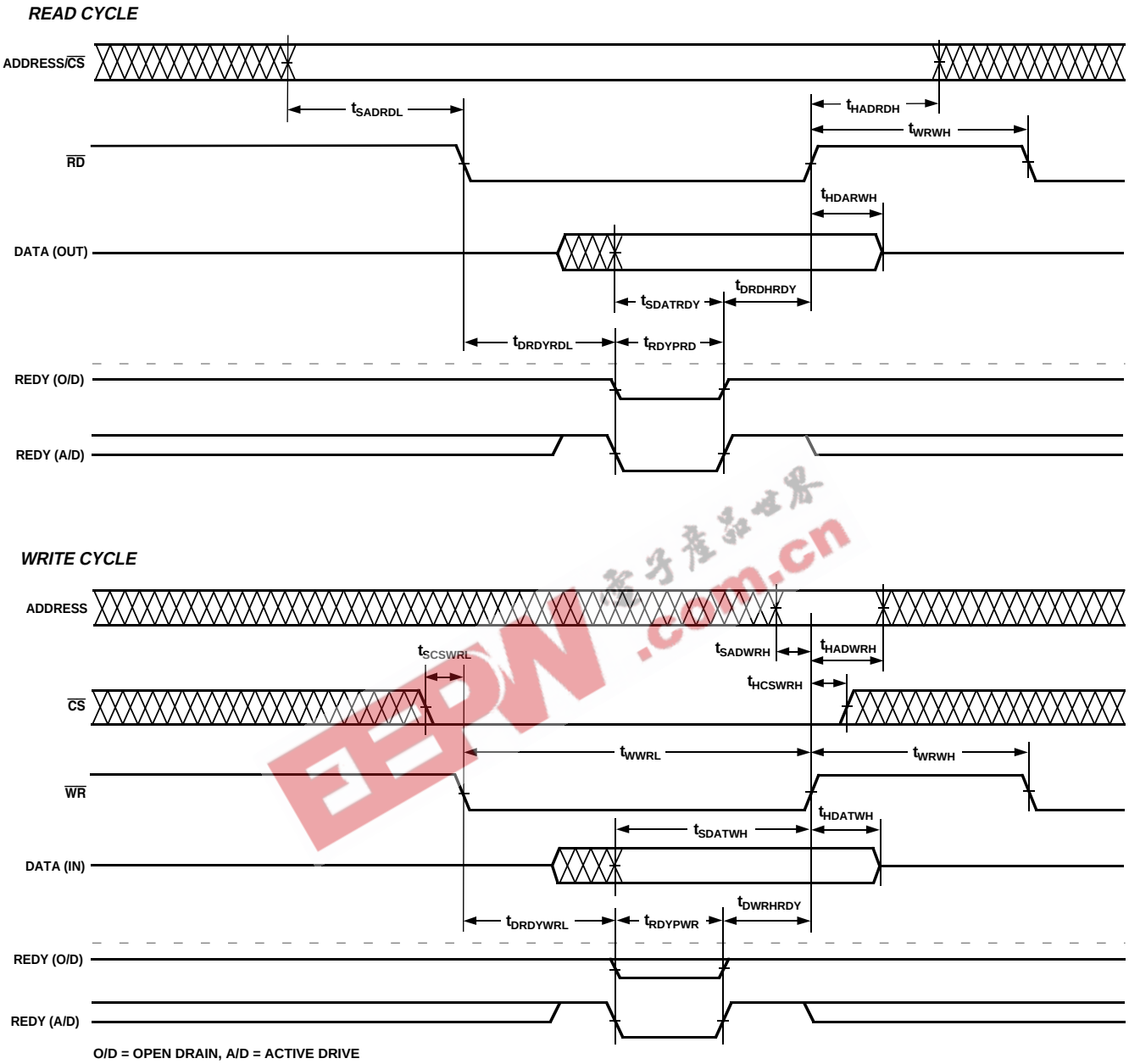


Figure 19b. Asynchronous Read/Write—Host to ADSP-2106x

Three-State Timing—Bus Master, Bus Slave, $\overline{\text{HBR}}$, $\overline{\text{SBTS}}$

These specifications show how the memory interface is disabled (stops driving) or enabled (resumes driving) relative to CLKIN and the $\overline{\text{SBTS}}$ pin. This timing is applicable to bus master transition cycles (BTC) and host transition cycles (HTC) as well as the $\overline{\text{SBTS}}$ pin.

Parameter		5 V Min	5 V Max	3.3 V Min	3.3 V Max	Units
Timing Requirements:						
t_{STSCK}	$\overline{\text{SBTS}}$ Setup Before CLKIN	12 + DT/2		12 + DT/2		ns
t_{HTSCK}	$\overline{\text{SBTS}}$ Hold Before CLKIN		5.5 + DT/2		5.5 + DT/2	ns
Switching Characteristics:						
t_{MIENA}	Address/Select Enable After CLKIN	–1.5 – DT/8		–1.25 – DT/8		ns
t_{MIENS}	Strobes Enable After CLKIN[1]	–1.5 – DT/8		–1.5 – DT/8		ns
t_{MIENHG}	$\overline{\text{HBG}}$ Enable After CLKIN	–1.5 – DT/8		–1.5 – DT/8		ns
t_{MITRA}	Address/Select Disable After CLKIN		1 – DT/4		1 – DT/4	ns
t_{MITRS}	Strobes Disable After CLKIN[1]		2.5 – DT/4		2.5 – DT/4	ns
t_{MITRHG}	$\overline{\text{HBG}}$ Disable After CLKIN		3 – DT/4		3 – DT/4	ns
t_{DATEN}	Data Enable After CLKIN[2]	9 + 5DT/16		9 + 5DT/16		ns
t_{DATTR}	Data Disable After CLKIN[2]	0 – DT/8	8 – DT/8	0 – DT/8	8 – DT/8	ns
t_{ACKEN}	ACK Enable After CLKIN[2]	7.5 + DT/4		7.5 + DT/4		ns
t_{ACKTR}	ACK Disable After CLKIN[2]	–1 – DT/8	7 – DT/8	–1 – DT/8	7 – DT/8	ns
t_{ADCEN}	ADRCLK Enable After CLKIN	–2 – DT/8		–2 – DT/8		ns
t_{ADCTR}	ADRCLK Disable After CLKIN		9 – DT/4		9 – DT/4	ns
t_{MTRHBG}	Memory Interface Disable Before $\overline{\text{HBG}}$ Low[3]	–1 + DT/8		–1 + DT/8		ns
t_{MENHBG}	Memory Interface Enable After $\overline{\text{HBG}}$ High[3]	18.5 + DT		18.5 + DT		ns

NOTES
[1]Strobes = $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{SW}}$, PAGE, $\overline{\text{DMAG}}$.
[2]In addition to bus master transition cycles, these specs also apply to bus master and bus slave synchronous read/write.
[3]Memory Interface = Address, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{MS}}$x, $\overline{\text{SW}}$, $\overline{\text{HBG}}$, PAGE, $\overline{\text{DMAG}}$x, $\overline{\text{BMS}}$ (in EPROM boot mode).

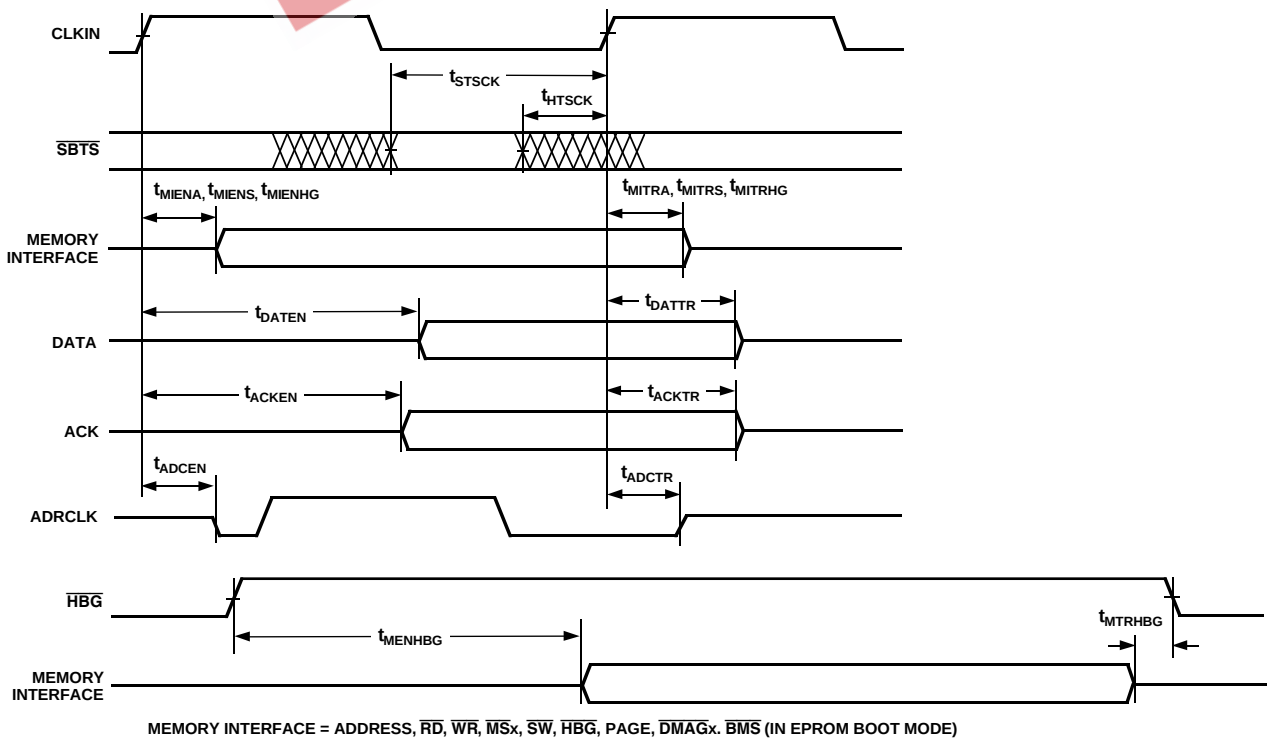


Figure 20. Three-State Timing

DMA Handshake

These specifications describe the three DMA handshake modes. In all three modes $\overline{\text{DMAR}}$ is used to initiate transfers. For handshake mode, $\overline{\text{DMAG}}$ controls the latching or enabling of data externally. For external handshake mode, the data transfer is controlled by the $ADDR_{31-0}$, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, PAGE, $\overline{MS}_{3-0}$, ACK, and $\overline{\text{DMAG}}$ signals. For Paced Master mode, the data transfer is controlled by $ADDR_{31-0}$, $\overline{RD}$, $\overline{WR}$, $\overline{MS}_{3-0}$, and ACK (not $\overline{\text{DMAG}}$). For Paced Master mode, the "Memory Read–Bus Master", "Memory Write–Bus Master", and "Synchronous Read/Write–Bus Master" timing specifications for $ADDR_{31-0}$, $\overline{RD}$, $\overline{WR}$, $\overline{MS}_{3-0}$, $\overline{SW}$, PAGE, $DATA_{47-0}$, and ACK also apply.

Parameter		5 V Min	5 V Max	3.3 V Min	3.3 V Max	Units
Timing Requirements:						
t_{SDRLC}	$\overline{\text{DMAR}}$x Low Setup Before CLKIN[1]	5		5		ns
t_{SDRHC}	$\overline{\text{DMAR}}$x High Setup Before CLKIN[1]	5		5		ns
t_{WDR}	$\overline{\text{DMAR}}$x Width Low (Nonsynchronous)	6		6		ns
$t_{SDATDGL}$	Data Setup After $\overline{\text{DMAG}}$x Low[2]		9.5 + 5DT/8		9.5 + 5DT/8	ns
$t_{HDATIDG}$	Data Hold After $\overline{\text{DMAG}}$x High	2.5		2.5		ns
t_{DATDRH}	Data Valid After $\overline{\text{DMAG}}$x High[2]		15.5 + 7DT/8		15.5 + 7DT/8	ns
t_{DMARLL}	$\overline{\text{DMAG}}$x Low Edge to Low Edge	23 + 7DT/8		23 + 7DT/8		ns
t_{DMARH}	$\overline{\text{DMAG}}$x Width High	6		6		ns
Switching Characteristics:						
t_{DDGL}	$\overline{\text{DMAG}}$x Low Delay After CLKIN	9 + DT/4	16 + DT/4	9 + DT/4	16 + DT/4	ns
t_{WDGH}	$\overline{\text{DMAG}}$x High Width	6 + 3DT/8		6 + 3DT/8		ns
t_{WDGL}	$\overline{\text{DMAG}}$x Low Width	12 + 5DT/8		12 + 5DT/8		ns
t_{HDGC}	$\overline{\text{DMAG}}$x High Delay After CLKIN	–2 – DT/8	7 – DT/8	–2 – DT/8	7 – DT/8	ns
$t_{VDATDGH}$	Data Valid Before $\overline{\text{DMAG}}$x High[3]	7.5 + 9DT/16		7.5 + 9DT/16		ns
$t_{DATRDGH}$	Data Disable After $\overline{\text{DMAG}}$x High[4]	–0.5	8	–0.5	8	ns
t_{DGWRL}	$\overline{WR}$ Low Before $\overline{\text{DMAG}}$x Low	–0.5	2.5	–0.5	2.5	ns
t_{DGWRH}	$\overline{\text{DMAG}}$x Low Before $\overline{WR}$ High	9.5 + 5DT/8 + W		9.5 + 5DT/8 + W		ns
t_{DGWRR}	$\overline{WR}$ High Before $\overline{\text{DMAG}}$x High	0.5 + DT/16	3.5 + DT/16	0.5 + DT/16	3.5 + DT/16	ns
t_{DGRDL}	$\overline{RD}$ Low Before $\overline{\text{DMAG}}$x Low	–0.5	2	–0.5	2	ns
t_{DRDGH}	$\overline{RD}$ Low Before $\overline{\text{DMAG}}$x High	10.5 + 9DT/16 + W		10.5 + 9DT/16 + W		ns
t_{DGRDR}	$\overline{RD}$ High Before $\overline{\text{DMAG}}$x High	–0.5	3.5	–0.5	3.5	ns
t_{DGWR}	$\overline{\text{DMAG}}$x High to $\overline{WR}$, $\overline{RD}$, $\overline{\text{DMAG}}$x Low	4.5 + 3DT/8 + HI		4.5 + 3DT/8 + HI		ns
t_{DADGH}	Address/Select Valid to $\overline{\text{DMAG}}$x High	16 + DT		16 + DT		ns
t_{DDGHA}	Address/Select Hold after $\overline{\text{DMAG}}$x High	–1		–1		ns

W = (number of wait states specified in WAIT register) × t_{CK}.
HI = t_{CK} (if an address hold cycle or bus idle cycle occurs, as specified in WAIT register; otherwise HI = 0).

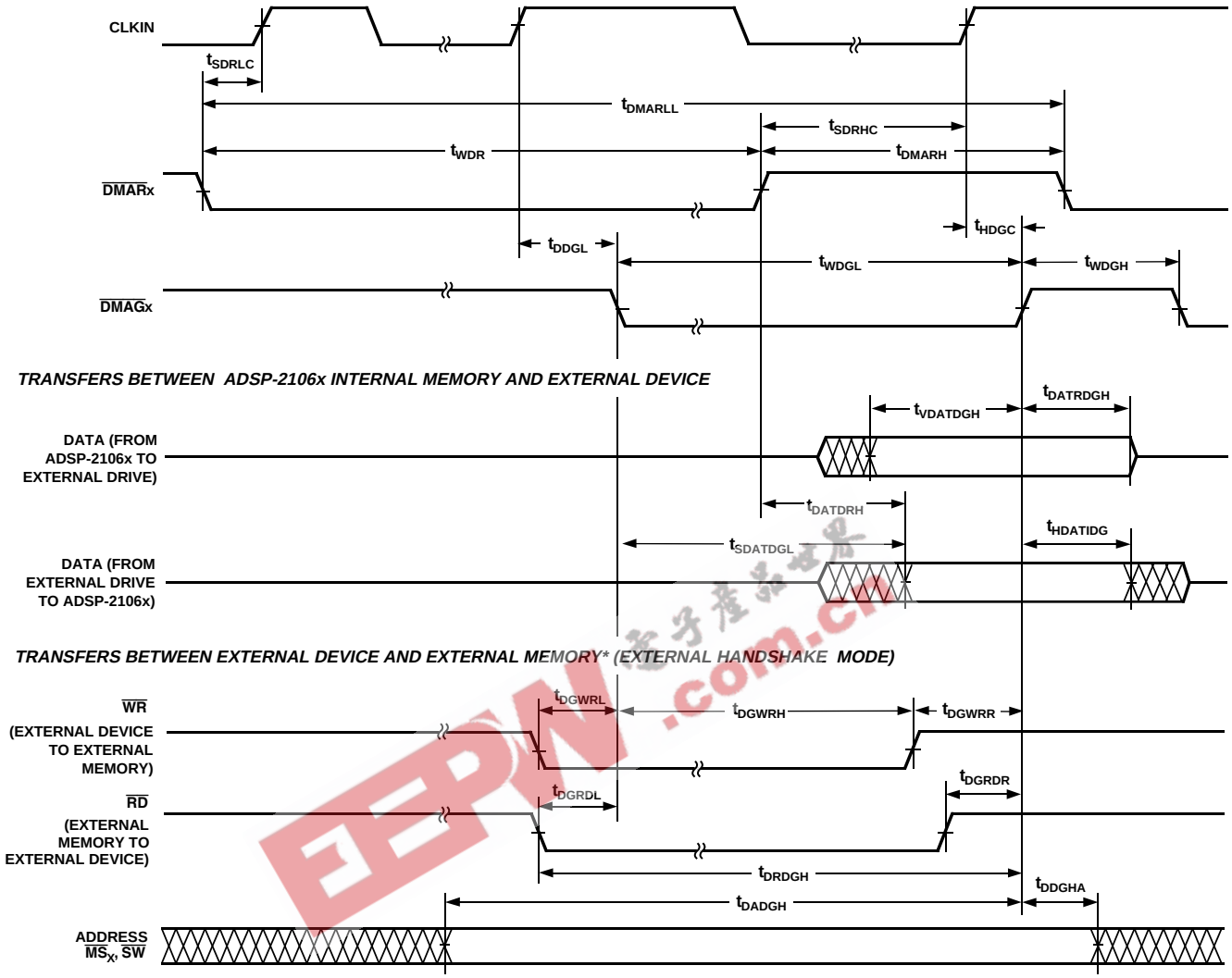
NOTES

[1]Only required for recognition in the current cycle.

[2]$t_{SDATDGL}$ is the data setup requirement if $\overline{\text{DMAR}}$x is not being used to hold off completion of a write. Otherwise, if $\overline{\text{DMAR}}$x low holds off completion of the write, the data can be driven t_{DATDRH} after $\overline{\text{DMAR}}$x is brought high.

[3]$t_{VDATDGH}$ is valid if $\overline{\text{DMAR}}$x is not being used to hold off completion of a read. If $\overline{\text{DMAR}}$x is used to prolong the read, then $t_{VDATDGH}$ = 7.5 + 9DT/16 + (n × t_{CK}) where *n* equals the number of extra cycles that the access is prolonged.

[4]See System Hold Time Calculation under Test Conditions for calculation of hold times given capacitive and dc loads.



* "MEMORY READ – BUS MASTER," "MEMORY WRITE – BUS MASTER," AND "SYNCHRONOUS READ/WRITE – BUS MASTER" TIMING SPECIFICATIONS FOR ADDR$_{31-0}$, RD, WR, SW, MS$_{3-0}$ AND ACK ALSO APPLY HERE.

Figure 21. DMA Handshake Timing

Link Ports: 1 × CLK Speed Operation

Parameter		5 V Min	5 V Max	3.3 V Min	3.3 V Max	Units
Receive						
Timing Requirements:						
t_{SLDCL}	Data Setup Before LCLK Low	3.5		3		ns
t_{HLDCL}	Data Hold After LCLK Low	3		3		ns
t_{LCLKIW}	LCLK Period (1 × Operation)	t_{CK}		t_{CK}		ns
$t_{LCLKRWL}$	LCLK Width Low	6		6		ns
$t_{LCLKRWH}$	LCLK Width High	5		5		ns
Switching Characteristics:						
t_{DLAHC}	LACK High Delay After CLKIN High	18 + DT/2	29.5 + DT/2	18 + DT/2	29.5 + DT/2	ns
t_{DLALC}	LACK Low Delay After LCLK High[1]	–3	13.5	–3	13.5	ns
t_{ENDLK}	LACK Enable from CLKIN	5 + DT/2		5 + DT/2		ns
t_{TDLK}	LACK Disable from CLKIN		21 + DT/2		21 + DT/2	ns
Transmit						
Timing Requirements:						
t_{SLACH}	LACK Setup Before LCLK High	18		20		ns
t_{HLACH}	LACK Hold After LCLK High	–7		–7		ns
Switching Characteristics:						
t_{DLCLK}	LCLK Delay After CLKIN (1 × Operation)		16.5		17.5	ns
t_{DLDCH}	Data Delay After LCLK High		3.5		3	ns
t_{HLDCH}	Data Hold After LCLK High	–3		–3		ns
$t_{LCLKTWL}$	LCLK Width Low	$(t_{CK}/2) - 2$	$(t_{CK}/2) + 2$	$(t_{CK}/2) - 1$	$(t_{CK}/2) + 1.25$	ns
$t_{LCLKTWH}$	LCLK Width High	$(t_{CK}/2) - 2$	$(t_{CK}/2) + 2$	$(t_{CK}/2) - 1.25$	$(t_{CK}/2) + 1$	ns
t_{DLACLK}	LCLK Low Delay After LACK High	$(t_{CK}/2) + 8.5$	$(3 \times t_{CK}/2) + 17.5$	$(t_{CK}/2) + 8$	$(3 \times t_{CK}/2) + 18$	ns
t_{ENDLK}	LDAT, LCLK Enable After CLKIN	5 + DT/2		5 + DT/2		ns
t_{TDLK}	LDAT, LCLK Disable After CLKIN		21 + DT/2		21 + DT/2	ns
Link Port Service Request Interrupts: 1 × and 2 × Speed Operations						
Timing Requirements:						
t_{SLCK}	LACK/LCLK Setup Before CLKIN Low[2]	10		10		ns
t_{HLCK}	LACK/LCLK Hold After CLKIN Low[2]	2.5		2.5		ns

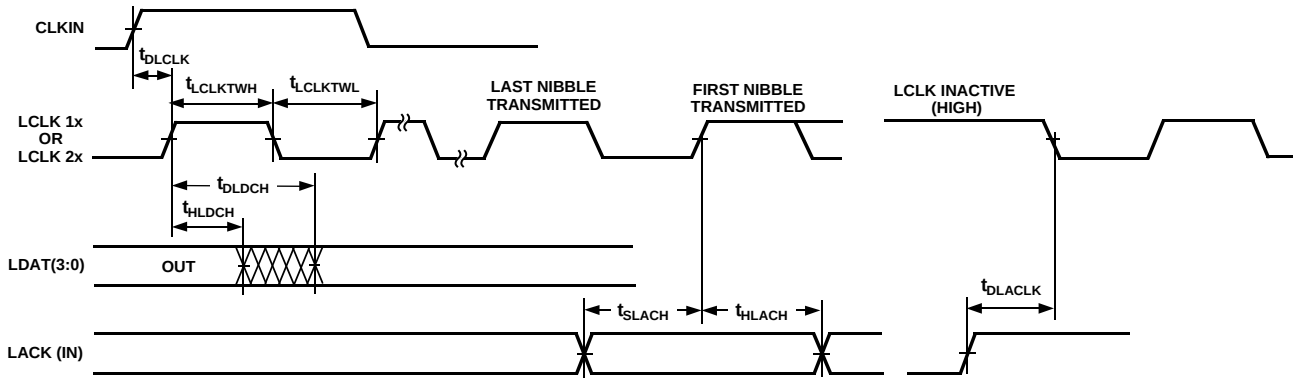
NOTES
[1]LACK will go low with t_{DLALC} relative to rising edge of LCLK after first nibble is received. LACK will not go low if the receiver's link buffer is not about to fill.
[2]Only required for interrupt recognition in the current cycle.

Link Ports: 2× CLK Speed Operation

Parameter		5 V Min	5 V Max	3.3 V Min	3.3 V Max	Units
Receive						
Timing Requirements:						
t_{SLDCL}	Data Setup Before LCLK Low	2.5		2.25		ns
t_{HLDCL}	Data Hold After LCLK Low	2.25		2.25		ns
t_{LCLKIW}	LCLK Period (2 × Operation)	$t_{CK}/2$		$t_{CK}/2$		ns
$t_{LCLKRWL}$	LCLK Width Low	4.5		5		ns
$t_{LCLKRWH}$	LCLK Width High	4.25		4		ns
Switching Characteristics:						
t_{DLAHC}	LACK High Delay After CLKIN High	18 + DT/2	29.5 + DT/2	18 + DT/2	30.5 + DT/2	ns
t_{DLALC}	LACK Low Delay After LCLK High[1]	6	16.5	6	18.5	ns
Transmit						
Timing Requirements:						
t_{SLACH}	LACK Setup Before LCLK High	19		19		ns
t_{HLACH}	LACK Hold After LCLK High	–6.75		–6.5		ns
Switching Characteristics:						
t_{DLCLK}	LCLK Delay After CLKIN		9		9	ns
t_{DLDCH}	Data Delay After LCLK High		3		2.75	ns
t_{HLDCH}	Data Hold After LCLK High	–2		–2		ns
$t_{LCLKTWL}$	LCLK Width Low	$(t_{CK}/4) – 1$	$(t_{CK}/4) + 1$	$(t_{CK}/4) – 0.75$	$(t_{CK}/4) + 1.5$	ns
$t_{LCLKTWH}$	LCLK Width High	$(t_{CK}/4) – 1$	$(t_{CK}/4) + 1$	$(t_{CK}/4) – 1.5$	$(t_{CK}/4) + 1$	ns
t_{DLACLK}	LCLK Low Delay After LACK High	$(t_{CK}/4) + 9$	$(3 × t_{CL}/4) + 17$	$(t_{CK}/4) + 9$	$(3 × t_{CL}/4) + 17$	ns

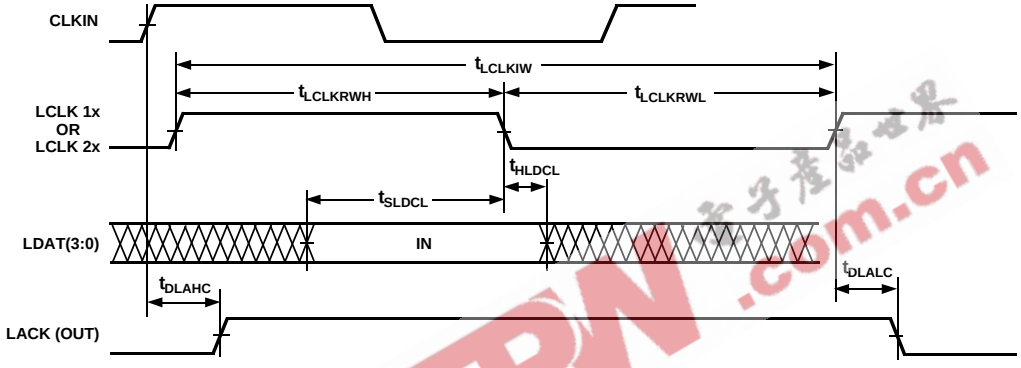
NOTE
[1]LACK will go low with t_{DLALC} relative to rising edge of LCLK after first nibble is received. LACK will not go low if the receiver's link buffer is not about to fill.

TRANSMIT



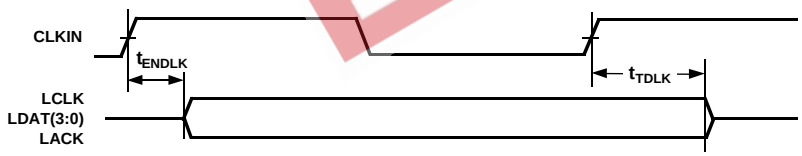
THE t_{SLACH} REQUIREMENT APPLIES TO THE RISING EDGE OF LCLK ONLY FOR THE FIRST NIBBLE TRANSMITTED.

RECEIVE



LACK GOES LOW ONLY AFFTER THE SECOND NIBBLE IS RECEIVED.

LINK PORT ENABLE/THREE-STATE DELAY FROM INSTRUCTION



LINK PORT ENABLE OR THREE-STATE TAKES EFFECT 2 CYCLES AFTER A WRITE TO A LINK PORT CONTROL REGISTER.

LINK PORT INTERRUPT SETUP TIME

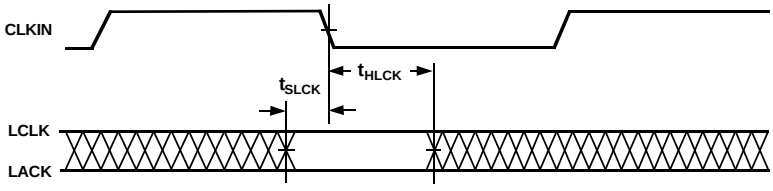


Figure 22. Link Ports

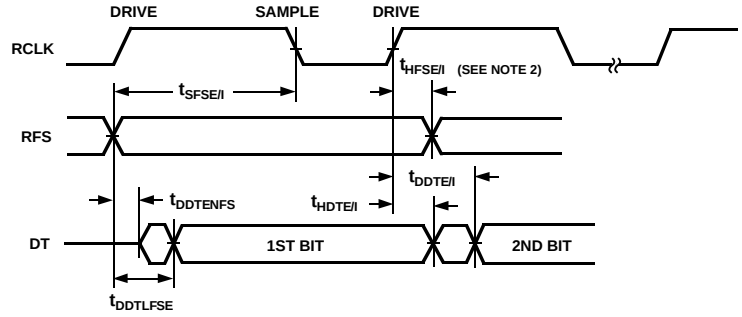
Serial Ports

Parameter		5 V Min	5 V Max	3.3 V Min	3.3 V Max	Units
External Clock						
Timing Requirements:						
t_{SFSE}	TFS/RFS Setup Before TCLK/RCLK[1]	4		4		ns
t_{HFSE}	TFS/RFS Hold After TCLK/RCLK[1, 2]	4.5		4.5		ns
t_{SDRE}	Receive Data Setup Before RCLK[1]	2		2		ns
t_{HDRE}	Receive Data Hold After RCLK[1]	4.5		4.5		ns
t_{SCLKW}	TCLK/RCLK Width	9.5		9		ns
t_{SCLK}	TCLK/RCLK Period	t_{CK}		t_{CK}		ns
Internal Clock						
Timing Requirements:						
t_{SFSI}	TFS Setup Before TCLK[1]; RFS Setup Before RCLK[1]	9		9		ns
t_{HFSI}	TFS/RFS Hold After TCLK/RCLK[1, 2]	1		1		ns
t_{SDRI}	Receive Data Setup Before RCLK[1]	4		4		ns
t_{HDRI}	Receive Data Hold After RCLK[1]	3		3		ns
External or Internal Clock						
Switching Characteristics:						
t_{DFSE}	RFS Delay After RCLK (Internally Generated RFS)[3]		14		14	ns
t_{HFSE}	RFS Hold After RCLK (Internally Generated RFS)[3]	3		3		ns
External Clock						
Switching Characteristics:						
t_{DFSE}	TFS Delay After TCLK (Internally Generated TFS)[3]		14		14	ns
t_{HFSE}	TFS Hold After TCLK (Internally Generated TFS)[3]	3		3		ns
t_{DDTE}	Transmit Data Delay After TCLK[3]		17		17	ns
t_{HDTE}	Transmit Data Hold After TCLK[3]	5		5		ns
Internal Clock						
Switching Characteristics:						
t_{DFSI}	TFS Delay After TCLK (Internally Generated TFS)[3]		5		5	ns
t_{HFSI}	TFS Hold After TCLK (Internally Generated TFS)[3]	–1.5		–1.5		ns
t_{DDTI}	Transmit Data Delay After TCLK[3]		8		8	ns
t_{HDTI}	Transmit Data Hold After TCLK[3]	0		0		ns
t_{SCLKIW}	TCLK/RCLK Width	(SCLK/2) – 2	(SCLK/2) + 2	(SCLK/2) – 2.5	(SCLK/2) + 2.5	ns
Enable and Three-State						
Switching Characteristics:						
t_{DDTEN}	Data Enable from External TCLK[3]	3.5		4		ns
t_{DDTTE}	Data Disable from External TCLK[3]		11.5		11.5	ns
t_{DDTIN}	Data Enable from Internal TCLK[3]	0		0		ns
t_{DDTTI}	Data Disable from Internal TCLK[3]		3		3	ns
t_{DCLK}	TCLK/RCLK Delay from CLKIN		23 + 3DT/8		23 + 3DT/8	ns
t_{DPTR}	SPORT Disable After CLKIN		18		18	ns
External Late Frame Sync						
Switching Characteristics:						
$t_{DDTLFSE}$	Data Delay from Late External TFS or External RFS with MCE = 1, MFD = 0[4]		13		13.8	ns
$t_{DDTENFS}$	Data Enable from late FS or MCE = 1, MFD = 0[4]	3.0		3.5		ns

To determine whether communication is possible between two devices at clock speed *n*, the following specifications must be confirmed: 1) frame sync delay and frame sync setup and hold, 2) data delay and data setup and hold, and 3) SCLK width.

NOTES
[1]Referenced to sample edge.
[2]RFS hold after RCK when MCE = 1, MFD = 0 is 0.5 ns minimum from drive edge. TFS hold after TCK for late external TFS is 0.5 ns minimum from drive edge.
[3]Referenced to drive edge.
[4]MCE = 1, TFS enable and TFS valid follow $t_{DDTLFSE}$ and $t_{DDTENFS}$.

EXTERNAL RFS with MCE = 1, MFD = 0



LATE EXTERNAL TFS

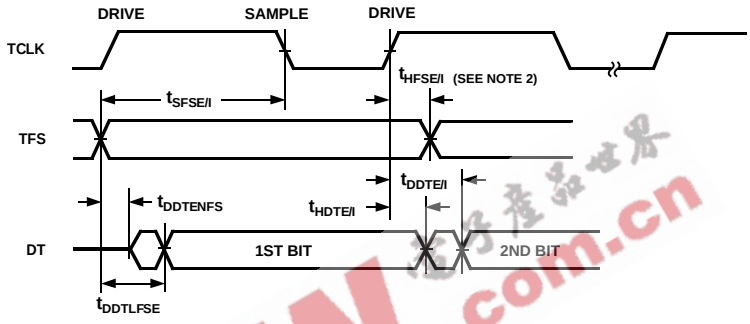
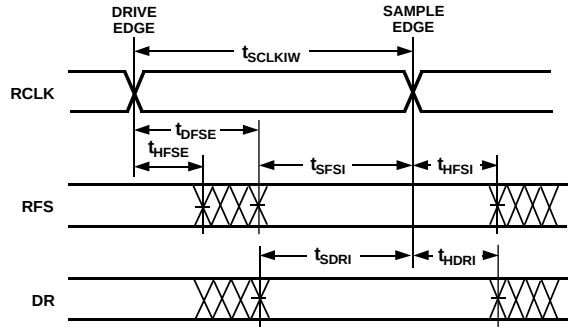
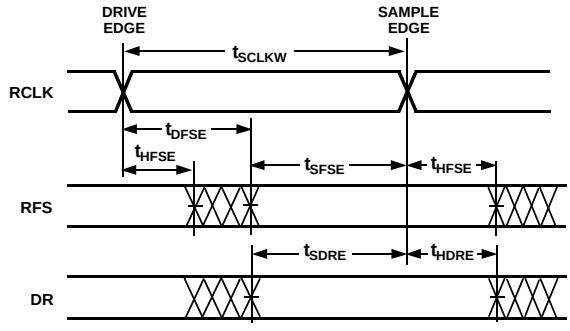


Figure 23. External Late Frame Sync

DATA RECEIVE– INTERNAL CLOCK

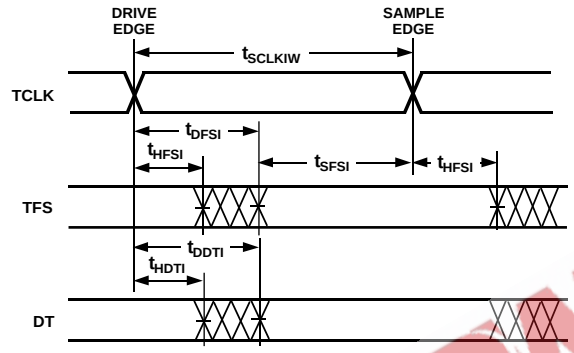


DATA RECEIVE– EXTERNAL CLOCK

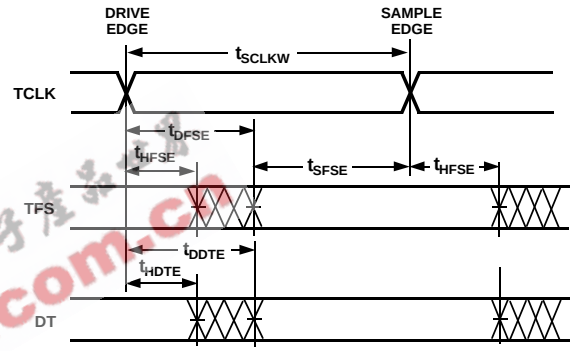


NOTE: EITHER THE RISING EDGE OR FALLING EDGE OF RCLK, TCLK CAN BE USED AS THE ACTIVE SAMPLING EDGE.

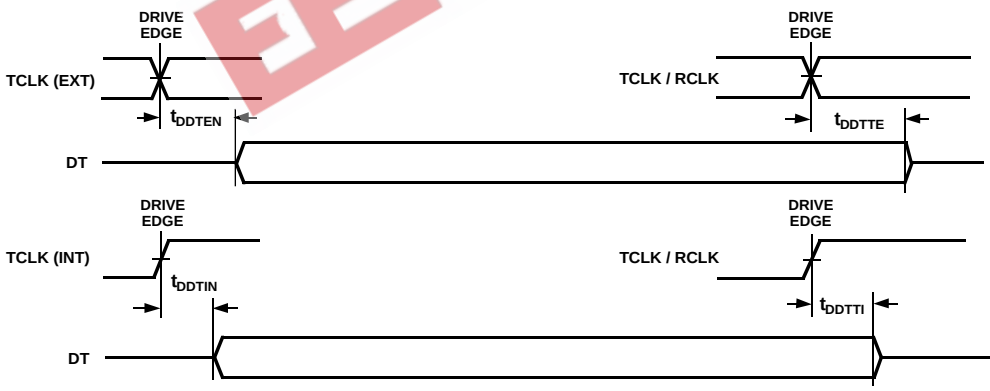
DATA TRANSMIT– INTERNAL CLOCK

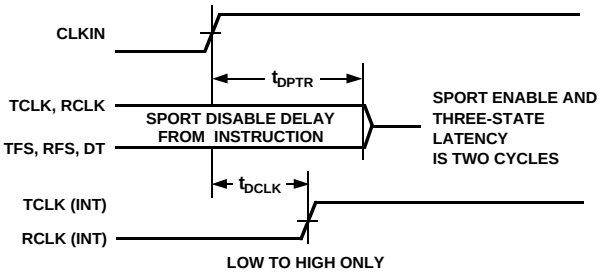


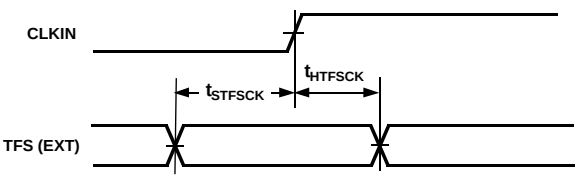
DATA TRANSMIT– EXTERNAL CLOCK



NOTE: EITHER THE RISING EDGE OR FALLING EDGE OF RCLK, TCLK CAN BE USED AS THE ACTIVE SAMPLING EDGE.







NOTE: APPLIES ONLY TO GATED SERIAL CLOCK MODE WITH EXTERNAL TFS, AS USED IN THE SERIAL PORT SYSTEM I/O FOR MESH MULTIPROCESSING.

Figure 24. Serial Ports

JTAG Test Access Port and Emulation

Parameter		5 V Min	5 V Max	3.3 V Min	3.3 V Max	Units
Timing Requirements:						
t_{TCK}	TCK Period	t_{CK}		t_{CK}		ns
t_{STAP}	TDI, TMS Setup Before TCK High	5		5		ns
t_{HTAP}	TDI, TMS Hold After TCK High	6		6		ns
t_{SSYS}	System Inputs Setup Before TCK Low[1]	8		8		ns
t_{HSYS}	System Inputs Hold After TCK Low[1]	18.5		19		ns
t_{TRSTW}	$\overline{TRST}$ Pulsewidth	$4t_{CK}$		$4t_{CK}$		ns
Switching Characteristics:						
t_{DTDO}	TDO Delay from TCK Low		13		13	ns
t_{DSYS}	System Outputs Delay After TCK Low [2]		20		20	ns

NOTES

[1]System Inputs = $DATA_{47-0}$, $ADDR_{31-0}$, $\overline{RD}$, $\overline{WR}$, ACK, $\overline{SBTS}$, $\overline{SW}$, $\overline{HBR}$, $\overline{HBG}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{BR}_{6-1}$, RPBA, $\overline{IRQ}_{2-0}$, FLAG2-0, DR0, DR1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, $LxDAT_{3-0}$, LxCLK, LxACK, EBOOT, LBOOT, $\overline{BMS}$, CLKIN, $\overline{RESET}$.

[2]System Outputs = $DATA_{47-0}$, $ADDR_{31-0}$, $\overline{MS}_{3-0}$, $\overline{RD}$, $\overline{WR}$, ACK, PAGE, ADRCLK, $\overline{SW}$, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BR}_{6-1}$, $\overline{CPA}$, $FLAG_{2-0}$, TIMEXP, DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, $LxDAT_{3-0}$, LxCLK, LxACK, $\overline{BMS}$.

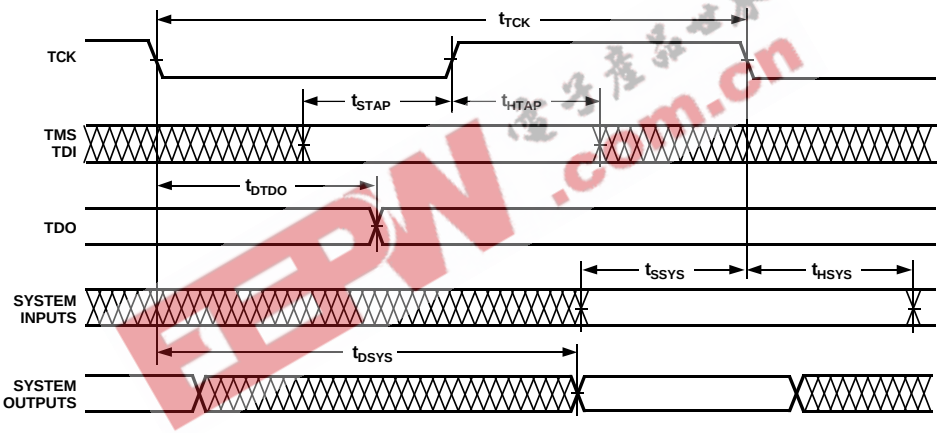


Figure 25. IEEE 11499.1 JTAG Test Access Port

OUTPUT DRIVE CURRENTS

Figure 26 shows typical I-V characteristics for the output drivers of the ADSP-2106x. The curves represent the current drive capability of the output drivers as a function of output voltage.

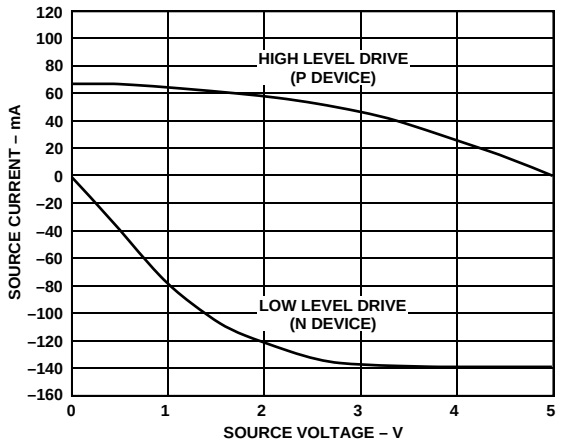


Figure 26. ADSP-2106x Typical Drive Currents (V_{DD} = 5 V)

POWER DISSIPATION

Total power dissipation has two components, one due to internal circuitry and one due to the switching of external output drivers. Internal power dissipation is dependent on the instruction execution sequence and the data operands involved. Internal power dissipation is calculated in the following way:

$$P_{INT} = I_{DDIN} \times V_{DD}$$

The external component of total power dissipation is caused by the switching of output pins. Its magnitude depends on:

– the number of output pins that switch during each cycle (O)
– the maximum frequency at which they can switch (f)
– their load capacitance (C)
– their voltage swing (V_{DD})

and is calculated by:

$$P_{EXT} = O \times C \times V_{DD}^2 \times f$$

The load capacitance should include the processor's package capacitance (C_{IN}). The switching frequency includes driving the load high and then back low. Address and data pins can drive high and low at a maximum rate of $1/(2t_{CK})$. The write strobe can switch every cycle at a frequency of $1/t_{CK}$. Select pins switch at $1/(2t_{CK})$, but selects can switch on each cycle.

Example:

Estimate P_{EXT} with the following assumptions:

–A system with one bank of external data memory RAM (32-bit)
–Four 128K × 8 RAM chips are used, each with a load of 10 pF
–External data memory writes occur every other cycle, a rate of $1/(4t_{CK})$, with 50% of the pins switching
–The instruction cycle rate is 40 MHz (t_{CK} = 25 ns) and V_{DD} = 5.0 V.

The P_{EXT} equation is calculated for each class of pins that can drive:

Pin Type	# of Pins	% Switching	× C	× f	× V_{DD}^2	= P_{EXT}
Address	15	50	× 55 pF	× 20 MHz	× 25 V	= 0.206 W
$\overline{MS0}$	1	0	× 55 pF	× 20 MHz	× 25 V	= 0.00 W
$\overline{WR}$	1	–	× 55 pF	× 40 MHz	× 25 V	= 0.055 W
Data	32	50	× 25 pF	× 20 MHz	× 25 V	= 0.200 W
ADRCLK	1	–	× 15 pF	40 MHz	× 25 V	= 0.015 W

P_{EXT} (5 V) = 0.476 W
P_{EXT} (3.3 V) = 0.207 W

A typical power consumption can now be calculated for these conditions by adding a typical internal power dissipation:

$$P_{TOTAL} = P_{EXT} + (I_{DDIN2} \times 5.0\ V)$$

Note that the conditions causing a worst-case P_{EXT} are different from those causing a worst-case P_{INT}. Maximum P_{INT} cannot occur while 100% of the output pins are switching from all ones to all zeros. Also note that it is not common for an application to have 100% or even 50% of the outputs switching simultaneously.

TEST CONDITIONS

Output Disable Time

Output pins are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load, C_L, and the load current, I_L. This decay time can be approximated by the following equation:

$$t_{DECAY} = \frac{C_L\ \Delta V}{I_L}$$

The output disable time, t_{DIS}, is the difference between $t_{MEASURED}$ and t_{DECAY} as shown in Figure 27. The time $t_{MEASURED}$ is the interval from when the reference signal switches to when the output voltage decays ΔV from the measured output high or output low voltage. t_{DECAY} is calculated with test loads C_L and I_L, and with ΔV equal to 0.5 V.

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high impedance state to when they start driving. The output enable time, t_{ENA}, is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in the Output Enable/Disable diagram (Figure 27). If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the equation given above. Choose ΔV to be the difference between the ADSP-2106x's output voltage and the input threshold for the device requiring the hold time. A typical ΔV will be 0.4 V. C_L is the total bus capacitance (per data line), and I_L is the total leakage or three-state current

(per data line). The hold time will be t_{DECAY} plus the minimum disable time (i.e., t_{HDWD} for the write cycle).

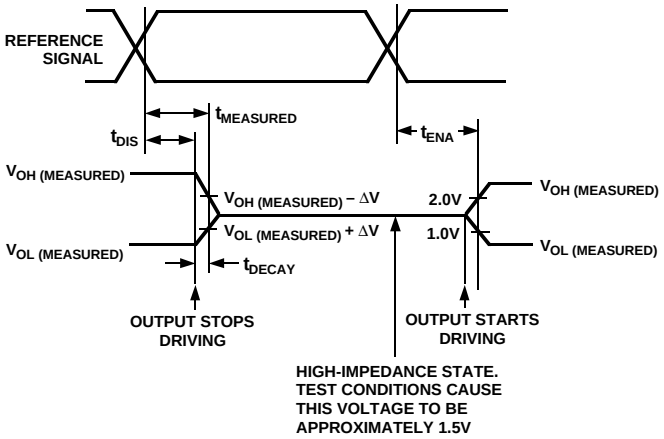


Figure 27. Output Enable/Disable

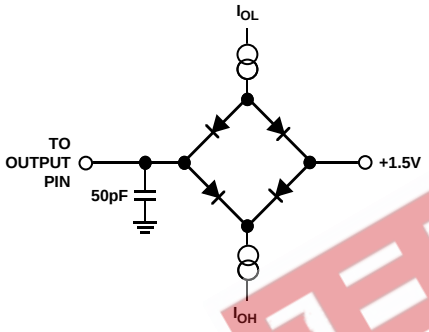


Figure 28. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

Figure 29. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Capacitive Loading

Output delays and holds are based on standard capacitive loads: 50 pF on all pins (see Figure 28). The delay and hold specifications given should be derated by a factor of 1.5 ns/50 pF for loads other than the nominal value of 50 pF. Figures 30 and 31 show how output rise time varies with capacitance. Figure 32 graphically shows how output delays and holds vary with load capacitance. (Note that this graph or derating does not apply to output disable delays; see the previous section Output Disable Time under Test Conditions.) The graphs of Figures 30, 31 and 32 may not be linear outside the ranges shown.

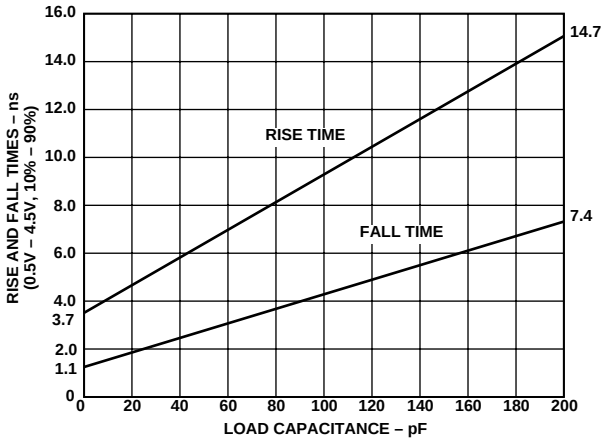


Figure 30. Typical Output Rise Time (10%–90% V_{DD}) vs. Load Capacitance (V_{DD} = 5 V)

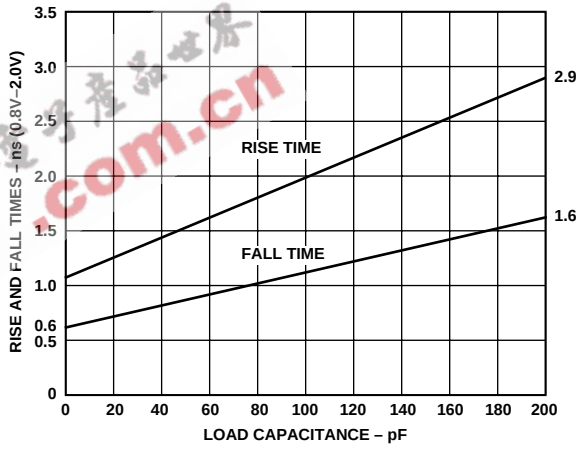


Figure 31. Typical Output Rise Time (0.8 V –2.0 V) vs. Load Capacitance (V_{DD} = 5 V)

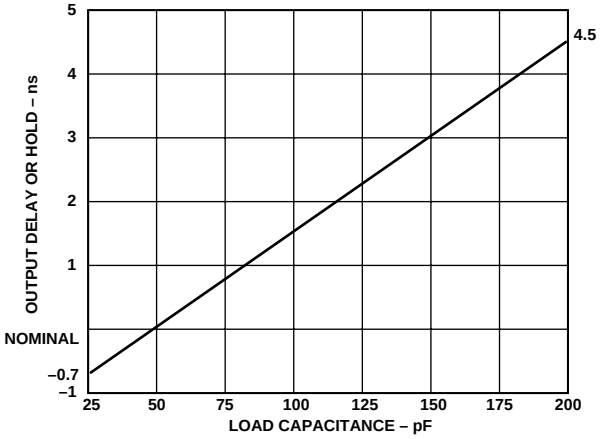


Figure 32. Typical Output Delay or Hold vs. Load Capacitance (at Maximum Case Temperature) (V_{DD} = 5 V)

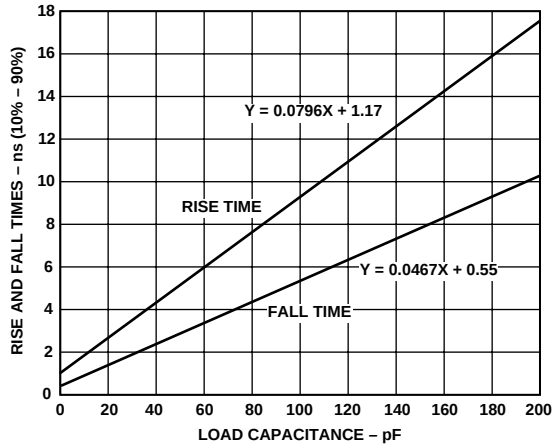


Figure 33. Typical Output Rise Time (10%–90% V_{DD}) vs. Load Capacitance (V_{DD} = 3.3 V)

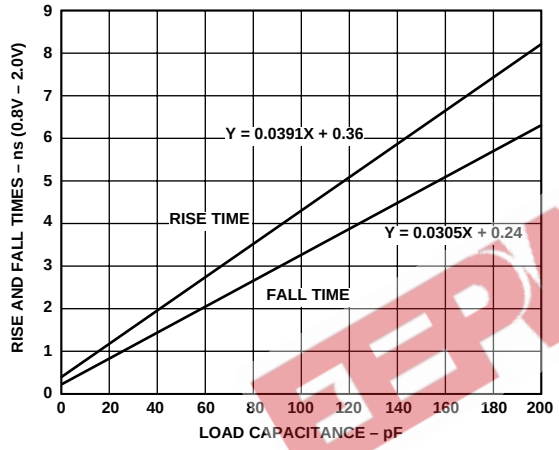


Figure 34. Typical Output Rise Time (0.8 V –2.0 V) vs. Load Capacitance (V_{DD} = 3.3 V)

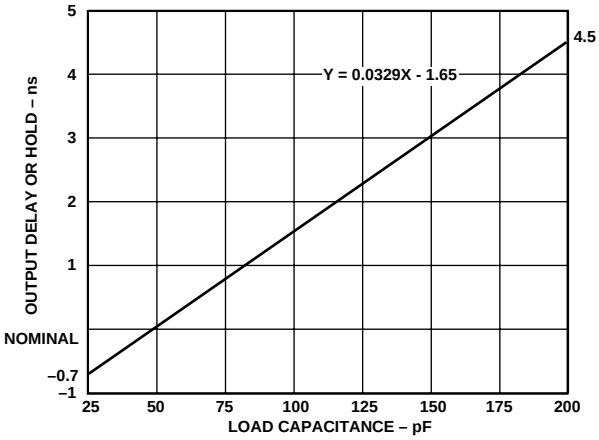


Figure 35. Typical Output Delay or Hold vs. Load Capacitance (at Maximum Case Temperature) (V_{DD} = 3.3 V)

AD14060/AD14060L ASSEMBLY RECOMMENDATIONS

SOCKET INFORMATION

Standard sockets and carriers are available for the AD14060/AD14060L, if needed. Socket part number IC53-3084-262 and carrier part number ICC-308-1 are available from Yamaichi Electronics.

Trim and Form

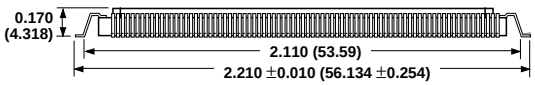
The AD14060/AD14060L will be shipped as shown on the final page of the data sheet with untrimmed and unformed leads and with the nonconductive tie bar in place. This avoids disturbance of lead spacing and coplanarity prior to assembly. Optimally, the leads should be trimmed, formed and solder-dipped just prior to placement on the board.

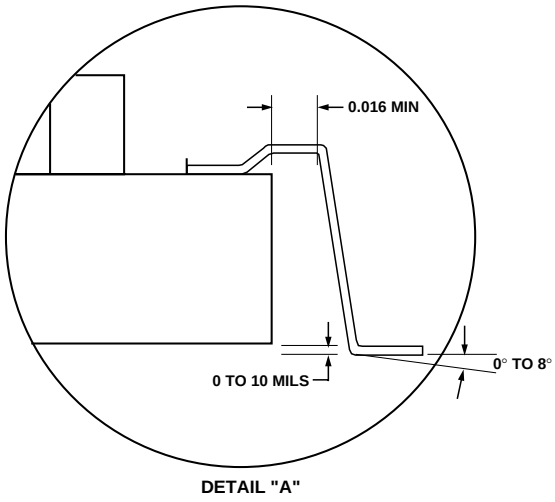
Trim/Form can be accomplished with a Universal Trim/Form, Customer-Designed Trim/Form, or with the Analog Devices' Developed Tooling described below.

A trim/form tool specific to the AD14060/AD14060L has been developed and is available for use by all parties at:

Tintronics Industries
2122-A Metro Circle
Huntsville, AL 35801
205-650-0220
Contact Person: Tom Rice

The package outline and dimensions resulting from this tool are shown below. (Alternatively, the package can also be trimmed/formed for cavity-down placement.)

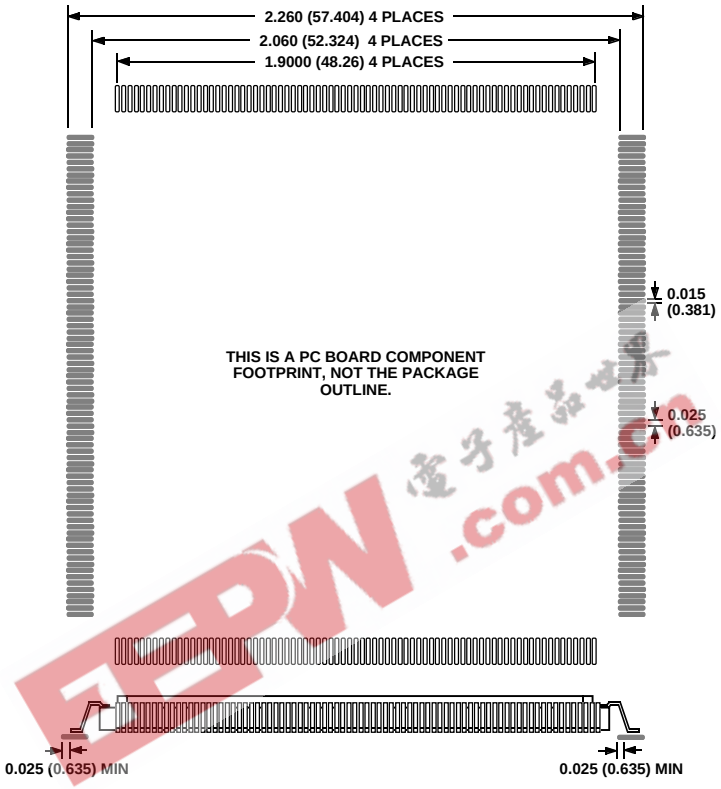




PCB LAYOUT GUIDELINES

The drawing below assumes that the trim/form tooling described above is used. These recommendations are provided for user convenience and are recommendations only, based on standard practice. PCB pad footprint geometries and placement are illustrated.

NOTE: These drawings are recommended PCB layout guidelines only, and they assume that the trim/form tooling described above is used.



Thermal Characteristics

The AD14060/AD14060L is packaged in a 308-lead ceramic quad flatpack (CQFP). The package is optimized for thermal conduction through the core (base of the package) down to the mounting surface. The AD14060/AD14060L is specified for a case temperature (T_{CASE}). Design of the mounting surface and attachment material should be such that T_{CASE} is not exceeded.

$$\theta_{JC} = 0.36°C/W$$

Thermal Cross-Section

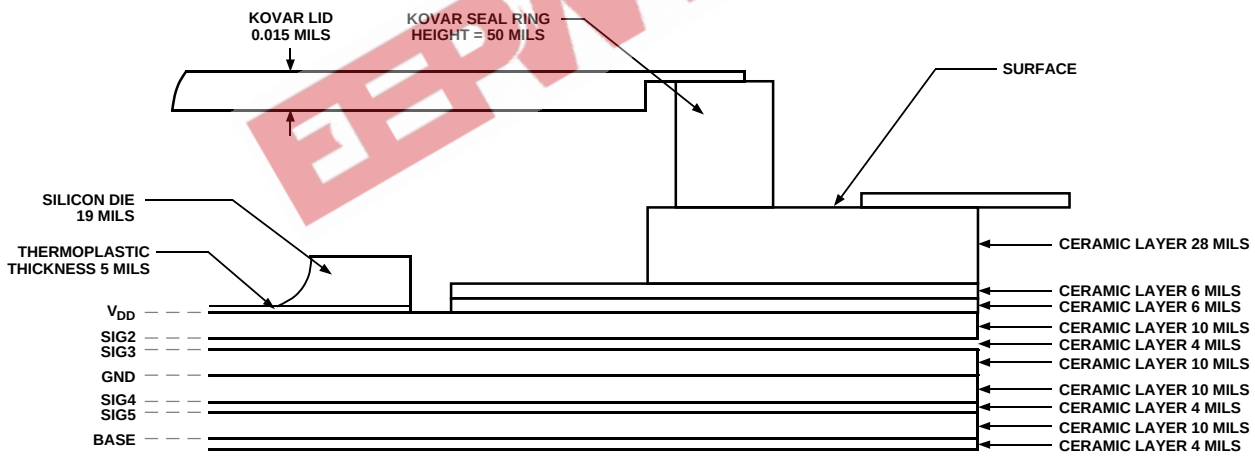
The data below, together with the detailed mechanical drawings at the end of the data sheet, allows for constructing simple thermal models for further analysis within targeted systems. The top layer of the package, where the die are mounted, is a metal V_{DD} layer. The approximate metal area coverage from the metal planes and routing layers is estimated below.

Thermal Conductivity

Material	Thermal Conductivity W/cm°C
Ceramic	0.18
Kovar	0.14
Tungsten	1.78
Thermoplastic	0.03
Silicon	1.45

Metal Coverage Per Layer

Layer	Percent Metal (1 Mil Thick)
V_{DD}	88
SIG2	16
SIG3	14
GND	91
SIG4	15
SIG5	13
BASE	95



MECHANICAL CHARACTERISTICS

Lid Deflection Analysis

External Pressure Reduction

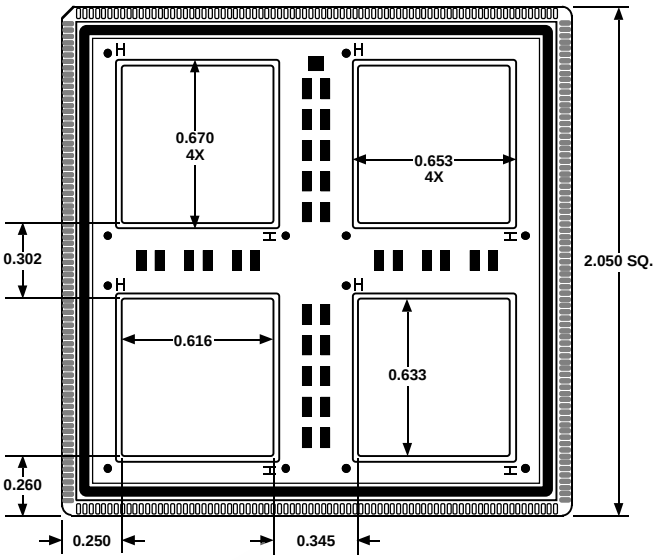
Delta Pressure	Deflection
12 psi	10.0 mil
15 psi	11.9 mil

Mechanical Model

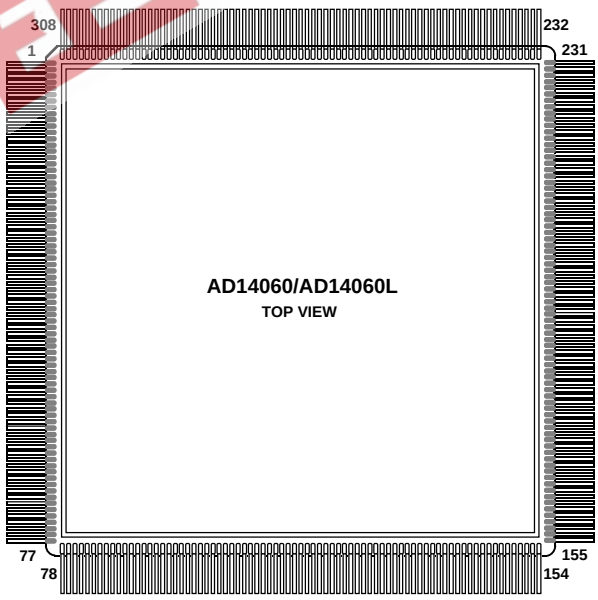
The data below, together with the detailed mechanical drawings at the end of the data sheet, allows for construction of simple mechanical models for further analysis within targeted systems.

Mechanical Properties

Material	Modulus of Elasticity
Ceramic	26×10^3 kg/mm^2
Kovar	14.1×10^3 kg/mm^2
Tungsten	35×10^3 kg/mm^2
Thermoplastic	279 kg/mm^2
Silicon	11×10^3 kg/mm^2



308-LEAD CQFP PIN CONFIGURATION



PIN CONFIGURATIONS

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	$\overline{WR}$	45	GND	89	ADDR13	133	$\overline{IRQ}$B0	177	LC4DAT2	221	GND	265	GND
2	$\overline{RD}$	46	RFSD1	90	ADDR12	134	$\overline{IRQ}$B1	178	LC4DAT3	222	LA3ACK	266	DATA24
3	GND	47	RCLKD1	91	ADDR11	135	$\overline{IRQ}$B2	179	GND	223	LA3CLK	267	DATA25
4	$\overline{CSA}$	48	DRD1	92	GND	136	GND	180	LC3ACK	224	LA3DAT0	268	DATA26
5	$\overline{CSB}$	49	TFSD1	93	ADDR10	137	$\overline{IRQ}$C0	181	LC3CLK	225	LA3DAT1	269	DATA27
6	$\overline{CSC}$	50	TCLKD1	94	ADDR9	138	$\overline{IRQ}$C1	182	LC3DAT0	226	LA3DAT2	270	V_{DD}
7	$\overline{CSD}$	51	DTD1	95	ADDR8	139	$\overline{IRQ}$C2	183	LC3DAT1	227	LA3DAT3	271	DATA28
8	GND	52	V_{DD}	96	V_{DD}	140	$\overline{IRQ}$D0	184	LC3DAT2	228	V_{DD}	272	DATA29
9	$\overline{HBG}$	53	$\overline{HBR}$	97	ADDR7	141	$\overline{IRQ}$D1	185	LC3DAT3	229	LA1ACK	273	DATA30
10	REDY	54	$\overline{DMAR1}$	98	ADDR6	142	$\overline{IRQ}$D2	186	V_{DD}	230	LA1CLK	274	DATA31
11	ADRCLK	55	$\overline{DMAR2}$	99	ADDR5	143	V_{DD}	187	LC1ACK	231	LA1DAT0	275	GND
12	V_{DD}	56	$\overline{SBTS}$	100	GND	144	EBOOTA	188	LC1CLK	232	LA1DAT1	276	DATA32
13	RFS0	57	$\overline{BMSA}$	101	ADDR4	145	LBOOTA	189	LC1DAT0	233	LA1DAT2	277	DATA33
14	RCLK0	58	$\overline{BMSBCD}$	102	ADDR3	146	EBOOTBCD	190	LC1DAT1	234	LA1DAT3	278	DATA34
15	DR0	59	$\overline{SW}$	103	ADDR2	147	LBOOTBCD	191	LC1DAT2	235	GND	279	DATA35
16	TFS0	60	GND	104	V_{DD}	148	GND	192	LC1DAT3	236	DATA0	280	V_{DD}
17	TCLK0	61	$\overline{MS0}$	105	ADDR1	149	$\overline{RESET}$	193	GND	237	DATA1	281	DATA36
18	DT0	62	$\overline{MS1}$	106	ADDR0	150	RPBA	194	LB4ACK	238	DATA2	282	DATA37
19	GND	63	$\overline{MS2}$	107	FLAGA0	151	GND	195	LB4CLK	239	DATA3	283	DATA38
20	CPAA	64	$\overline{MS3}$	108	GND	152	LD4ACK	196	LB4DAT0	240	V_{DD}	284	DATA39
21	CPAB	65	V_{DD}	109	FLAGA2	153	LD4CLK	197	LB4DAT1	241	DATA4	285	GND
22	CPAC	66	ADDR31	110	FLAGB0	154	LD4DAT0	198	LB4DAT2	242	DATA5	286	DATA40
23	CPAD	67	ADDR30	111	FLAGB2	155	LD4DAT1	199	LB4DAT3	243	DATA6	287	DATA41
24	V_{DD}	68	ADDR29	112	FLAGC0	156	LD4DAT2	200	V_{DD}	244	DATA7	288	CLKIN
25	RFSA1	69	GND	113	FLAGC2	157	LD4DAT3	201	LB3ACK	245	GND	289	GND
26	RCLKA1	70	ADDR28	114	FLAGD0	158	V_{DD}	202	LB3CLK	246	DATA8	290	DATA42
27	DRA1	71	ADDR27	115	FLAGD2	159	LD3ACK	203	LB3DAT0	247	DATA9	291	DATA43
28	TFSA1	72	ADDR26	116	V_{DD}	160	LD3CLK	204	LB3DAT1	248	DATA10	292	V_{DD}
29	TCLKA1	73	V_{DD}	117	FLAG1	161	LD3DAT0	205	LB3DAT2	249	DATA11	293	DATA44
30	DTA1	74	ADDR25	118	$\overline{EMU}$	162	LD3DAT1	206	LB3DAT3	250	V_{DD}	294	DATA45
31	GND	75	ADDR24	119	TIMEXPA	163	LD3DAT2	207	GND	251	DATA12	295	DATA46
32	RFSB1	76	ADDR23	120	TIMEXPB	164	LD3DAT3	208	LB1ACK	252	DATA13	296	DATA47
33	RCLKB1	77	ADDR22	121	TIMEXPC	165	GND	209	LB1CLK	253	DATA14	297	GND
34	DRB1	78	ADDR21	122	TIMEXPD	166	LD1ACK	210	LB1DAT0	254	DATA15	298	$\overline{BR}$1
35	TFSB1	79	ADDR20	123	GND	167	LD1CLK	211	LB1DAT1	255	GND	299	$\overline{BR}$2
36	TCLKB1	80	V_{DD}	124	TDO	168	LD1DAT0	212	LB1DAT2	256	DATA16	300	$\overline{BR}$3
37	DTB1	81	ADDR19	125	$\overline{TRST}$	169	LD1DAT1	213	LB1DAT3	257	DATA17	301	$\overline{BR}$4
38	V_{DD}	82	ADDR18	126	TDI	170	LD1DAT2	214	V_{DD}	258	DATA18	302	$\overline{BR}$5
39	RFSC1	83	ADDR17	127	TMS	171	LD1DAT3	215	LA4ACK	259	DATA19	303	$\overline{BR}$6
40	RCLKC1	84	GND	128	TCK	172	V_{DD}	216	LA4CLK	260	V_{DD}	304	PAGE
41	DRC1	85	ADDR16	129	V_{DD}	173	LC4ACK	217	LA4DAT0	261	DATA20	305	V_{DD}
42	TFSC1	86	ADDR15	130	$\overline{IRQ}$A0	174	LC4CLK	218	LA4DAT1	262	DATA21	306	$\overline{DMAG1}$
43	TCLKC1	87	ADDR14	131	$\overline{IRQ}$A1	175	LC4DAT0	219	LA4DAT2	263	DATA22	307	$\overline{DMAG2}$
44	DTC1	88	V_{DD}	132	$\overline{IRQ}$A2	176	LC4DAT1	220	LA4DAT3	264	DATA23	308	ACK

ORDERING GUIDE

Part Number	Case Temperature Range	SMD	Instruction Rate	Operating Voltage
AD14060BF-4	–40°C to +100°C	N/A	40 MHz	5 V
AD14060LBF-4	–40°C to +100°C	N/A	40 MHz	3.3 V
5962-9750601HXC	–40°C to +100°C	QML-H	40 MHz	5 V
5962-9750701HXC*	–40°C to +100°C	QML-H	40 MHz	3.3 V

*Part numbers marked with an * are shipping as x-grade (preproduction) material at the time of this printing. These parts are packaged in a 308-lead Ceramic Quad Flatpack Package (CQFP). MIL-SMD parts, in the same package, are in development.

PACKAGE DIMENSIONS

Dimensions shown in inches and (mm).

308-Lead Ceramic Quad Flatpack (CQFP)
(QS-308)