



# AC '97 SoundMAX® Codec

## AD1981BL

### FEATURES

#### AC '97 2.3 COMPATIBLE FEATURES

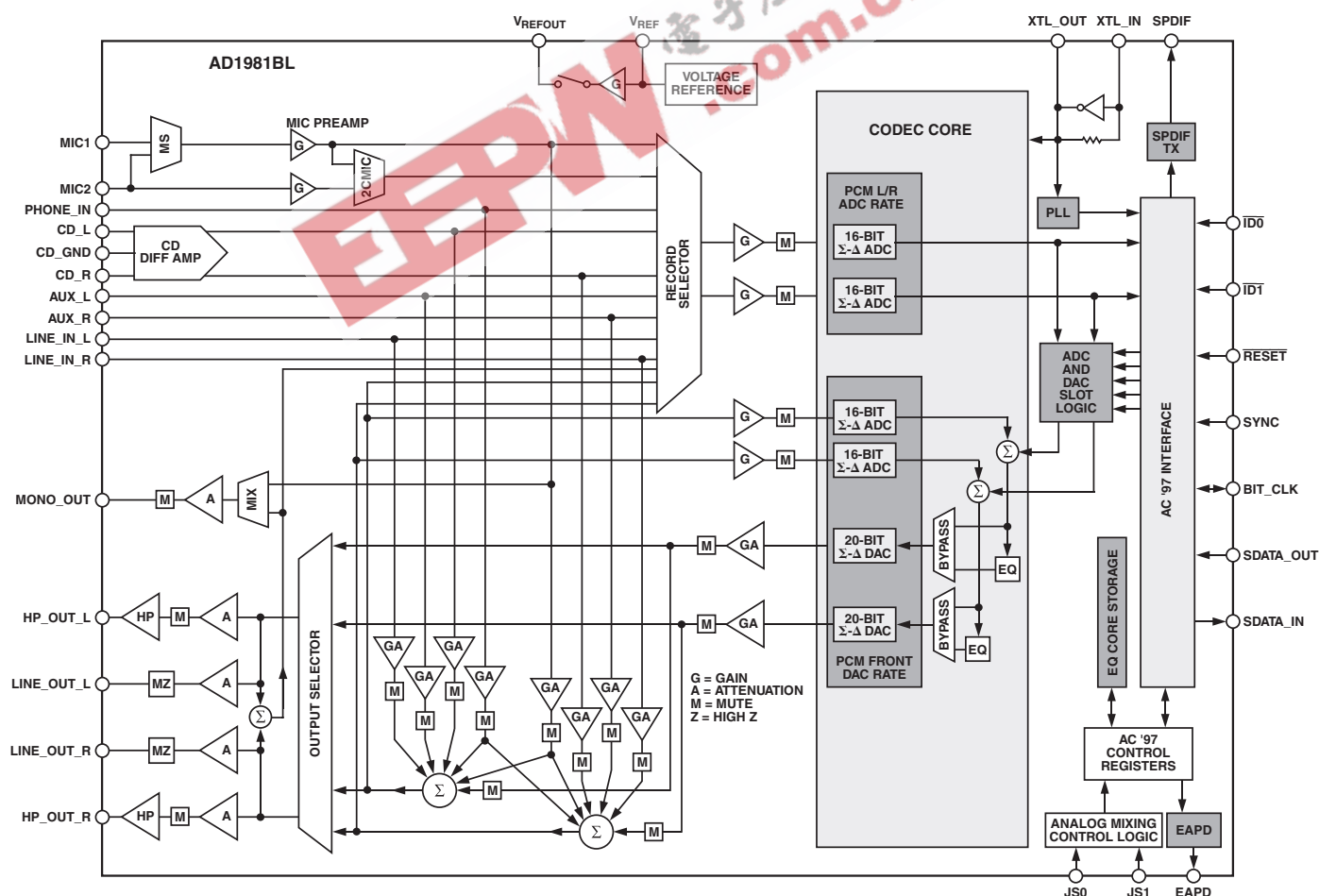
S/PDIF Output, 20 Bits Data Format, Supporting  
48 kHz and 44.1 kHz Sample Rates  
Integrated Stereo Headphone Amplifier  
Variable Sample Rate Audio  
External Audio Power-Down Control  
Greater than 90 dB Dynamic Range  
Stereo Full-Duplex Codec  
20-Bit PCM DAC  
3 Analog Line-Level Stereo Inputs for  
Line-In, AUX, and CD  
Mono Line-Level Phone Input  
Dual MIC Input with Built-In Programmable Preamp  
High Quality CD Input with Ground Sense

Mono Output for Speakerphone or Internal Speaker  
Power Management Support  
48-Lead LQFP Package, Lead-Free Package Available

### ENHANCED FEATURES

Stereo MIC Preamps Support  
Built-In Digital Equalizer Function for Optimized  
Speaker Sound  
Full-Duplex Variable Sample Rates from 7040 Hz to  
48 kHz with 1 Hz Resolution  
Jack Sense Pins Provide Automatic Output Switching  
Software Programmed  $V_{REFOUT}$  Output for Biasing  
Microphone and External Power Amp  
Low Power 3.3 V Operation for Analog and  
Digital Supplies  
Multiple Codec Configuration Options

### FUNCTIONAL BLOCK DIAGRAM



REV. 0

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# AD1981BL—SPECIFICATIONS

## STANDARD TEST CONDITIONS, UNLESS OTHERWISE NOTED

|                         |                 |
|-------------------------|-----------------|
| Temperature             | 25°C            |
| Digital Supply (DVDD)   | 3.3 V           |
| Analog Supply (AVDD)    | 3.3 V           |
| Sample Rate ( $f_s$ )   | 48 kHz          |
| Input Signal            | 1008 Hz         |
| Analog Output Pass Band | 20 Hz to 20 kHz |

## DAC Test Conditions

|                                          |
|------------------------------------------|
| Calibrated                               |
| −3 dB Attenuation Relative to Full Scale |
| 0 dB Input                               |
| 10 k $\Omega$ Output Load (LINE_OUT)     |
| 32 $\Omega$ Output Load (HP_OUT)         |

## ADC Test Conditions

|                                      |
|--------------------------------------|
| Calibrated                           |
| 0 dB Gain                            |
| Input −3.0 dB Relative to Full Scale |

| Parameter                                                                                     | Min              | Typ      | Max              | Unit       |
|-----------------------------------------------------------------------------------------------|------------------|----------|------------------|------------|
| <b>ANALOG INPUT</b>                                                                           |                  |          |                  |            |
| Input Voltage (RMS Values Assume Sine Wave Input)<br>LINE_IN, AUX, CD, PHONE_IN               |                  | 0.707    |                  | V rms      |
|                                                                                               |                  | 2.0      |                  | V p-p      |
| MIC_IN with +20 dB Gain                                                                       |                  | 0.0707   |                  | V rms      |
|                                                                                               |                  | 0.2      |                  | V p-p      |
| MIC_IN with 0 dB Gain                                                                         |                  | 0.707    |                  | V rms      |
|                                                                                               |                  | 2.0      |                  | V p-p      |
| Input Impedance <sup>1</sup>                                                                  |                  | 20       |                  | k $\Omega$ |
| Input Capacitance <sup>1</sup>                                                                |                  | 5        | 7.5              | pF         |
| <b>MASTER VOLUME</b>                                                                          |                  |          |                  |            |
| Step Size (0 dB to −46.5 dB): LINE_OUT_L, LINE_OUT_R                                          |                  | 1.5      |                  | dB         |
| Output Attenuation Range <sup>1</sup>                                                         |                  | 46.5     |                  | dB         |
| Step Size (0 dB to −46.5 dB): MONO_OUT                                                        |                  | 1.5      |                  | dB         |
| Output Attenuation Range <sup>1</sup>                                                         |                  | 46.5     |                  | dB         |
| Step Size (0 dB to −46.5 dB): HP_OUT_R, HP_OUT_L                                              |                  | 1.5      |                  | dB         |
| Output Attenuation Range Span <sup>1</sup>                                                    |                  | 46.5     |                  | dB         |
| Mute Attenuation of 0 dB Fundamental <sup>1</sup>                                             | 80               |          |                  | dB         |
| <b>PROGRAMMABLE GAIN AMPLIFIER—ADC</b>                                                        |                  |          |                  |            |
| Step Size (0 dB to 22.5 dB)                                                                   |                  | 1.5      |                  | dB         |
| PGA Gain Range                                                                                |                  | 22.5     |                  | dB         |
| <b>ANALOG MIXER—INPUT GAIN/AMPLIFIERS/ATTENUATORS</b>                                         |                  |          |                  |            |
| Signal-to-Noise Ratio (SNR)<br>CD to LINE_OUT                                                 |                  | 90       |                  | dB         |
| Other to LINE_OUT <sup>1</sup>                                                                |                  | 90       |                  | dB         |
| Step Size (+12 dB to −34.5 dB) (All Steps Tested):<br>MIC_IN, LINE_IN, CD, AUX, PHONE_IN, DAC |                  | 1.5      |                  | dB         |
| Input Gain/Attenuation Range:<br>MIC_IN, LINE_IN, CD, AUX, PHONE_IN, DAC                      |                  | 46.5     |                  | dB         |
| <b>DIGITAL DECIMATION AND INTERPOLATION FILTERS<sup>1</sup></b>                               |                  |          |                  |            |
| Pass Band                                                                                     | 0                |          | $0.4 \times f_s$ | Hz         |
| Pass-Band Ripple                                                                              |                  |          | $\pm 0.09$       | dB         |
| Transition Band                                                                               | $0.4 \times f_s$ |          | $0.6 \times f_s$ | Hz         |
| Stop Band                                                                                     | $0.6 \times f_s$ |          | $\infty$         | Hz         |
| Stop-Band Rejection                                                                           | −74              |          |                  | dB         |
| Group Delay                                                                                   |                  | $16/f_s$ |                  | sec        |
| Group Delay Variation over Pass Band                                                          |                  | 0        |                  | $\mu$ s    |

| Parameter                                                                                                                       | Min         | Typ          | Max         | Unit           |
|---------------------------------------------------------------------------------------------------------------------------------|-------------|--------------|-------------|----------------|
| ANALOG-TO-DIGITAL CONVERTERS                                                                                                    |             |              |             |                |
| Resolution                                                                                                                      |             | 16           |             | Bits           |
| Total Harmonic Distortion (THD)                                                                                                 |             | −87          |             | dB             |
| Dynamic Range (−60 dB Input THD+N Referenced to Full Scale, A-Weighted)                                                         | 78          | 83           |             | dB             |
| Signal-to-Intermodulation Distortion <sup>1</sup> (CCIF Method)                                                                 |             | 85           |             | dB             |
| ADC Crosstalk <sup>1</sup>                                                                                                      |             |              |             |                |
| Line Inputs (Input L, Ground R, Read R; Input R, Ground L, Read L)                                                              |             | −80          |             | dB             |
| Line_In to Other                                                                                                                |             | −100         | −80         | dB             |
| Gain Error <sup>2</sup> (Full-Scale Span Relative to Nominal Input Voltage)                                                     |             |              | ±10         | %              |
| Interchannel Gain Mismatch (Difference of Gain Errors)                                                                          |             |              | ±0.5        | dB             |
| ADC Offset Error <sup>1</sup>                                                                                                   |             |              | ±5          | mV             |
| DIGITAL-TO-ANALOG CONVERTERS                                                                                                    |             |              |             |                |
| Resolution                                                                                                                      |             | 20           |             | Bits           |
| Total Harmonic Distortion (THD) LINE_OUT                                                                                        |             | −88          |             | dB             |
| Total Harmonic Distortion (THD) HP_OUT                                                                                          |             | −81          |             | dB             |
| Dynamic Range (−60 dB Input THD+N Referenced to Full Scale, A-Weighted)                                                         | 82          | 87.5         |             | dB             |
| Signal-to-Intermodulation Distortion <sup>1</sup> (CCIF Method)                                                                 |             | −100         |             | dB             |
| Gain Error <sup>2</sup> (Output FS Voltage Relative to Nominal Output FS Voltage)                                               |             |              | ±10         | %              |
| Interchannel Gain Mismatch (Difference of Gain Errors)                                                                          |             |              | ±0.7        | dB             |
| DAC Crosstalk <sup>1</sup> (Input L, Zero R, Measure R_OUT; Input R, Zero L, Measure L_OUT)                                     |             |              | −80         | dB             |
| ANALOG OUTPUT                                                                                                                   |             |              |             |                |
| Full-Scale Output Voltage; LINE_OUT and MONO_OUT                                                                                |             | 0.707<br>2.0 |             | V rms<br>V p-p |
| Output Impedance <sup>1</sup>                                                                                                   |             |              | 800         | Ω              |
| External Load Impedance <sup>1</sup>                                                                                            | 10          |              |             | kΩ             |
| Output Capacitance <sup>1</sup>                                                                                                 |             | 15           |             | pF             |
| External Load Capacitance <sup>1</sup>                                                                                          |             |              | 100         | pF             |
| Full-Scale Output Voltage; HP_OUT (0 dB Gain)                                                                                   |             | 1            |             | V rms          |
| External Load Impedance <sup>1</sup>                                                                                            | 32          |              |             | Ω              |
| V <sub>REF</sub>                                                                                                                | 1           | 1.12         | 1.225       | V              |
| V <sub>REF_OUT</sub>                                                                                                            |             | 2.25         |             | V              |
| V <sub>REF_OUT</sub> Current Drive                                                                                              |             |              | 5           | mA             |
| Mute Click (Muted Output Minus Unmuted Midscale DAC Output)                                                                     |             | ±5           |             | mV             |
| STATIC DIGITAL SPECIFICATIONS                                                                                                   |             |              |             |                |
| High Level Input Voltage (V <sub>IH</sub> ): Digital Inputs                                                                     | 0.65 × DVDD |              |             | V              |
| Low Level Input Voltage (V <sub>IL</sub> )                                                                                      |             |              | 0.35 × DVDD | V              |
| High Level Output Voltage (V <sub>OH</sub> ), I <sub>OH</sub> = 2 mA                                                            | 0.9 × DVDD  |              |             | V              |
| Low Level Output Voltage (V <sub>OL</sub> ), I <sub>OL</sub> = 2 mA                                                             |             |              | 0.1 × DVDD  | V              |
| Input Leakage Current                                                                                                           | −10         |              | +10         | μA             |
| Output Leakage Current                                                                                                          | −10         |              | +10         | μA             |
| POWER SUPPLY                                                                                                                    |             |              |             |                |
| Power Supply Range—(AV <sub>DD</sub> and DV <sub>DD</sub> )                                                                     | 3.0         |              | 3.47        | V              |
| Power Dissipation                                                                                                               |             | 287          |             | mW             |
| Analog Supply Current—3.3 V (AV <sub>DD</sub> )                                                                                 |             | 39           |             | mA             |
| Digital Supply Current—3.3 V (DV <sub>DD</sub> )                                                                                |             | 48           |             | mA             |
| Power Supply Rejection (100 mV p-p Signal @ 1 kHz) <sup>1</sup><br>(At Both Analog and Digital Supply Pins, Both ADCs and DACs) |             | 40           |             | dB             |

# AD1981BL

## SPECIFICATIONS (continued)

| Parameter                         | Min | Typ    | Max | Unit |
|-----------------------------------|-----|--------|-----|------|
| CLOCK SPECIFICATIONS <sup>1</sup> |     |        |     |      |
| Input Clock Frequency             |     | 24.576 |     | MHz  |
| Recommended Clock Duty Cycle      | 40  | 50     | 60  | %    |

### NOTES

<sup>1</sup>Guaranteed but not tested.

<sup>2</sup>Measurements reflect main ADC.

Specifications subject to change without notice.

| Parameter          | Set Bits                     | DV <sub>DD</sub> Typ | AV <sub>DD</sub> Typ | Unit |
|--------------------|------------------------------|----------------------|----------------------|------|
| POWER-DOWN STATES* |                              |                      |                      |      |
| (Fully Active)     | (No Bits Value)              | 47.76                | 38.9                 | mA   |
| ADC                | PR0                          | 40.1                 | 34.39                | mA   |
| DAC                | PR1                          | 32.8                 | 26.3                 | mA   |
| ADC + DAC          | PR1, PR0                     | 13.2                 | 20.55                | mA   |
| Mixer              | PR2                          | 47.7                 | 19.39                | mA   |
| ADC + Mixer        | PR2, PR0                     | 40                   | 14.86                | mA   |
| DAC + Mixer        | PR2, PR1                     | 32.77                | 6.39                 | mA   |
| ADC + DAC + Mixer  | PR2, PR1, PR0                | 13.9                 | 1.15                 | mA   |
| Standby            | PR5, PR4, PR3, PR2, PR1, PR0 | 0                    | 0                    | mA   |
| Headphone Standby  | PR6                          | 47.7                 | 32                   | mA   |

\*Values presented with V<sub>REFOUT</sub> not loaded.

Specifications subject to change without notice.

## TIMING PARAMETERS (Guaranteed over Operating Temperature Range)

| Parameter                                                   | Symbol                   | Min   | Typ    | Max   | Unit |
|-------------------------------------------------------------|--------------------------|-------|--------|-------|------|
| RESET Active Low Pulse Width                                | t <sub>RST_LOW</sub>     |       | 1.0    |       | ms   |
| RESET Inactive to BIT_CLK Start-Up Delay                    | t <sub>RST2CLK</sub>     | 162.8 |        |       | ns   |
| SYNC Active High Pulse Width                                | t <sub>SYNC_HIGH</sub>   |       | 1.3    |       | μs   |
| SYNC Low Pulse Width                                        | t <sub>SYNC_LOW</sub>    |       | 19.5   |       | μs   |
| SYNC Inactive to BIT_CLK Start-Up Delay                     | t <sub>SYNC2CLK</sub>    | 162.8 |        |       | ns   |
| BIT_CLK Frequency                                           |                          |       | 12.288 |       | MHz  |
| BIT_CLK Frequency Accuracy                                  |                          |       |        | ±1    | ppm  |
| BIT_CLK Period                                              | t <sub>CLK_PERIOD</sub>  |       | 81.4   |       | ns   |
| BIT_CLK Output Jitter <sup>1, 2, 3</sup>                    |                          |       | 750    | 2000  | ps   |
| BIT_CLK High Pulse Width                                    | t <sub>CLK_HIGH</sub>    | 32.56 | 42     | 48.84 | ns   |
| BIT_CLK Low Pulse Width                                     | t <sub>CLK_LOW</sub>     | 32.56 | 38     |       | ns   |
| SYNC Frequency                                              |                          |       | 48.0   |       | kHz  |
| SYNC Period                                                 | t <sub>SYNC_PERIOD</sub> |       | 20.8   |       | ms   |
| Setup to Falling Edge of BIT_CLK                            | t <sub>SETUP</sub>       | 5     | 2.5    |       | ns   |
| Hold from Falling Edge of BIT_CLK                           | t <sub>HOLD</sub>        | 5     |        |       | ns   |
| BIT_CLK Rise Time                                           | t <sub>RISECLK</sub>     | 2     | 4      | 6     | ns   |
| BIT_CLK Fall Time                                           | t <sub>FALLCLK</sub>     | 2     | 4      | 6     | ns   |
| SYNC Rise Time                                              | t <sub>RISESYNC</sub>    | 2     | 4      | 6     | ns   |
| SYNC Fall Time                                              | t <sub>FALLSYNC</sub>    | 2     | 4      | 6     | ns   |
| SDATA_IN Rise Time                                          | t <sub>RISEDIN</sub>     | 2     | 4      | 6     | ns   |
| SDATA_IN Fall Time                                          | t <sub>FALLDIN</sub>     | 2     | 4      | 6     | ns   |
| SDATA_OUT Rise Time                                         | t <sub>RISEDOUT</sub>    | 2     | 4      | 6     | ns   |
| SDATA_OUT Fall Time                                         | t <sub>FALLDOUT</sub>    | 2     | 4      | 6     | ns   |
| End of Slot 2 to BIT_CLK, SDATA_IN Low                      | t <sub>S2_PDOWN</sub>    | 0     |        | 1.0   | ms   |
| Setup to Trailing Edge of RESET                             |                          |       |        |       |      |
| (Applies to SYNC, SDATA_OUT)                                | t <sub>SETUP2RST</sub>   | 15    |        |       | ns   |
| Rising Edge of RESET to Hi-Z Delay                          | t <sub>OFF</sub>         |       |        | 25    | ns   |
| Propagation Delay                                           |                          |       |        | 15    | ns   |
| RESET Rise Time                                             |                          |       |        | 50    | ns   |
| Output Valid Delay from Rising Edge of BIT_CLK to SDI Valid |                          |       |        | 15    | ns   |

### NOTES

<sup>1</sup>Guaranteed but not tested.

<sup>2</sup>Output jitter is directly dependent on crystal input jitter.

<sup>3</sup>Maximum jitter specification for noncrystal operation only. Crystal operation maximum is much lower.

Specifications subject to change without notice.

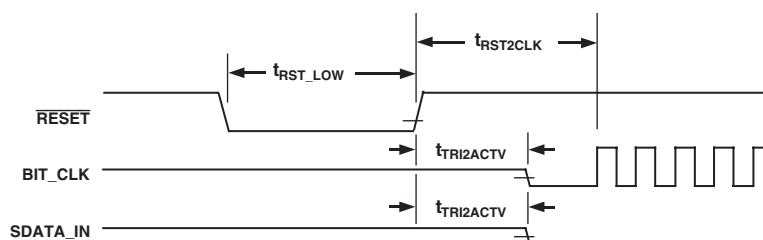


Figure 1. Cold Reset Timing (Codec Is Supplying the BIT\_CLK Signal)

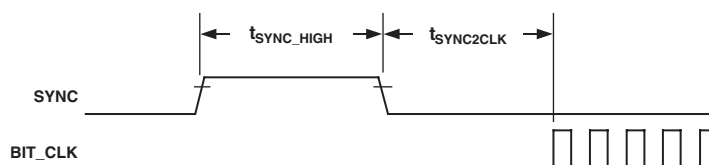


Figure 2. Warm Reset Timing

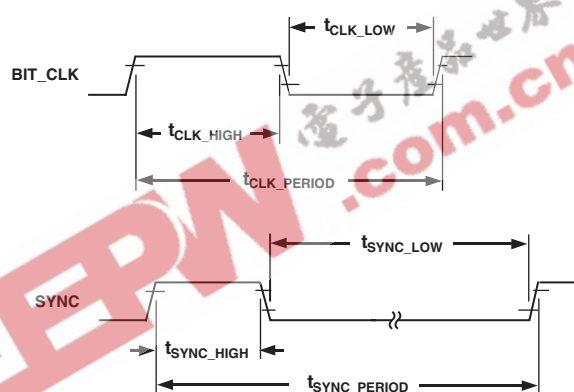


Figure 3. Clock Timing

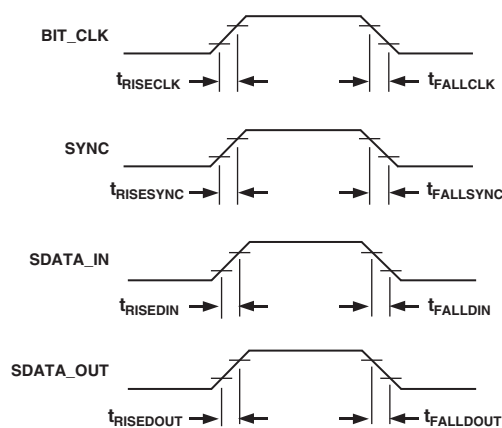


Figure 4. Signal Rise and Fall Times

AD1981BL

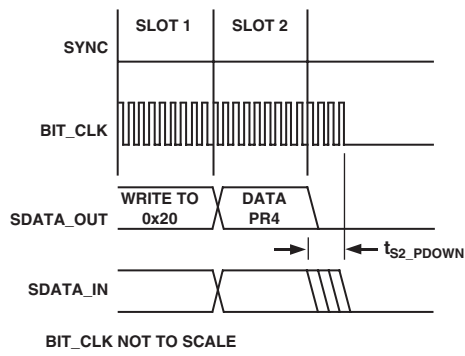


Figure 5. AC-Link Low Power Mode Timing

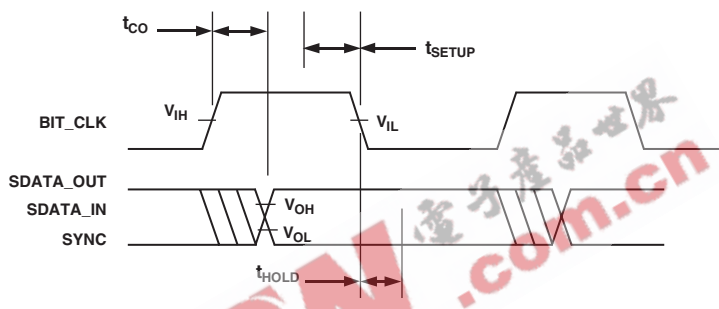


Figure 6. AC-Link Low Power Mode Timing, SYNC and BIT\_CLK Chopped

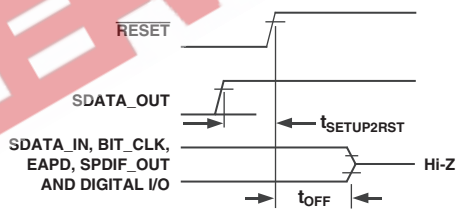


Figure 7. ATE Test Mode

**ABSOLUTE MAXIMUM RATINGS\***(T<sub>A</sub> = 25°C, unless otherwise noted.)**Power Supplies**Digital (DV<sub>DD</sub>) ..... -0.3 V to +3.6 VAnalog (AV<sub>DD</sub>) ..... -0.3 V to +6.0 V

Input Current (Except Supply Pins) ..... ±10 mA

**Signals Pins**Digital Input Voltage ..... -0.3 V to DV<sub>DD</sub> + 0.3 VAnalog Input Voltage ..... -0.3 V to AV<sub>DD</sub> + 0.3 V

Ambient Temperature Range (Operating) ..... 0°C to 70°C

\*Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**ENVIRONMENTAL CONDITIONS\***

Ambient Temperature Rating (LQFP Package)

T<sub>CASE</sub> = Case Temperature in °C

PD = Power Dissipation in W

θ<sub>JA</sub> Thermal Resistance (Junction to Ambient)θ<sub>JC</sub> Thermal Resistance (Junction to Case)

| Package | θ <sub>JA</sub> | θ <sub>JC</sub> |
|---------|-----------------|-----------------|
| LQFP    | 50.1°C/W        | 17.8°C/W        |

\*All measurements per EIA-JESD51 with 2S2P test board per EIA-JESD51-7

**ORDERING GUIDE**

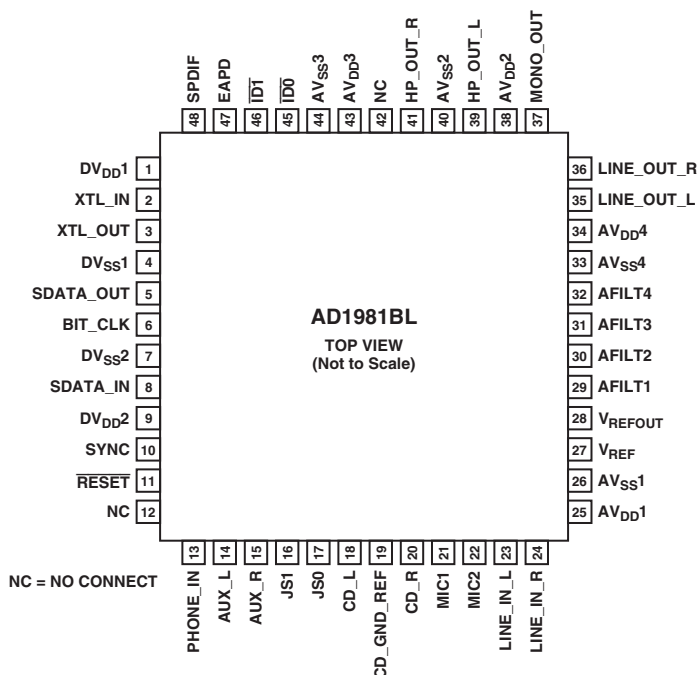
| Model                          | Temperature Range | Package Description | Package Option <sup>1</sup> |
|--------------------------------|-------------------|---------------------|-----------------------------|
| AD1981BLJST                    | 0°C to 70°C       | 48-Lead LQFP (Tray) | ST-48                       |
| AD1981BLJST-REEL               | 0°C to 70°C       | 48-Lead LQFP (Reel) | ST-48                       |
| AD1981BLJSTZ <sup>2</sup>      | 0°C to 70°C       | 48-Lead LQFP (Tray) | ST-48                       |
| AD1981BLJSTZ-REEL <sup>2</sup> | 0°C to 70°C       | 48-Lead LQFP (Reel) | ST-48                       |

**NOTES**<sup>1</sup>ST = Low Profile Quad Flatpack.

<sup>2</sup>The AD1981BLJSTZ is a lead-free environmentally friendly product. It is manufactured using the most up-to-date materials and processes. The coating on the leads of each device is 100% pure tin electroplate. The device is suitable for lead-free applications and is able to withstand surface-mount soldering at up to 255 °C (±5°C). In addition, it is backward compatible with conventional tin-lead soldering processes. This means that the electroplated tin coating can be soldered with tin-lead solder pastes at reflow temperatures of 220°C to 235°C.

**CAUTION**

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD1981BL features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

**PIN CONFIGURATION****48-Lead LQFP**



# AD1981BL

## PIN FUNCTION DESCRIPTIONS

| Pin No.                                                                                        | Mnemonic                 | I/O | Function                                                                                               |
|------------------------------------------------------------------------------------------------|--------------------------|-----|--------------------------------------------------------------------------------------------------------|
| DIGITAL I/O                                                                                    |                          |     |                                                                                                        |
| 2                                                                                              | XTL_IN                   | I   | Crystal Input (24.576 MHz) or External Clock Input.                                                    |
| 3                                                                                              | XTL_OUT                  | O   | Crystal Output.                                                                                        |
| 5                                                                                              | SDATA_OUT                | I   | AC-Link Serial Data Output, AD1981BL Data Input Stream.                                                |
| 6                                                                                              | BIT_CLK                  | O/I | AC-Link Bit Clock Output (12.288 MHz) or Bit Clock Input if Secondary Mode Selected.                   |
| 8                                                                                              | SDATA_IN                 | O   | AC-Link Serial Data Input, AD1981BL Data Output Stream.                                                |
| 10                                                                                             | SYNC                     | I   | AC-Link Frame Sync.                                                                                    |
| 11                                                                                             | RESET                    | I   | AC-Link Reset, AD1981BL Master Hardware Reset.                                                         |
| 48                                                                                             | SPDIF                    | O   | S/PDIF Output.                                                                                         |
| CHIP SELECTS (These pins can also be used to select an external clock. See Table IX.)          |                          |     |                                                                                                        |
| 45                                                                                             | $\overline{\text{ID}}_0$ | I   | Chip Select Input 0 (Active Low). This pin can also be used as the chain input from a secondary codec. |
| 46                                                                                             | $\overline{\text{ID}}_1$ | I   | Chip Select Input 1 (Active Low).                                                                      |
| JACK SENSE AND EAPD                                                                            |                          |     |                                                                                                        |
| 17                                                                                             | JS0                      | I   | Jack Sense 0 Input.                                                                                    |
| 16                                                                                             | JS1                      | I   | Jack Sense 1 Input.                                                                                    |
| 47                                                                                             | EAPD                     | O   | External Amp Power-Down Control.                                                                       |
| ANALOG I/O                                                                                     |                          |     |                                                                                                        |
| 13                                                                                             | PHONE_IN                 | I   | Phone Input. Mono input from telephony subsystem speaker phone or handset.                             |
| 14                                                                                             | AUX_L                    | I   | Auxiliary Input Left Channel.                                                                          |
| 15                                                                                             | AUX_R                    | I   | Auxiliary Input Right Channel.                                                                         |
| 18                                                                                             | CD_L                     | I   | CD Audio Left Channel.                                                                                 |
| 19                                                                                             | CD_GND_REF               | I   | CD Audio Analog Ground Reference for Differential CD Input.                                            |
| 20                                                                                             | CD_R                     | I   | CD Audio Right Channel.                                                                                |
| 21                                                                                             | MIC1                     | I   | Microphone 1 Input (Mono) or Left Channel when 2-Channel Mode Selected (Stereo MIC).                   |
| 22                                                                                             | MIC2                     | I   | Microphone 2 Input (Mono) or Right Channel when 2-Channel Mode Selected (Stereo MIC).                  |
| 23                                                                                             | LINE_IN_L                | I   | Line In Left Channel.                                                                                  |
| 24                                                                                             | LINE_IN_R                | I   | Line In Right Channel.                                                                                 |
| 35                                                                                             | LINE_OUT_L               | O   | Line Out (Front) Left Channel.                                                                         |
| 36                                                                                             | LINE_OUT_R               | O   | Line Out (Front) Right Channel.                                                                        |
| 37                                                                                             | MONO_OUT                 | O   | Monaural Output to Telephony Subsystem Speakerphone.                                                   |
| 39                                                                                             | HP_OUT_L                 | O   | Headphone Left Channel Output.                                                                         |
| 41                                                                                             | HP_OUT_R                 | O   | Headphone Right Channel Output.                                                                        |
| FILTER/REFERENCE (These signals are connected to resistors, capacitors, or specific voltages.) |                          |     |                                                                                                        |
| 27                                                                                             | V <sub>REF</sub>         | O   | Voltage Reference Filter.                                                                              |
| 28                                                                                             | V <sub>REFOUT</sub>      | O   | Voltage Reference Output 5 mA Drive (Intended for MIC Bias and Power Amp Bias).                        |
| 29                                                                                             | AFILT1                   | O   | Antialiasing Filter Capacitor—ADC Right Channel.                                                       |
| 30                                                                                             | AFILT2                   | O   | Antialiasing Filter Capacitor—ADC Left Channel.                                                        |
| 31                                                                                             | AFILT3                   | O   | Antialiasing Filter Capacitor—Mixer ADC Right Channel.                                                 |
| 32                                                                                             | AFILT4                   | O   | Antialiasing Filter Capacitor—Mixer ADC Left Channel.                                                  |
| POWER AND GROUND SIGNALS                                                                       |                          |     |                                                                                                        |
| 1                                                                                              | DV <sub>DD</sub> 1       | I   | Digital V <sub>DD</sub> 3.3 V.                                                                         |
| 4                                                                                              | DV <sub>SS</sub> 1       | I   | Digital GND.                                                                                           |
| 7                                                                                              | DV <sub>SS</sub> 2       | I   | Digital GND.                                                                                           |
| 9                                                                                              | DV <sub>DD</sub> 2       | I   | Digital V <sub>DD</sub> 3.3 V.                                                                         |
| 25                                                                                             | AV <sub>DD</sub> 1       | I   | Analog V <sub>DD</sub> 5.0 V.                                                                          |
| 26                                                                                             | AV <sub>SS</sub> 1       | I   | Analog GND.                                                                                            |
| 38                                                                                             | AV <sub>DD</sub> 2       | I   | Analog V <sub>DD</sub> 5.0 V.                                                                          |
| 40                                                                                             | AV <sub>SS</sub> 2       | I   | Analog GND.                                                                                            |
| 43                                                                                             | AV <sub>DD</sub> 3       | I   | Analog V <sub>DD</sub> 5.0 V.                                                                          |
| 44                                                                                             | AV <sub>SS</sub> 3       | I   | Analog GND.                                                                                            |
| 34                                                                                             | AV <sub>DD</sub> 4       | I   | Analog V <sub>DD</sub> 5.0 V.                                                                          |
| 33                                                                                             | AV <sub>SS</sub> 4       | I   | Analog GND.                                                                                            |
| NO CONNECTS                                                                                    |                          |     |                                                                                                        |
| 12                                                                                             | NC                       |     | No Connect.                                                                                            |
| 42                                                                                             | NC                       |     | No Connect.                                                                                            |



## Indexed Control Registers

| Reg | Name                   | D15     | D14      | D13    | D12    | D11    | D10    | D9      | D8      | D7      | D6      | D5     | D4     | D3     | D2     | D1      | D0      | Default |
|-----|------------------------|---------|----------|--------|--------|--------|--------|---------|---------|---------|---------|--------|--------|--------|--------|---------|---------|---------|
| 00h | Reset                  | X       | SE4      | SE3    | SE2    | SE1    | SE0    | ID9     | ID8     | ID7     | ID6     | ID5    | ID4    | ID3    | ID2    | ID1     | ID0     | 0090h   |
| 02h | Master Volume          | MM      | X        | X      | LMV4   | LMV3   | LMV2   | LMV1    | LMV0    | RM*     | X       | X      | RMV4   | RMV3   | RMV2   | RMV1    | RMV0    | 8000h   |
| 04h | Headphones Volume      | HPM     | X        | X      | LHV4   | LHV3   | LHV2   | LHV1    | LHV0    | RM*     | X       | X      | RHV4   | RHV3   | RHV2   | RHV1    | RHV0    | 8000h   |
| 06h | Mono Volume            | MVM     | X        | X      | X      | X      | X      | X       | X       | X       | X       | X      | MV4    | MV3    | MV2    | MV1     | MV0     | 8000h   |
| 0Ch | Phone Volume           | PHM     | X        | X      | X      | X      | X      | X       | X       | X       | X       | X      | PHV4   | PHV3   | PHV2   | PHV1    | PHV0    | 8008h   |
| 0Eh | MIC Volume             | MCM     | X        | X      | X      | X      | X      | X       | X       | X       | M20     | X      | MCV4   | MCV3   | MCV2   | MCV1    | MCV0    | 8008h   |
| 10h | Line-In Volume         | LVM     | X        | X      | LLV4   | LLV3   | LLV2   | LLV1    | LLV0    | RM*     | X       | X      | RLV4   | RLV3   | RLV2   | RLV1    | RLV0    | 8808h   |
| 12h | CD Volume              | CVM     | X        | X      | LCV4   | LCV3   | LCV2   | LCV1    | LCV0    | RM*     | X       | X      | RCV4   | RCV3   | RCV2   | RCV1    | RCV0    | 8808h   |
| 16h | AUX Volume             | AM      | X        | X      | LAV4   | LAV3   | LAV2   | LAV1    | LAV0    | RM*     | X       | X      | RAV4   | RAV3   | RAV2   | RAV1    | RAV0    | 8808h   |
| 18h | PCM-Out Vol            | OM      | X        | X      | LOV4   | LOV3   | LOV2   | LOV1    | LOV0    | RM*     | X       | X      | ROV4   | ROV3   | ROV2   | ROV1    | ROV0    | 8808h   |
| 1Ah | Record Select          | X       | X        | X      | X      | X      | LS2    | LS1     | LS0     | X       | X       | X      | X      | X      | RS2    | RS1     | RS0     | 0000h   |
| 1Ch | Record Gain            | IM      | X        | X      | X      | LIM3   | LIM2   | LIM1    | LIM0    | RM*     | X       | X      | X      | RIM3   | RIM2   | RIM1    | RIM0    | 8000h   |
| 20h | General-Purpose        | X       | X        | X      | X      | X      | X      | MIX     | MS      | LPBK    | X       | X      | X      | X      | X      | X       | X       | 0000h   |
| 26h | Power-Down Ctrl/Stat   | EAPD    | PR6      | PR5    | PR4    | PR3    | PR2    | PR1     | PR0     | X       | X       | X      | X      | REF    | ANL    | DAC     | ADC     | 000Xh   |
| 28h | Ext'd Audio ID         | IDC1    | IDC0     | X      | X      | REVC1  | REVC0  | AMAP    | X       | X       | X       | DSA1   | DSA0   | X      | SPDIF  | X       | VRAS    | X605h   |
| 2Ah | Ext'd Audio Stat/ Ctrl | VFORCE  | X        | X      | X      | X      | SPCV   | X       | X       | X       | X       | SPSA1  | SPSA0  | X      | SPDIF  | X       | VRA     | 0000h   |
| 2Ch | PCM Front DAC Rate     | SRF15   | SRF14    | SRF13  | SRF12  | SRF11  | SRF10  | SRF9    | SRF8    | SRF7    | SRF6    | SRF5   | SRF4   | SRF3   | SRF2   | SRF1    | SRF0    | BB80h   |
| 32h | PCM L/R ADC Rate       | SRA15   | SRA14    | SRA13  | SRA12  | SRA11  | SRA10  | SRA9    | SRA8    | SRA7    | SRA6    | SRA5   | SRA4   | SRA3   | SRA2   | SRA1    | SRA0    | BB80h   |
| 3Ah | SPDIF Control          | V       | X        | SPSR1  | SPSR0  | L      | CC6    | CC5     | CC4     | CC3     | CC2     | CC1    | CC0    | PRE    | COPY   | /AUD    | PRO     | 2000h   |
| 60h | EQ CTRL                | EQM     | MAD LBEN | X      | X      | X      | X      | X       | X       | SYM     | CHS     | BCA5   | BCA4   | BCA3   | BCA2   | BCA1    | BCA0    | 8080h   |
| 62h | EQ DATA                | CFD15   | CFD14    | CFD13  | CFD12  | CFD11  | CFD10  | CFD9    | CFD8    | CFD7    | CFD6    | CFD5   | CFD4   | CFD3   | CFD2   | CFD1    | CFD0    | 0000h   |
| 64h | Mixer ADC, Volume      | MXM     | X        | X      | X      | LMG3   | LMG2   | LMG1    | LMG0    | RM*     | X       | X      | X      | RMG3   | RMG2   | RMG1    | RMG0    | 8000h   |
| 72h | Jack Sense             | X       | X        | X      | JS MT2 | JS MT1 | JS MT0 | JS1 EQB | JS0 EQB | JS1 TMR | JS0 TMR | JS1 MD | JS0 MD | JS1 ST | JS0 ST | JS1 INT | JS0 INT | 0000h   |
| 74h | Serial Configuration   | SLOT 16 | REGM 2   | REGM 1 | REGM 0 | X      | X      | X       | CHEN    | X       | X       | X      | INTS   | X      | SPAL   | SPDZ    | SPLNK   | 7001h   |
| 76h | Misc Control Bits      | DACZ    | X        | M SPLT | LODIS  | DAM    | X      | FMXE    | X       | MAD PD  | 2CMIC   | X      | MAD ST | VREF H | VREF D | MBG1    | MBG0    | 0000h   |
| 7Ch | Vendor ID1             | F7      | F6       | F5     | F4     | F3     | F2     | F1      | F0      | S7      | S6      | S5     | S4     | S3     | S2     | S1      | S0      | 4144h   |
| 7Eh | Vendor ID2             | T7      | T6       | T5     | T4     | T3     | T2     | T1      | T0      | REV7    | REV6    | REV5   | REV4   | REV3   | REV2   | REV1    | REV0    | 5374h   |

## NOTES

All registers not shown. Bits containing an X are assumed to be reserved.

Odd register addresses are aliased to the next lower even address.

Reserved registers should not be written.

Zeros should be written to reserved bits.

\*For AC '97 compatibility, Bit D7 (RM) is available only by setting the MSPLT bit, Register 76h. The MSPLT bit enables separate mute bits for the left and right channels. If MSPLT is not set, RM bit has no effect.

# AD1981BL

**Reset Register (Index 00h)**

| Reg No. | Name  | D15 | D14 | D13 | D12 | D11 | D10 | D9  | D8  | D7  | D6  | D5  | D4  | D3  | D2  | D1  | D0  | Default |
|---------|-------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|---------|
| 00h     | Reset | X   | SE4 | SE3 | SE2 | SE1 | SE0 | ID9 | ID8 | ID7 | ID6 | ID5 | ID4 | ID3 | ID2 | ID1 | ID0 | 0090h   |

## NOTES

X in the above table is a wild card and has no effect on the value.

Writing any value to this register performs a register reset that causes all registers to revert to their default values (except 74h, which forces the serial configuration).

Reading this register returns the ID code of the part and a code for the type of 3D stereo enhancement.

ID[9:0] Identify Capability. The ID decodes the capabilities of AD1981BL based on the following:

| Bit | Function                          | AD1981BL |
|-----|-----------------------------------|----------|
| ID0 | Dedicated Mic PCM In Channel      | 0        |
| ID1 | Modem Line Codec Support          | 0        |
| ID2 | Bass and Treble Control           | 0        |
| ID3 | Simulated Stereo (Mono to Stereo) | 0        |
| ID4 | Headphone Out Support             | 1        |
| ID5 | Loudness (Bass Boost) Support     | 0        |
| ID6 | 18-Bit DAC Resolution             | 0        |
| ID7 | 20-Bit DAC Resolution             | 1        |
| ID8 | 18-Bit ADC Resolution             | 0        |
| ID9 | 20-Bit ADC Resolution             | 0        |

SE[4:0] Stereo Enhancement. The AD1981BL does not provide hardware 3D stereo enhancement (all bits are zeros).

**Master Volume Register (Index 02h)**

| Reg No. | Name          | D15 | D14 | D13 | D12  | D11  | D10  | D9   | D8   | D7  | D6 | D5 | D4   | D3   | D2   | D1   | D0   | Default |
|---------|---------------|-----|-----|-----|------|------|------|------|------|-----|----|----|------|------|------|------|------|---------|
| 02h     | Master Volume | MM  | X   | X   | LMV4 | LMV3 | LMV2 | LMV1 | LMV0 | RM* | X  | X  | RMV4 | RMV3 | RMV2 | RMV1 | RMV0 | 8000h   |

\* For AC '97 compatibility, Bit D7 (RM) is available only by setting the MSPLT bit, Register 76h. The MSPLT bit enables separate mute bits for the left and right channels. If MSPLT is not set, RM bit has no effect. All registers not shown and bits containing an X are assumed to be reserved.

Refer to Table I for examples. This register controls the Line\_Out volume controls for both stereo channels and the mute bit. Each volume subregister contains five bits, generating 32 volume levels with 31 steps of 1.5 dB each. Because AC '97 defines 6-bit volume registers, to maintain compatibility whenever the D5 or D13 bits are set to 1, their respective lower five volume bits are automatically set to 1 by the codec logic. On readback, all lower five bits will read 1s whenever these bits are set to 1.

|          |                                                                                                                                                                                                               |
|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RMV[4:0] | Right Master Volume Control. The least significant bit represents 1.5 dB. This register controls the output from 0 dB to a maximum attenuation of 46.5 dB.                                                    |
| RM       | Right Channel Mute. Once enabled by the MSPLT bit in Register 76h, this bit mutes the right channel separately from the MM bit. Otherwise, this bit will always read 0 and will have no effect when set to 1. |
| LMV[4:0] | Left Master Volume Control. The least significant bit represents 1.5 dB. This register controls the output from 0 dB to a maximum attenuation of 46.5 dB.                                                     |
| MM       | Master Volume Mute. When this bit is set to 1, both the left and right channels are muted, unless the MSPLT bit in Register 76h is set to 1, in which case this mute bit will affect only the left channel.   |

Headphones Volume Register (Index 04h)

| Reg No. | Name             | D15 | D14 | D13 | D12   | D11   | D10   | D9    | D8    | D7  | D6 | D5 | D4    | D3    | D2    | D1    | D0    | Default |
|---------|------------------|-----|-----|-----|-------|-------|-------|-------|-------|-----|----|----|-------|-------|-------|-------|-------|---------|
| 04h     | Headphone Volume | HPM | X   | X   | LHV 4 | LHV 3 | LHV 2 | LHV 1 | LHV 0 | RM* | X  | X  | RHV 4 | RHV 3 | RHV 2 | RHV 1 | RHV 0 | 8000h   |

\*For AC '97 compatibility, Bit D7 (RM) is available only by setting the MSPLT bit, Register 76h. The MSPLT bit enables separate mute bits for the left and right channels. If MSPLT is not set, RM bit has no effect. All registers not shown, and bits containing an X are assumed to be reserved.

Refer to Table I for examples. This register controls the headphone volume controls for both stereo channels and mute bit. Each volume subregister contains five bits, generating 32 volume levels with 31 steps of 1.5 dB each. Because AC '97 defines 6-bit volume registers, to maintain compatibility, whenever the D5 or D13 bits are set to 1, their respective lower five volume bits are automatically set to 1 by the codec logic. On readback, all lower five bits will read 1s whenever these bits are set to 1.

|           |                                                                                                                                                                                                                 |
|-----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RHV [4:0] | Right Headphone Volume Control. The least significant bit represents 1.5 dB. This register controls the output from 0 dB to a maximum attenuation of 46.5 dB.                                                   |
| RM        | Right Channel Mute. Once enabled by the MSPLT bit in Register 76h, this bit mutes the right channel separately from the HPM bit. Otherwise, this bit will always read 0 and will have no effect when set to 1.  |
| LHV [4:0] | Left Headphone Volume Control. The least significant bit represents 1.5 dB. This register controls the output from 0 dB to a maximum attenuation of 46.5 dB.                                                    |
| HPM       | Headphones Volume Mute. When this bit is set to 1, both the left and right channels are muted, unless the MSPLT bit in Register 76h is set to 1, in which case this mute bit will affect only the left channel. |

Table I. Volume Settings for Master and Headphone

| Reg. 76h | Control Bits                                   |         |          |                             |                             |         |          |                              |
|----------|------------------------------------------------|---------|----------|-----------------------------|-----------------------------|---------|----------|------------------------------|
|          | Master Volume (02h) and Headphone Volume (04h) |         |          |                             |                             |         |          |                              |
|          | Left Channel Volume D[13:8]                    |         |          |                             | Right Channel Volume D[5:0] |         |          |                              |
| MSPLT*   | D15                                            | Write   | Readback | Function                    | D7*                         | Write   | Readback | Function                     |
| 0        | 0                                              | 00 0000 | 00 0000  | 0 dB Gain                   | x                           | 00 0000 | 00 0000  | 0 dB Gain                    |
| 0        | 0                                              | 00 1111 | 00 1111  | -22.5 dB Gain               | x                           | 00 1111 | 00 1111  | -22.5 dB Gain                |
| 0        | 0                                              | 01 1111 | 01 1111  | -46.5 dB Gain               | x                           | 01 1111 | 01 1111  | -46.5 dB Gain                |
| 0        | 0                                              | 1x xxxx | 01 1111  | -46.5 dB Gain               | x                           | 1x xxxx | 01 1111  | -46.5 dB Gain                |
| 0        | 1                                              | xx xxxx | xx xxxx  | -∞ dB Gain, Muted           | x                           | xx xxxx | xx xxxx  | -∞ dB Gain, Muted            |
| 1        | 0                                              | 1x xxxx | 01 1111  | -46.5 dB Gain               | 1                           | xx xxxx | xx xxxx  | -∞ dB Gain, Right Only Muted |
| 1        | 1                                              | xx xxxx | xx xxxx  | -∞ dB Gain, Left Only Muted | 0                           | xx xxxx | xx xxxx  | -46.5 dB Gain                |
| 1        | 1                                              | xx xxxx | xx xxxx  | -∞ dB Gain, Left Muted      | 1                           | xx xxxx | xx xxxx  | -∞ dB Gain, Right Muted      |

\*For AC '97 compatibility, Bit D7 (RM) is available only by setting the MSPLT bit, Register 76h. The MSPLT bit enables separate mute bits for the left and right channels. If MSPLT is not set, RM bit has no effect.

x in the above table is a wild card and has no effect on the value.

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**Mono Volume Register (Index 06h)**

| Reg No. | Name        | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4  | D3  | D2  | D1  | D0  | Default |
|---------|-------------|-----|-----|-----|-----|-----|-----|----|----|----|----|----|-----|-----|-----|-----|-----|---------|
| 06h     | Mono Volume | MVM | X   | X   | X   | X   | X   | X  | X  | X  | X  | X  | MV4 | MV3 | MV2 | MV1 | MV0 | 8000h   |

All registers not shown and bits containing an X are assumed to be reserved.

Refer to Table II for examples. This register controls the mono output volume and mute bit. The volume register contains five bits, generating 32 volume levels with 31 steps of 1.5 dB each. Because AC '97 defines 6-bit volume registers, to maintain compatibility, whenever the D5 bit is set to 1, their respective lower five volume bits are automatically set to 1 by the codec logic. On readback, all lower five bits will read 1s whenever this bit is set to 1.

|         |                                                                                                                                                    |
|---------|----------------------------------------------------------------------------------------------------------------------------------------------------|
| MV[4:0] | Mono Volume Control. The least significant bit represents 1.5 dB. This register controls the output from 0 dB to a maximum attenuation of 46.5 dB. |
| MVM     | Mono Volume Mute. When this bit is set to 1, the channel is muted.                                                                                 |

**Table II. Volume Settings for Mono**

| D15 | Control Bits D[4:0] for Mono (06h) |          | Function          |
|-----|------------------------------------|----------|-------------------|
|     | WRITE                              | READBACK |                   |
| 0   | 0000                               | 0 0000   | 0 dB Gain         |
| 0   | 0 1111                             | 0 1111   | -22.5 dB Gain     |
| 0   | 1 1111                             | 1 1111   | -46.5 dB Gain     |
| 1   | x xxxx                             | x xxxx   | -∞ dB Gain, Muted |

x in the above table is a wild card and has no effect on the value.

**Phone Volume Register (Index 0Ch)**

| Reg No. | Name         | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4   | D3   | D2   | D1   | D0   | Default |
|---------|--------------|-----|-----|-----|-----|-----|-----|----|----|----|----|----|------|------|------|------|------|---------|
| 0Ch     | Phone Volume | PHM | X   | X   | X   | X   | X   | X  | X  | X  | X  | X  | PHV4 | PHV3 | PHV2 | PHV1 | PHV0 | 8008h   |

All registers not shown and bits containing an X are assumed to be reserved. Refer to Table III for examples.

|          |                                                                                                                                                                                                                                       |
|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PHV[4:0] | Phone Volume. Allows setting the phone volume attenuator in 32 volume levels with 31 steps of 1.5 dB each. The LSB represents 1.5 dB, and the gain range is +12 dB to -34.5 dB. The default value is 0 dB, with the mute bit enabled. |
| PHM      | Phone Mute. When this bit is set to 1, the phone channel is muted.                                                                                                                                                                    |

All registers not shown and bits containing an X are assumed to be reserved. Refer to Table III for examples.

**MIC Volume Register (Index 0Eh)**

| Reg No. | Name       | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6  | D5 | D4   | D3   | D2   | D1   | D0   | Default |
|---------|------------|-----|-----|-----|-----|-----|-----|----|----|----|-----|----|------|------|------|------|------|---------|
| 0Eh     | MIC Volume | MCM | X   | X   | X   | X   | X   | X  | X  | X  | M20 | X  | MCV4 | MCV3 | MCV2 | MCV1 | MCV0 | 8008h   |

All registers not shown and bits containing an X are assumed to be reserved. Refer to Table III for examples.

|          |                                                                                                                                                                                                                                                                                                                                                                                                     |
|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| MCV[4:0] | MIC Volume Gain. Allows setting the phone volume attenuator in 32 volume levels with 31 steps of 1.5 dB each. The LSB represents 1.5 dB, and the gain range is +12 dB to -34.5 dB. The default value is 0 dB, with the mute bit enabled.                                                                                                                                                            |
| M20      | MIC Gain Boost. This bit allows setting additional MIC gain to increase the microphone sensitivity. The nominal gain boost by default is 20 dB; however, Bits D0 and D1 (MBG[1:0]) on the miscellaneous control bits register (76h) allow changing the gain boost to 10 dB or 30 dB if necessary.<br>0 = Disabled; Gain = 0 dB<br>1 = Enabled; Default Gain = 20 dB (see Register 76h, Bits D0, D1) |
| MCM      | MIC Mute. When this bit is set to 1, the MIC channel is muted.                                                                                                                                                                                                                                                                                                                                      |

Table III. Volume Settings for Phone and MIC

| D15 | Control Bits D[4:0]<br>Phone (0Ch) and MIC (0Eh) |          | Function          |
|-----|--------------------------------------------------|----------|-------------------|
|     | WRITE                                            | READBACK |                   |
| 0   | 0 0000                                           | 0 0000   | 12 dB Gain        |
| 0   | 0 1000                                           | 0 1000   | 0 dB Gain         |
| 0   | 1 1111                                           | 1 1111   | -34.5 dB Gain     |
| 1   | x xxxx                                           | x xxxx   | -∞ dB Gain, Muted |

x in the above table is a wild card, and has no effect on the value.

Line-In Volume Register (Index 10h)

| Reg No. | Name           | D15 | D14 | D13 | D12  | D11  | D10  | D9   | D8   | D7  | D6 | D5 | D4   | D3   | D2   | D1   | D0   | Default |
|---------|----------------|-----|-----|-----|------|------|------|------|------|-----|----|----|------|------|------|------|------|---------|
| 10h     | Line-In Volume | LVM | X   | X   | LLV4 | LLV3 | LLV2 | LLV1 | LLV0 | RM* | X  | X  | RLV4 | RLV3 | RLV2 | RLV1 | RLV0 | 8808h   |

\*For AC '97 compatibility, Bit D7 (RM) is available only by setting the MSPLT bit, Register 76h. The MSPLT bit enables separate mute bits for the left and right channels. If MSPLT is not set, the RM bit has no effect. All registers not shown, and bits containing an X are assumed to be reserved. Refer to Table IV for examples.

|          |                                                                                                                                                                                                               |
|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RLV[4:0] | Line-In Volume Right. Allows setting the line-in right channel attenuator in 32 volume levels. The LSB represents 1.5 dB, and the range is +12 dB to -34.5 dB. The default value is 0 dB, mute enabled.       |
| RM       | Right Channel Mute. Once enabled by the MSPLT bit in Register 76h, this bit mutes the right channel separately from the LM bit. Otherwise, this bit will always read 0 and will have no effect when set to 1. |
| LLV[4:0] | Line-In Volume Left. Allows setting the line in left channel attenuator in 32 volume levels. The LSB represents 1.5 dB, and the range is +12 dB to -34.5 dB. The default value is 0 dB, mute enabled.         |
| LVM      | Line-In Mute. When this bit is set to 1, both the left and right channels are muted unless the MSPLT bit in Register 76h is set to 1, in which case this mute bit will affect only the left channel.          |

CD Volume Register (Index 12h)

| Reg No. | Name      | D15 | D14 | D13 | D12  | D11  | D10  | D9   | D8   | D7  | D6 | D5 | D4   | D3   | D2   | D1   | D0   | Default |
|---------|-----------|-----|-----|-----|------|------|------|------|------|-----|----|----|------|------|------|------|------|---------|
| 12h     | CD Volume | CVM | X   | X   | LCV4 | LCV3 | LCV2 | LCV1 | LCV0 | RM* | X  | X  | RCV4 | RCV3 | RCV2 | RCV1 | RCV0 | 8808h   |

\*For AC '97 compatibility, Bit D7 (RM) is only available by setting the MSPLT bit, Register 76h. The MSPLT bit enables separate mute bits for the left and right channels. If MSPLT is not set, the RM bit has no effect. All registers not shown, and bits containing an X are assumed to be reserved. Refer to Table IV for examples.

|          |                                                                                                                                                                                                                |
|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RCV[4:0] | Right CD Volume. Allows setting the CD right channel attenuator in 32 volume levels. The LSB represents 1.5 dB, and the gain range is +12 dB to -34.5 dB. The default value is 0 dB, mute enabled.             |
| RM       | Right Channel Mute. Once enabled by the MSPLT bit in Register 76h, this bit mutes the right channel separately from the CVM bit. Otherwise, this bit will always read 0 and will have no affect when set to 1. |
| LCV[4:0] | Left CD Volume. Allows setting the CD left channel attenuator in 32 volume levels. The LSB represents 1.5 dB, and the gain range is +12 dB to -34.5 dB. The default value is 0 dB, mute enabled.               |
| CVM      | CD Volume Mute. When this bit is set to 1, both the left and right channels are muted, unless the MSPLT bit in Register 76h is set to 1, in which case this mute bit will affect only the left channel.        |

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**AUX Volume Register (Index 16h)**

| Reg No. | Name       | D15 | D14 | D13 | D12  | D11  | D10  | D9   | D8   | D7  | D6 | D5 | D4   | D3   | D2   | D1   | D0   | Default |
|---------|------------|-----|-----|-----|------|------|------|------|------|-----|----|----|------|------|------|------|------|---------|
| 16h     | AUX Volume | AM  | X   | X   | LAV4 | LAV3 | LAV2 | LAV1 | LAV0 | RM* | X  | X  | RAV4 | RAV3 | RAV2 | RAV1 | RAV0 | 8808h   |

\*For AC '97 compatibility, Bit D7 (RM) is available only by setting the MSPLT bit, Register 76h. The MSPLT bit enables separate mute bits for the left and right channels. If MSPLT is not set, RM bit has no effect. All registers not shown, and bits containing an X are assumed to be reserved. Refer to Table IV for examples.

|          |                                                                                                                                                                                                               |
|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RAV[4:0] | Right AUX Volume. Allows setting the AUX right channel attenuator in 32 volume levels. The LSB represents 1.5 dB, and the gain range is +12 dB to -34.5 dB. The default value is 0 dB, mute enabled.          |
| RM       | Right Channel Mute. Once enabled by the MSPLT bit in Register 76h, this bit mutes the right channel separately from the AM bit. Otherwise, this bit will always read 0 and will have no affect when set to 1. |
| LAV[4:0] | Left AUX Volume. Allows setting the AUX left channel attenuator in 32 volume levels. The LSB represents 1.5 dB, and the gain range is +12 dB to -34.5 dB. The default value is 0 dB, mute enabled.            |
| AM       | AUX Mute. When this bit is set to 1, both the left and right channels are muted, unless the MSPLT bit in Register 76h is set to 1, in which case this mute bit will affect only the left channel.             |

**PCM-Out Volume Register (Index 18h)**

| Reg No. | Name           | D15 | D14 | D13 | D12  | D11  | D10  | D9   | D8   | D7  | D6 | D5 | D4   | D3   | D2   | D1   | D0   | Default |
|---------|----------------|-----|-----|-----|------|------|------|------|------|-----|----|----|------|------|------|------|------|---------|
| 18h     | PCM-Out Volume | OM  | X   | X   | LOV4 | LOV3 | LOV2 | LOV1 | LOV0 | RM* | X  | X  | ROV4 | ROV3 | ROV2 | ROV1 | ROV0 | 8808h   |

\*For AC '97 compatibility, Bit D7 (RM) is available only by setting the MSPLT bit, Register 76h. The MSPLT bit enables separate mute bits for the left and right channels. If MSPLT is not set, RM bit has no effect. All registers not shown, and bits containing an X are assumed to be reserved. Refer to Table IV for examples.

|          |                                                                                                                                                                                                               |
|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ROV[4:0] | Right PCM-Out Volume. Allows setting the PCM right channel attenuator in 32 volume levels. The LSB represents 1.5 dB, and the range is +12 dB to -34.5 dB. The default value is 0 dB, mute enabled.           |
| RM       | Right Channel Mute. Once enabled by the MSPLT bit in Register 76h, this bit mutes the right channel separately from the OM bit. Otherwise, this bit will always read 0 and will have no effect when set to 1. |
| LOV[4:0] | Left PCM-Out Volume. Allows setting the PCM left channel attenuator in 32 volume levels. The LSB represents 1.5 dB, and the range is +12 dB to -34.5 dB. The default value is 0 dB, mute enabled.             |
| OM       | PCM-Out Volume Mute. When this bit is set to 1, both the left and right channels are muted unless the MSPLT bit in Register 76h is set to 1, in which case this mute bit will affect only the left channel.   |

**Table IV. Volume Settings for Line-In, CD Volume, AUX, and PCM-Out**

| Reg. 76h | Control Bits                                          |        |          |                             |                             |        |          |                              |
|----------|-------------------------------------------------------|--------|----------|-----------------------------|-----------------------------|--------|----------|------------------------------|
|          | Line-In (10h), CD (12h), AUX (16h), and PCM-Out (18h) |        |          |                             |                             |        |          |                              |
|          | Left Channel Volume D[12:8]                           |        |          |                             | Right Channel Volume D[4:0] |        |          |                              |
| MSPLT*   | D15                                                   | Write  | Readback | Function                    | D7*                         | Write  | Readback | Function                     |
| 0        | 0                                                     | 0 0000 | 0 0000   | 12 dB Gain                  | x                           | 0 0000 | 0 0000   | +12 dB Gain                  |
| 0        | 0                                                     | 0 1000 | 0 1000   | 0 dB Gain                   | x                           | 0 1000 | 0 1000   | 0 dB Gain                    |
| 0        | 0                                                     | 1 1111 | 1 1111   | 34.5 dB Gain                | x                           | 1 1111 | 1 1111   | -34.5 dB Gain                |
| 0        | 1                                                     | x xxxx | x xxxx   | -∞ dB Gain, Muted           | x                           | x xxxx | x xxxx   | -∞ dB Gain, Muted            |
| 1        | 0                                                     | 1 1111 | 1 1111   | -34.5 dB Gain               | 1                           | x xxxx | x xxxx   | -∞ dB Gain, Right Only Muted |
| 1        | 1                                                     | x xxxx | x xxxx   | -∞ dB Gain, Left Only Muted | 0                           | 1 1111 | 1 1111   | -34.5 dB Gain                |
| 1        | 1                                                     | x xxxx | x xxxx   | -∞ dB Gain, Left Muted      | 1                           | x xxxx | x xxxx   | -∞ dB Gain, Right Muted      |

\*For AC '97 compatibility, Bit D7 (RM) is available only by setting the MSPLT bit, Register 76h. The MSPLT bit enables separate mute bits for the left and right channels. If MSPLT is not set, RM bit has no effect.

x in the above table is a wild card and has no effect on the value.



Record Select Control Register (Index 1Ah)

| Reg No. | Name          | D15 | D14 | D13 | D12 | D11 | D10 | D9  | D8  | D7 | D6 | D5 | D4 | D3 | D2  | D1  | D0  | Default |
|---------|---------------|-----|-----|-----|-----|-----|-----|-----|-----|----|----|----|----|----|-----|-----|-----|---------|
| 1Ah     | Record Select | X   | X   | X   | X   | X   | LS2 | LS1 | LS0 | X  | X  | X  | X  | X  | RS2 | RS1 | RS0 | 0000h   |

All registers not shown and bits containing an X are assumed to be reserved. Used to select the record source independently for right and left. The default value is 0000h, which corresponds to MIC In. Refer to Table V for examples.

|         |                     |
|---------|---------------------|
| RS[2:0] | Right Record Select |
| LS[2:0] | Left Record Select  |

Table V. Settings for Record Select Control

| LS [10:8] | Left Record Source | RS [2:0] | Right Record Source |
|-----------|--------------------|----------|---------------------|
| 000       | MIC                | 000      | MIC                 |
| 001       | CD_L               | 001      | CD_R                |
| 010       | Muted              | 010      | Muted               |
| 011       | AUX_L              | 011      | AUX_R               |
| 100       | LINE_IN_L          | 100      | LINE_IN_R           |
| 101       | Stereo Mix (L)     | 101      | Stereo Mix (R)      |
| 110       | Mono Mix           | 110      | Mono Mix            |
| 111       | PHONE_IN           | 111      | PHONE_IN            |

Record Gain Register (Index 1Ch)

| Reg No. | Name        | D15 | D14 | D13 | D12 | D11  | D10  | D9   | D8   | D7  | D6 | D5 | D4 | D3   | D2   | D1   | D0   | Default |
|---------|-------------|-----|-----|-----|-----|------|------|------|------|-----|----|----|----|------|------|------|------|---------|
| 1Ch     | Record Gain | IM  | X   | X   | X   | LIM3 | LIM2 | LIM1 | LIM0 | RM* | X  | X  | X  | RIM3 | RIM2 | RIM1 | RIM0 | 8000h   |

\*For AC '97 compatibility, Bit D7 (RM) is available only by setting the MSPLT bit, Register 76h. The MSPLT bit enables separate mute bits for the left and right channels. If MSPLT is not set, RM bit has no effect. All registers not shown and bits containing an X are assumed to be reserved. Refer to Table VI for examples.

|          |                                                                                                                                                                                                               |
|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RIM[3:0] | Right Input Mixer Gain Control. Each LSB represents 1.5 dB, 0000 = 0 dB, and the gain range is 0 dB to 22.5 dB.                                                                                               |
| RM       | Right Channel Mute. Once enabled by the MSPLT bit in Register 76h, this bit mutes the right channel separately from the IM bit. Otherwise, this bit will always read 0 and will have no affect when set to 1. |
| LIM[3:0] | Left Input Mixer Gain Control. Each LSB represents 1.5 dB, 0000 = 0 dB, and the gain range is 0 dB to 22.5 dB.                                                                                                |
| IM       | Input Mute. When this bit is set to 1, both the left and right channels are muted, unless the MSPLT bit in Register 76h is set to 1, in which case this mute bit will affect only the left channel.           |

Table VI. Settings for Record Gain Register

| Reg. 76h | Control Bits—Record Gain (1Ch)   |       |          |                             |                                  |       |          |                              |
|----------|----------------------------------|-------|----------|-----------------------------|----------------------------------|-------|----------|------------------------------|
| MSPLT*   | Left Channel Input Mixer D[11:8] |       |          |                             | Right Channel Input Mixer D[3:0] |       |          |                              |
|          | D15                              | Write | Readback | Function                    | D7*                              | Write | Readback | Function                     |
| 0        | 0                                | 1111  | 1111     | 22.5 dB Gain                | x                                | 1111  | 1111     | 22.5 dB Gain                 |
| 0        | 0                                | 0000  | 0000     | 0 dB Gain                   | x                                | 0000  | 0000     | 0 dB Gain                    |
| 0        | 1                                | xxxx  | xxxx     | −∞ dB Gain, Muted           | x                                | xxxx  | xxxx     | −∞ dB Gain, Muted            |
| 1        | 0                                | 1111  | 1111     | 22.5 dB Gain                | 1                                | xxxx  | xxxx     | −∞ dB Gain, Right Only Muted |
| 1        | 1                                | xxxx  | xxxx     | −∞ dB Gain, Left Only Muted | 0                                | 1111  | 1111     | 22.5 dB Gain                 |
| 1        | 1                                | xxxx  | xxxx     | −∞ dB Gain, Left Muted      | 1                                | xxxx  | xxxx     | −∞ dB Gain, Right Muted      |

\*For AC '97 compatibility, Bit D7 (RM) is available only by setting the MSPLT bit, Register 76h. The MSPLT bit enables separate mute bits for the left and right channels. If MSPLT is not set, RM bit has no effect.

x is a wild card and has no effect on the value.



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**General-Purpose Register (Index 20h)**

| Reg No. | Name            | D15 | D14 | D13 | D12 | D11 | D10 | D9  | D8 | D7   | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---------|-----------------|-----|-----|-----|-----|-----|-----|-----|----|------|----|----|----|----|----|----|----|---------|
| 20h     | General-Purpose | X   | X   | X   | X   | X   | X   | MIX | MS | LPBK | X  | X  | X  | X  | X  | X  | X  | 0000h   |

This register should be read before writing to generate a mask for only the bit(s) that need to be changed. All registers not shown and bits containing an X are assumed to be reserved.

|      |                                                                                                                                                     |
|------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| LPBK | Loopback Control. ADC/DAC Digital Loopback Mode.<br>0 = No Loopback (Default).<br>1 = Loopback PCM Digital Data from ADC Output to DAC.             |
| MS   | MIC Select. Selects mono MIC input.<br>0 = Select MIC1.<br>1 = Select MIC2.<br>See 2CMIC bit in Register 76h to enable stereo microphone recording. |
| MIX  | Mono Output Select. Selects mono output audio source.<br>0 = Mixer mono output (reset default).<br>1 = MIC1 channel.                                |

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## Power-Down Control/Status Register (Index 26h)

| Reg No. | Name                 | D15  | D14 | D13 | D12 | D11 | D10 | D9  | D8  | D7 | D6 | D5 | D4 | D3  | D2  | D1  | D0  | Default |
|---------|----------------------|------|-----|-----|-----|-----|-----|-----|-----|----|----|----|----|-----|-----|-----|-----|---------|
| 26h     | Power-Down Ctrl/Stat | EAPD | PR6 | PR5 | PR4 | PR3 | PR2 | PR1 | PR0 | X  | X  | X  | X  | REF | ANL | DAC | ADC | 000Xh   |

The ready bits are read-only; writing to REF, ANL, DAC, ADC will have no effect. These bits indicate the status for the AD1981BL subsections. If the bit is a 1, that subsection is *ready*. *Ready* is defined as the subsection able to perform in its nominal state. All registers not shown, and bits containing an X are assumed to be reserved.

|          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ADC      | ADC Sections Ready to Transmit Data.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| DAC      | DAC Sections Ready to Accept Data.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| ANL      | Analog Amplifiers, Attenuators, and Mixers Ready.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| REF      | Voltage References, $V_{REF}$ and $V_{REFOUT}$ up to Nominal Level.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| PR [6:0] | <p>Codec Power-Down Modes. The first three bits are to be used individually rather than in combination with each other. PR3 can be used in combination with PR2 or by itself. The mixer and reference cannot be powered down via PR3 unless the ADCs and DACs are also powered down.</p> <p>Nothing else can be powered up until the reference is up. PR5 has no effect unless all ADCs, DACs, and the ac-link are powered down. The reference and the mixer can be either up or down, but all power-up sequences must be allowed to run to completion before PR5 and PR4 are both set.</p> <p>In multiple codec systems, the master codec's PR5 and PR4 bits control the slave codec. PR5 is also effective in the slave codec if the master's PR5 bit is clear, but the PR4 bit has no effect except to enable or disable PR5.</p> |
| EAPD     | <p>External Audio Power-Down Control. Controls the state of the EAPD pin.</p> <p>EAPD = 0 sets the EAPD pin low, enabling an external power amplifier (reset default).</p> <p>EAPD = 1 sets the EAPD pin high, shutting the external power amplifier off.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |

| Power-Down State                                          | Set Bits                          | PR [6:0]   |
|-----------------------------------------------------------|-----------------------------------|------------|
| ADCs and Input Mux Power-Down                             | PR0                               | [000 0001] |
| DACs Power-Down                                           | PR1                               | [000 0010] |
| Analog Mixer Power-Down ( $V_{REF}$ and $V_{REFOUT}$ On)  | PR1, PR2                          | [000 0101] |
| Analog Mixer Power-Down ( $V_{REF}$ and $V_{REFOUT}$ Off) | PR0, PR1, PR3                     | [000 1011] |
| AC-Link Interface Power-Down                              | PR4                               | [001 0000] |
| Internal Clocks Disabled                                  | PR0, PR1, PR4, PR5                | [011 0011] |
| ADC and DAC Power-Down                                    | PR0, PR1                          | [000 0011] |
| $V_{REF}$ Standby Mode                                    | PR0, PR1, PR2, PR4, PR5           | [011 0111] |
| Total Power-Down                                          | PR0, PR1, PR2, PR3, PR4, PR5, PR6 | [111 1111] |
| Headphone Amp Power-In Standby                            | PR6                               | [100 0000] |

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**Extended Audio ID Register (Index 28h)**

| Reg No. | Name           | D15  | D14  | D13 | D12 | D11   | D10   | D9   | D8 | D7 | D6 | D5   | D4   | D3 | D2    | D1 | D0   | Default |
|---------|----------------|------|------|-----|-----|-------|-------|------|----|----|----|------|------|----|-------|----|------|---------|
| 28h     | Ext'd Audio ID | IDC1 | IDC0 | X   | X   | REVC1 | REVC0 | AMAP | X  | X  | X  | DSA1 | DSA0 | X  | SPDIF | X  | VRAS | X605h   |

The Extended Audio ID register identifies which extended audio features are supported. A nonzero Extended Audio ID value indicates that one or more of the extended audio features are supported. All registers not shown, and bits containing an X are assumed to be reserved.

|           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| VRAS      | Variable Rate PCM Audio Support (Read-Only). This bit returns a 1 when Read To indicates that the variable rate PCM audio is supported.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| SPDIF     | SPDIF Support (Read-Only). This bit returns a 1 when Read To indicates that the SPDIF transmitter is supported (IEC958).<br>This bit is also used to validate that the SPDIF transmitter output is actually enabled. The SPDIF bit is allowed to be set high only if the SPDIF pin (48) is pulled down at power-up, enabling the codec transmitter logic. If the SPDIF pin is floating or pulled high at power-up, the transmitter logic is disabled; therefore, this bit returns a low, indicating that the SPDIF transmitter is not available. This bit must always be read back to verify that the SPDIF transmitter is actually enabled. |
| DSA[1,0]  | DAC Slot Assignments (Read/Write) (Reset Default = 00).<br>00 DACs 1, 2 = 3 and 4.<br>01 DACs 1, 2 = 7 and 8.<br>10 DACs 1, 2 = 6 and 9.<br>11 Reserved.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| AMAP      | Slot DAC Mappings Based on Codec ID (Read-Only). This bit returns a 1 when read to indicate that slot/DAC mappings based on the codec ID are supported.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| REVC[1,0] | REVC[1,0] = 01 indicates codec is AC '97 revision 2.2 compliant (Read-Only).                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| IDC[1:0]  | Indicates Codec Configuration (Read-Only).<br>00 = Primary.<br>01, 10, 11 = Secondary.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |

## Extended Audio Status and Control Register (Index 2Ah)

| Reg No. | Name                  | D15    | D14 | D13 | D12 | D11 | D10  | D9 | D8 | D7 | D6 | D5    | D4    | D3 | D2    | D1 | D0  | Default |
|---------|-----------------------|--------|-----|-----|-----|-----|------|----|----|----|----|-------|-------|----|-------|----|-----|---------|
| 2Ah     | Ext'd Audio Stat/Ctrl | VFORCE | X   | X   | X   | X   | SPCV | X  | X  | X  | X  | SPSA1 | SPSA0 | X  | SPDIF | X  | VRA | 0000h   |

All registers not shown and bits containing an X are assumed to be reserved. The Extended Audio Status and Control register is a read/write register that provides status and control of the extended audio features.

|           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| VRA       | Variable Rate Audio (Read/Write).<br>VRA = 0 sets fixed sample rate audio at 48 kHz (reset default).<br>VRA = 1 enables variable rate audio mode (enables sample rate registers and SLOTREQ signaling).                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| SPDIF     | SPDIF Transmitter Subsystem Enable/Disable Bit (Read/Write).<br>SPDIF = 1 enables the SPDIF transmitter.<br>SPDIF = 0 disables the SPDIF transmitter (default).<br>This bit is also used to validate that the SPDIF transmitter output is actually enabled. The SPDIF bit is allowed to be set high only if the SPDIF pin (48) is pulled down at power-up, enabling the codec transmitter logic. If the SPDIF pin is floating or pulled high at power-up, the transmitter logic is disabled and this bit therefore returns a low, indicating that the SPDIF transmitter is not available. This bit must always be read back to verify that the SPDIF transmitter is actually enabled. |
| SPSA[1:0] | SPDIF Slot Assignment Bits (Read/Write). These bits control the SPDIF slot assignment and respective defaults, depending on the codec ID configuration.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| SPCV      | SPDIF Configuration Valid (Read-Only). Indicates the status of the SPDIF transmitter subsystem, enabling the driver to determine if the currently programmed SPDIF configuration is supported. SPCV is always valid, independent of the SPDIF enable bit status.<br>SPCV = 0 indicates current SPDIF configuration (SPSA, SPSR, DAC slot rate, DRS) is not valid (not supported).<br>SPCV = 1 indicates current SPDIF configuration (SPSA, SPSR, DAC slot rate, DRS) is valid (is supported).                                                                                                                                                                                         |
| VFORCE    | Validity Force Bit (Reset Default = 0).<br>When asserted, this bit forces the SPDIF stream Validity flag (Bit 28 within each SPDIF L/R subframe) to be controlled by the V bit (D15) in Register 3Ah (SPDIF control register).<br>VFORCE = 0 and V = 0; the Validity bit is managed by the codec error detection logic.<br>VFORCE = 0 and V = 1; the Validity bit is forced high, indicating subframe data is invalid.<br>VFORCE = 1 and V = 0; the Validity bit is forced low, indicating subframe data is valid.<br>VFORCE = 1 and V = 1; the Validity bit is forced high, indicating subframe data is invalid.                                                                     |

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## AC '97 2.2 AMAP Compliant Default SPDIF Slot Assignments

| Codec ID | Function                | SPSA = 00 | SPSA = 01         | SPSA = 10         | SPSA = 11           |
|----------|-------------------------|-----------|-------------------|-------------------|---------------------|
| 00       | 2-Ch Primary w/SPDIF    | 3 and 4   | 7 and 8 (default) | 6 and 9           | 10 and 11           |
| 00       | 4-Ch Primary w/SPDIF    | 3 and 4   | 7 and 8           | 6 and 9 (default) | 10 and 11           |
| 00       | 6-Ch Primary w/SPDIF    | 3 and 4   | 7 and 8           | 6 and 9           | 10 and 11 (default) |
| 01       | +2-Ch Secondary w/SPDIF | 3 and 4   | 7 and 8           | 6 and 9 (default) |                     |
| 01       | +4-Ch Secondary w/SPDIF | 3 and 4   | 7 and 8           | 6 and 9           | 10 and 11 (default) |
| 10       | +2-Ch Secondary w/SPDIF | 3 and 4   | 7 and 8           | 6 and 9 (default) |                     |
| 10       | +4-Ch Secondary w/SPDIF | 3 and 4   | 7 and 8           | 6 and 9           | 10 and 11 (default) |
| 11       | +2-Ch Secondary w/SPDIF | 3 and 4   | 7 and 8           | 6 and 9           | 10 and 11 (default) |

## PCM Front DAC Rate Register (Index 2Ch)

| Reg No. | Name               | D15   | D14   | D13   | D12   | D11   | D10   | D9   | D8   | D7   | D6   | D5   | D4   | D3   | D2   | D1   | D0   | Default |
|---------|--------------------|-------|-------|-------|-------|-------|-------|------|------|------|------|------|------|------|------|------|------|---------|
| 2Ch     | PCM Front DAC Rate | SRF15 | SRF14 | SRF13 | SRF12 | SRF11 | SRF10 | SRF9 | SRF8 | SRF7 | SRF6 | SRF5 | SRF4 | SRF3 | SRF2 | SRF1 | SRF0 | BB80h   |

This read/write sample rate control register contains a 16-bit unsigned value, representing the rate of operation in Hz.

|           |                                                                                                                                                                   |
|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SRF[15:0] | Sample Rate. The sampling frequency range is from 7 kHz (1B58h) to 48 kHz (BB80h) in 1 Hz increments. If 0 is written to VRA, the sample rate is reset to 48 kHz. |
|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|

## PCM ADC Rate Register (Index 32h)

| Reg No. | Name             | D15   | D14   | D13   | D12   | D11   | D10   | D9   | D8   | D7   | D6   | D5   | D4   | D3   | D2   | D1   | D0   | Default |
|---------|------------------|-------|-------|-------|-------|-------|-------|------|------|------|------|------|------|------|------|------|------|---------|
| 32h     | PCM L/R ADC Rate | SRA15 | SRA14 | SRA13 | SRA12 | SRA11 | SRA10 | SRA9 | SRA8 | SRA7 | SRA6 | SRA5 | SRA4 | SRA3 | SRA2 | SRA1 | SRA0 | BB80h   |

This read/write sample rate control register contains 16-bit unsigned value, representing the rate of operation in Hz.

|           |                                                                                                                                                                   |
|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SRA[15:0] | Sample Rate. The sampling frequency range is from 7 kHz (1B58h) to 48 kHz (BB80h) in 1 Hz increments. If 0 is written to VRA, the sample rate is reset to 48 kHz. |
|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|

## SPDIF Control Register (Index 3Ah)

| Reg No. | Name          | D15 | D14 | D13   | D12   | D11 | D10 | D9  | D8  | D7  | D6  | D5  | D4  | D3  | D2   | D1  | D0  | Default |
|---------|---------------|-----|-----|-------|-------|-----|-----|-----|-----|-----|-----|-----|-----|-----|------|-----|-----|---------|
| 3Ah     | SPDIF Control | V   | X   | SPSR1 | SPSR0 | L   | CC6 | CC5 | CC4 | CC3 | CC2 | CC1 | CC0 | PRE | COPY | AUD | PRO | 2000h   |

Register 3Ah is a read/write register that controls SPDIF functionality and manages bit fields propagated as channel status (or subframe in the V case). With the exception of V, this register should be written to only when the SPDIF transmitter is disabled (SPDIF bit in Register 2Ah is 0). This ensures that control and status information start up correctly at the beginning of SPDIF transmission.

|           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PRO       | Professional. 1 indicates professional use of channel status.<br>0 indicates consumer.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| AUD       | Non-Audio. 1 indicates data is non-PCM format.<br>0 data is PCM.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| COPY      | Copyright. 1 indicates copyright is asserted.<br>0 copyright is not asserted.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| PRE       | Pre-Emphasis. 1 indicates filter pre-emphasis is 50 $\mu$ s/15 $\mu$ s.<br>0 pre-emphasis is none.                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| CC[6:0]   | Category Code. Programmed according to IEC standards, or as appropriate.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| L         | Generation Level. Programmed according to IEC standards, or as appropriate.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| SPSR[1:0] | SPDIF Transmit Sample Rate.<br>SPSR[1:0] = 00 Transmit sample rate = 44.1 kHz.<br>SPSR[1:0] = 01 Reserved.<br>SPSR[1:0] = 10 Transmit sample rate = 48 kHz (reset default).<br>SPSR[1:0] = 11 Not supported.                                                                                                                                                                                                                                                                                                                                                           |
| V         | Validity. This bit affects the validity flag (Bit 28 transmitted in each SPDIF L/R subframe) and enables the SPDIF transmitter to maintain connection during error or mute conditions.<br>V = 1 Each SPDIF subframe (L + R) has Bit 28 set to 1. This tags both samples as invalid.<br>V = 0 Each SPDIF subframe (L + R) has Bit 28 set to 0 for valid data and 1 for invalid data (error condition).<br>Note that when V = 0, asserting the VFORCE bit (D15) in Register 2Ah (Ext'd Audio Stat/Ctrl) will force the Validity flag low, marking both samples as valid. |

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**EQ Control Register (Index 60h)**

| Reg No. | Name    | D15 | D14      | D13 | D12 | D11 | D10 | D9 | D8 | D7  | D6  | D5   | D4   | D3   | D2   | D1   | D0   | Default |
|---------|---------|-----|----------|-----|-----|-----|-----|----|----|-----|-----|------|------|------|------|------|------|---------|
| 60h     | EQ CTRL | EQM | MAD LBEN | X   | X   | X   | X   | X  | X  | SYM | CHS | BCA5 | BCA4 | BCA3 | BCA2 | BCA1 | BCA0 | 8080h   |

Register 60h is a read/write register that controls the equalizer functionality and data setup. This register also contains the Biquad and Coefficient Address pointer, which is used in conjunction with the EQ Data Register (78h) to set up the equalizer coefficients. The reset default disables the equalizer function until the coefficients can be properly set up by the software and sets the Symmetry bit to allow equal coefficients for left and right channels. All registers not shown and bits containing an X are assumed to be reserved.

|          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| BCA[5,0] | <p>Biquad and Coefficient Address Pointer</p> <p>biquad 0 coef a0 BCA[5,0] = 011011</p> <p>biquad 0 coef a1 BCA[5,0] = 011010</p> <p>biquad 0 coef a2 BCA[5,0] = 011001</p> <p>biquad 0 coef b1 BCA[5,0] = 011101</p> <p>biquad 0 coef b2 BCA[5,0] = 011100</p> <p>biquad 1 coef a0 BCA[5,0] = 100000</p> <p>biquad 1 coef a1 BCA[5,0] = 011111</p> <p>biquad 1 coef a2 BCA[5,0] = 011110</p> <p>biquad 1 coef b1 BCA[5,0] = 100010</p> <p>biquad 1 coef b2 BCA[5,0] = 100001</p> <p>biquad 2 coef a0 BCA[5,0] = 100101</p> <p>biquad 2 coef a1 BCA[5,0] = 100100</p> <p>biquad 2 coef a2 BCA[5,0] = 100011</p> <p>biquad 2 coef b1 BCA[5,0] = 100111</p> <p>biquad 2 coef b2 BCA[5,0] = 100110</p> <p>biquad 3 coef a0 BCA[5,0] = 101010</p> <p>biquad 3 coef a1 BCA[5,0] = 101001</p> <p>biquad 3 coef a2 BCA[5,0] = 101000</p> <p>biquad 3 coef b1 BCA[5,0] = 101100</p> <p>biquad 3 coef b2 BCA[5,0] = 101011</p> <p>biquad 4 coef a0 BCA[5,0] = 101111</p> <p>biquad 4 coef a1 BCA[5,0] = 101110</p> <p>biquad 4 coef a2 BCA[5,0] = 101101</p> <p>biquad 4 coef b1 BCA[5,0] = 110001</p> <p>biquad 4 coef b2 BCA[5,0] = 110000</p> <p>biquad 5 coef a0 BCA[5,0] = 110100</p> <p>biquad 5 coef a1 BCA[5,0] = 110011</p> <p>biquad 5 coef a2 BCA[5,0] = 110010</p> <p>biquad 5 coef b1 BCA[5,0] = 110110</p> <p>biquad 5 coef b2 BCA[5,0] = 110101</p> <p>biquad 6 coef a0 BCA[5,0] = 111001</p> <p>biquad 6 coef a1 BCA[5,0] = 111000</p> <p>biquad 6 coef a2 BCA[5,0] = 110111</p> <p>biquad 6 coef b1 BCA[5,0] = 111011</p> <p>biquad 6 coef b2 BCA[5,0] = 111010</p> |
| CHS      | <p>Channel Select.</p> <p>CHS = 0 selects left channel coefficients data block.</p> <p>CHS = 1 selects right channel coefficients data block.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| SYM      | <p>Symmetry. When set to 1, this bit indicates that the left and right channel coefficients are equal. This shortens the coefficients' setup sequence since only the left channel coefficients need to be addressed and set up (the right channel coefficients are fetched from the left channel memory).</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| MAD LBEN | <p>Mixer ADC Loopback Enable. Enables mixer ADC data to be summed into PCM stream.</p> <p>0 = No loopback allowed (default).</p> <p>1 = Enable loopback.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| EQM      | <p>Equalizer Mute. When set to 1, this bit disables the equalizer function (allows all data to pass through). The reset default sets this bit to 1, disabling the equalizer function until the biquad coefficients can be properly set.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |



## EQ Data Register (Index 62h)

| Reg No. | Name    | D15   | D14   | D13   | D12   | D11   | D10   | D9   | D8   | D7   | D6   | D5   | D4   | D3   | D2   | D1   | D0   | Default |
|---------|---------|-------|-------|-------|-------|-------|-------|------|------|------|------|------|------|------|------|------|------|---------|
| 62h     | EQ DATA | CFD15 | CFD14 | CFD13 | CFD12 | CFD11 | CFD10 | CFD9 | CFD8 | CFD7 | CFD6 | CFD5 | CFD4 | CFD3 | CFD2 | CFD1 | CFD0 | 0000h   |

This read/write register is used to transfer EQ biquad coefficients into memory. The register data is transferred to, or retrieved from, the address pointed to by the BCA bits in the EQ CNTRL Register (60h). Data will be written to memory only if the EQM bit (Register 60h, Bit 15) is asserted.

|           |                                                                                                                                                            |
|-----------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CFD[15:0] | Coefficient Data. The biquad coefficients are fixed point format values with 16 bits of resolution. The CFD15 bit is the MSB, and the CFD0 bit is the LSB. |
|-----------|------------------------------------------------------------------------------------------------------------------------------------------------------------|

## Mixer ADC, Input Gain Register (Index 64h)

| Reg No. | Name         | D15 | D14 | D13 | D12 | D11  | D10  | D9   | D8   | D7  | D6 | D5 | D4 | D3   | D2   | D1   | D0   | Default |
|---------|--------------|-----|-----|-----|-----|------|------|------|------|-----|----|----|----|------|------|------|------|---------|
| 64h     | Mixer Volume | MXM | X   | X   | X   | LMG3 | LMG2 | LMG1 | LMG0 | RM* | X  | X  | X  | RMG3 | RMG2 | RMG1 | RMG0 | 8000h   |

\*For AC '97 compatibility, Bit D7 (RM) is available only by setting the MSPLT bit, Register 76h. The MSPLT bit enables separate mute bits for the left and right channels. If MSPLT is not set, the RM bit has no effect. All registers not shown and bits containing an X are assumed to be reserved. Refer to Table VII for examples.

|          |                                                                                                                                                                                                                |
|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| RMG[3:0] | Right Mixer Gain Control. This register controls the gain into the mixer ADC from 0 dB to a maximum gain of 22.5 dB. The least significant bit represents 1.5 dB.                                              |
| RM       | Right Channel Mute. Once enabled by the MSPLT bit in Register 76h, this bit mutes the right channel separately from the MXM bit. Otherwise, this bit will always read 0 and will have no affect when set to 1. |
| LMG[3:0] | Left Mixer Gain Control. This register controls the gain into the mixer ADC, from 0 dB to a maximum gain of 22.5 dB. The least significant bit represents 1.5 dB.                                              |
| MXM      | Mixer Gain Register Mute.<br>0 = Unmuted.<br>1 = Muted (reset default).                                                                                                                                        |

Table VII. Settings for Mixer ADC, Input Gain

| Reg. 76h | Control Bits<br>Mixer ADC, Input Gain (64h) |       |          |                             |                                 |       |          |                              |
|----------|---------------------------------------------|-------|----------|-----------------------------|---------------------------------|-------|----------|------------------------------|
|          | Left Channel Mixer Gain D[11:8]             |       |          |                             | Right Channel Mixer Gain D[3:0] |       |          |                              |
| MSPLT*   | D15                                         | Write | Readback | Function                    | D7*                             | Write | Readback | Function                     |
| 0        | 0                                           | 1111  | 1111     | 22.5 dB Gain                | x                               | 1111  | 1111     | 22.5 dB Gain                 |
| 0        | 0                                           | 0000  | 0000     | 0 dB Gain                   | x                               | 0000  | 0000     | 0 dB Gain                    |
| 0        | 1                                           | xxxx  | xxxx     | −∞ dB Gain, Muted           | x                               | xxxx  | xxxx     | −∞ dB Gain, Muted            |
| 1        | 0                                           | 1111  | 1111     | 22.5 dB Gain                | 1                               | xxxx  | xxxx     | −∞ dB Gain, Right Only Muted |
| 1        | 1                                           | xxxx  | xxxx     | −∞ dB Gain, Left Only Muted | 0                               | 1111  | 1111     | 22.5 dB Gain                 |
| 1        | 1                                           | xxxx  | xxxx     | −∞ dB Gain, Left Muted      | 1                               | xxxx  | xxxx     | −∞ dB Gain, Right Muted      |

\*For AC '97 compatibility, Bit D7 (RM) is available only by setting the MSPLT bit, Register 76h. The MSPLT bit enables separate mute bits for the left and right channels. If MSPLT is not set, RM bit has no effect.

x is a wild card and has no effect on the value.

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**Jack Sense/Audio Interrupt/Status Register (Index 72h)**

| Reg No. | Name       | D15 | D14 | D13 | D12    | D11    | D10    | D9      | D8      | D7      | D6      | D5     | D4     | D3     | D2     | D1      | D0      | Default |
|---------|------------|-----|-----|-----|--------|--------|--------|---------|---------|---------|---------|--------|--------|--------|--------|---------|---------|---------|
| 72h     | Jack Sense | X   | X   | X   | JS MT2 | JS MT1 | JS MT0 | JS1 EQB | JS0 EQB | JS1 TMR | JS0 TMR | JS1 MD | JS0 MD | JS1 ST | JS0 ST | JS1 INT | JS0 INT | 0000h   |

All register bits are read/write except for JS0ST and JS1ST, which are read-only. All registers not shown and bits containing an X are assumed to be reserved.

|           |                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| JS0INT    | Indicates Pin JS0 Has Generated an Interrupt. Remains set until the software services JS0 interrupt, i.e., JS0 ISR should clear this bit by writing a 0 to it. Note that the interrupt to the system is actually an OR combination of this bit and JS1INT. Also note that the actual interrupt implementation is selected by the INTS bit (Register 76h). It is also possible to generate a software system interrupt by writing a 1 to this bit. |
| JS1INT    | Indicates Pin JS1 Has Generated an Interrupt. Remains set until the software services JS1 interrupt, i.e., JS1 ISR should clear this bit by writing a 0 to it. See JS0INT description for additional details.                                                                                                                                                                                                                                     |
| JS0ST     | JS0 State. This bit always reports the logic state of JS0 pin.                                                                                                                                                                                                                                                                                                                                                                                    |
| JS1ST     | JS1 State. This bit always reports the logic state of JS1 pin.                                                                                                                                                                                                                                                                                                                                                                                    |
| JS0MD     | JS0 Mode. This bit selects the operation mode for the JS0 pin.<br>0 = Jack Sense mode (default).<br>1 = Interrupt mode.                                                                                                                                                                                                                                                                                                                           |
| JS1MD     | JS1 Mode. This bit selects the operation mode for the JS1 pin.<br>0 = Jack Sense mode (default).<br>1 = Interrupt mode.                                                                                                                                                                                                                                                                                                                           |
| JS0TMR    | JS0 Timer Enable. If this bit is set to a 1, JS0 must be high for greater than 278 ms to be recognized.                                                                                                                                                                                                                                                                                                                                           |
| JS1TMR    | JS1 Timer Enable. If this bit is set to a 1, JS1 must be high for greater than 278 ms to be recognized.                                                                                                                                                                                                                                                                                                                                           |
| JS0EQB    | JS0 EQ Bypass Enable. This bit enables JS0 to control the EQ bypass. When this bit is set to 1, JS0 = 1 will cause the EQ to be bypassed.                                                                                                                                                                                                                                                                                                         |
| JS1EQB    | JS1 EQ Bypass Enable. This bit enables JS1 to control the EQ bypass. When this bit is set to 1, JS1 = 1 will cause the EQ to be bypassed.                                                                                                                                                                                                                                                                                                         |
| JSMT[2,0] | JS Mute Enable Selector. These three bits select and enable the Jack Sense muting action (see Table VIII).                                                                                                                                                                                                                                                                                                                                        |

Table VIII. Jack Sense Mute Select-JSMT [2:0]

| REF | JS1 Headphone | JS0 Line Out | JSMT2 | JSMT1 | JSMT0 | H.P. Out | Line Out | Mono Out | Notes                                                  |
|-----|---------------|--------------|-------|-------|-------|----------|----------|----------|--------------------------------------------------------|
| 0   | OUT (0)       | OUT (0)      | 0     | 0     | 0     | ACTIVE   | ACTIVE   | ACTIVE   | JS0 and JS1 Ignored.                                   |
| 1   | OUT (0)       | IN (1)       | 0     | 0     | 0     | ACTIVE   | ACTIVE   | ACTIVE   |                                                        |
| 2   | IN (1)        | OUT (0)      | 0     | 0     | 0     | ACTIVE   | ACTIVE   | ACTIVE   |                                                        |
| 3   | IN (1)        | IN (1)       | 0     | 0     | 0     | ACTIVE   | ACTIVE   | ACTIVE   |                                                        |
| 4   | OUT (0)       | OUT (0)      | 0     | 0     | 1     | FMUTE    | FMUTE    | ACTIVE   | JS0 No Mute Action;<br>JS1 Mutes Line_Out.             |
| 5   | OUT (0)       | IN (1)       | 0     | 0     | 1     | FMUTE    | ACTIVE   | ACTIVE   |                                                        |
| 6   | IN (1)        | OUT (0)      | 0     | 0     | 1     | ACTIVE   | FMUTE    | ACTIVE   |                                                        |
| 7   | IN (1)        | IN (1)       | 0     | 0     | 1     | ACTIVE   | FMUTE    | ACTIVE   |                                                        |
| 8   | OUT (0)       | OUT (0)      | 0     | 1     | 0     | FMUTE    | FMUTE    | ACTIVE   | JS0 No Mute Action;<br>JS1 Mutes Mono and<br>Line_Out. |
| 9   | OUT (0)       | IN (1)       | 0     | 1     | 0     | FMUTE    | ACTIVE   | ACTIVE   |                                                        |
| 10  | IN (1)        | OUT (0)      | 0     | 1     | 0     | ACTIVE   | FMUTE    | FMUTE    |                                                        |
| 11  | IN (1)        | IN (1)       | 0     | 1     | 0     | ACTIVE   | FMUTE    | FMUTE    |                                                        |
| 12  | OUT (0)       | OUT (0)      | 0     | 1     | 1     | **       | **       | **       | ** Reserved                                            |
| 13  | OUT (0)       | IN (1)       | 0     | 1     | 1     | **       | **       | **       |                                                        |
| 14  | IN (1)        | OUT (0)      | 0     | 1     | 1     | **       | **       | **       |                                                        |
| 15  | IN (1)        | IN (1)       | 0     | 1     | 1     | **       | **       | **       |                                                        |
| 16  | OUT (0)       | OUT (0)      | 1     | 0     | 0     | FMUTE    | FMUTE    | ACTIVE   | JS0 Mutes Mono;<br>JS1 No Mute Action.                 |
| 17  | OUT (0)       | IN (1)       | 1     | 0     | 0     | FMUTE    | ACTIVE   | FMUTE    |                                                        |
| 18  | IN (1)        | OUT (0)      | 1     | 0     | 0     | ACTIVE   | FMUTE    | ACTIVE   |                                                        |
| 19  | IN (1)        | IN (1)       | 1     | 0     | 0     | ACTIVE   | ACTIVE   | FMUTE    |                                                        |
| 20  | OUT (0)       | OUT (0)      | 1     | 0     | 1     | FMUTE    | FMUTE    | ACTIVE   | JS0 Mutes Mono;<br>JS1 Mutes Line_Out.                 |
| 21  | OUT (0)       | IN (1)       | 1     | 0     | 1     | FMUTE    | ACTIVE   | FMUTE    |                                                        |
| 22  | IN (1)        | OUT (0)      | 1     | 0     | 1     | ACTIVE   | FMUTE    | ACTIVE   |                                                        |
| 23  | IN (1)        | IN (1)       | 1     | 0     | 1     | ACTIVE   | FMUTE    | FMUTE    |                                                        |
| 24  | OUT (0)       | OUT (0)      | 1     | 1     | 0     | FMUTE    | FMUTE    | ACTIVE   | JS0 Mutes Mono;<br>JS1 Mutes Mono and<br>Line_Out.     |
| 25  | OUT (0)       | IN (1)       | 1     | 1     | 0     | FMUTE    | ACTIVE   | FMUTE    |                                                        |
| 26  | IN (1)        | OUT (0)      | 1     | 1     | 0     | ACTIVE   | FMUTE    | FMUTE    |                                                        |
| 27  | IN (1)        | IN (1)       | 1     | 1     | 0     | ACTIVE   | FMUTE    | FMUTE    |                                                        |
| 28  | OUT (0)       | OUT (0)      | 1     | 1     | 1     | **       | **       | **       | ** Reserved                                            |
| 29  | OUT (0)       | IN (1)       | 1     | 1     | 1     | **       | **       | **       |                                                        |
| 30  | IN (1)        | OUT (0)      | 1     | 1     | 1     | **       | **       | **       |                                                        |
| 31  | IN (1)        | IN (1)       | 1     | 1     | 1     | **       | **       | **       |                                                        |

FMUTE = Output is forced to mute independent of the respective volume register setting.

ACTIVE = Output is not muted and its status is dependent on the respective volume register setting.

OUT = Nothing plugged into the jack and therefore the JS status is low (via the load resistor pull-down).

IN = Jack has plug inserted and therefore the JS status is high (via the codec JS internal pull-up).

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**Serial Configuration Register (Index 74h)**

| Reg No. | Name                 | D15    | D14   | D13   | D12   | D11 | D10 | D9 | D8   | D7 | D6 | D5 | D4   | D3 | D2   | D1   | D0    | Default |
|---------|----------------------|--------|-------|-------|-------|-----|-----|----|------|----|----|----|------|----|------|------|-------|---------|
| 74h     | Serial Configuration | SLOT16 | REGM2 | REGM1 | REGM0 | X   | X   | X  | CHEN | X  | X  | X  | INTS | X  | SPAL | SPDZ | SPLNK | 7001h   |

This register is not reset when the reset register (Register 00h) is written. All registers not shown and bits containing an X are assumed to be reserved.

|        |                                                                                                                                                                                                           |
|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SPLNK  | SPDIF Link. This bit enables the SPDIF to link with the DAC for data requesting.<br>0 = SPDIF and DAC are not linked.<br>1 = SPDIF and DAC are linked and receive the same data requests (reset default). |
| SPDZ   | SPDIF DACZ.<br>0 = Repeat last sample out of the SPDIF stream if FIFO underruns (reset default).<br>1 = Forces midscale sample out the SPDIF stream if FIFO underruns.                                    |
| SPAL   | SPDIF ADC Loop-Around.<br>0 = SPDIF transmitter is connected to the ac-link stream (reset default).<br>1 = SPDIF transmitter is connected to the digital ADC stream, not the ac-link.                     |
| INTS   | Interrupt Mode Select. This bit selects the JS interrupt implementation path.<br>0 = Bit 0 SLOT 12 (modem interrupt).<br>1 = Slot 6 valid bit (MIC ADC interrupt).                                        |
| CHEN   | Chain Enable. This bit enables chaining of a slave codec SDATA_IN stream into the ID0 pin (Pin 45).<br>0 = Disable chaining (reset default).<br>1 = Enable chaining into ID0 pin.                         |
| REGM0  | Master Codec Register Mask.                                                                                                                                                                               |
| REGM1  | Slave 1 Codec Register Mask.                                                                                                                                                                              |
| REGM2  | Slave 2 Codec Register Mask.                                                                                                                                                                              |
| SLOT16 | Enable 16-Bit Slot Mode. SLOT16 makes all ac-link slots 16 bits in length, formatted into 16 slots. This is a preferred mode for DSP serial port interfacing.                                             |

**Miscellaneous Control Bit Register (Index 76h)**

| Reg No. | Name              | D15  | D14 | D13   | D12   | D11 | D10 | D9   | D8 | D7    | D6    | D5 | D4    | D3    | D2    | D1   | D0   | Default |
|---------|-------------------|------|-----|-------|-------|-----|-----|------|----|-------|-------|----|-------|-------|-------|------|------|---------|
| 76h     | Misc Control Bits | DACZ | X   | MSPLT | LODIS | DAM | X   | FMXE | X  | MADPD | 2CMIC | X  | MADST | VREFH | VREFD | MBG1 | MBG0 | 0000h   |

All registers not shown and bits containing an X are assumed to be reserved.

|          |                                                                                                                                                                                                                                                                                                                                                                                  |
|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| MBG[1:0] | MIC Boost Gain Change Register.<br>These two bits allow changing the MIC preamp gain from the nominal 20 dB gain.<br>Note: This gain setting takes affect only while Bit D6 (M20) on the MIC volume register (0Eh) is set to 1; otherwise, the MIC boost block has a gain of 0 dB.<br>00 = 20 dB gain (reset default).<br>01 = 10 dB gain.<br>10 = 30 dB gain.<br>11 = Reserved. |
| VREFD    | V <sub>REFOUT</sub> Disable. Disables V <sub>REFOUT</sub> , placing it into High Z Out mode. Note that this bit overrides the VREFH bit selection (see below).<br>0 = V <sub>REFOUT</sub> pin is driven by the internal reference (reset default).<br>1 = V <sub>REFOUT</sub> pin is placed into High Z Out mode.                                                                |
| VREFH    | V <sub>REFOUT</sub> High. Changes V <sub>REFOUT</sub> from 2.25 V to 3.70 V for MIC bias applications.<br>0 = V <sub>REFOUT</sub> pin is set to 2.25 V output (reset default).<br>1 = V <sub>REFOUT</sub> pin is set to 2.25 V output.                                                                                                                                           |

|       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| MADST | Mixer ADC Status Bit. Indicates status of mixer digitizing ADC (left and right channels).<br>0 = Mixer ADC not ready.<br>1 = Mixer ADC ready.                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| MADPD | Mixer ADC Power-Down. Controls power down for mixer digitizing ADC.<br>0 = Mixer ADC is powered on (default).<br>1 = Mixer ADC is powered down.                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 2CMIC | 2-Channel MIC Select. This bit enables simultaneous recording from MIC1 and MIC2 inputs for applications that use a stereo microphone array. Note that this register works in conjunction with the MS bit in Register 20h.<br>0 = MIC1 or MIC2 (determined by MS bit) is routed to the record selector's left and right MIC channels as well as to the mixer (reset default).<br>1 = MIC1 is routed to the record selector's left MIC channel and MIC2 is routed to the record selector's right MIC channel. Note that in this mode, the MS bit should be set low and MIC1 can still be enabled into the mixer. |
| FMXE  | Front DAC into Mixer Enable. Controls the front (main) DAC to mixer mute switches.<br>0 = Front DAC outputs are allowed to sum into the mixer (reset default).<br>1 = Front DAC outputs are muted into the mixer (blocked).                                                                                                                                                                                                                                                                                                                                                                                     |
| DAM   | Digital Audio Mode. PCM DAC outputs bypass the analog mixer and are sent directly to the codec output.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| LODIS | LINE_OUT Disable. Disables the LINE_OUT pins (L/R), placing them into High Z mode so that the assigned output audio jack can be shared for input function (or other function).<br>0 = LINE_OUT pins have normal audio drive capability (reset default).<br>1 = LINE_OUT pins are placed into High Z mode.                                                                                                                                                                                                                                                                                                       |
| MSPLT | Mute Split. Allows separate mute control bits for Master, Headphone, LINE_IN, CD, AUX, and PCM volume control registers as well as record gain register.<br>0 = Both left and right channel mutes are controlled by Bit 15 in the respective registers (reset default).<br>1 = Bit 15 affects only the left channel mute and Bit 7 affects only the right channel mute.                                                                                                                                                                                                                                         |
| DACZ  | DAC Zero-Fill. Determines DAC data fill under starved conditions.<br>0 = DAC data is repeated when DACs are starved for data (reset default).<br>1 = DAC is zero-filled when DACs are starved for data.                                                                                                                                                                                                                                                                                                                                                                                                         |

## Vendor ID Register (Index 7Ch to 7Eh)

| Reg No. | Name       | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|---------|------------|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|---------|
| 7Ch     | Vendor ID1 | F7  | F6  | F5  | F4  | F3  | F2  | F1 | F0 | S7 | S6 | S5 | S4 | S3 | S2 | S1 | S0 | 4144h   |

S[7:0] This register is ASCII encoded to A.

F[7:0] This register is ASCII encoded to D.

| Reg No. | Name       | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7   | D6   | D5   | D4   | D3   | D2   | D1   | D0   | Default |
|---------|------------|-----|-----|-----|-----|-----|-----|----|----|------|------|------|------|------|------|------|------|---------|
| 7Eh     | Vendor ID2 | T7  | T6  | T5  | T4  | T3  | T2  | T1 | T0 | REV7 | REV6 | REV5 | REV4 | REV3 | REV2 | REV1 | REV0 | 5374h   |

T[7:0] This register is ASCII encoded to S.

REV[7:0] Vendor specific revision number: The AD1981BL assigns 74h to this field.

Table IX. Codec ID and External Clock Selection Table

| ID1 | ID0 | Codec ID       | Codec Clocking Source                           |
|-----|-----|----------------|-------------------------------------------------|
| 1   | 1   | (00) Primary   | 24.576 MHz (Local Xtal or External into XTL_IN) |
| 1   | 0   | (01) Secondary | 12.288 MHz (External into BIT_CLK)              |
| 0   | 1   | (00) Primary   | 48.000 MHz (External into XTL_IN)               |
| 0   | 0   | (00) Primary   | 14.31818 MHz (External into XTL_IN)             |

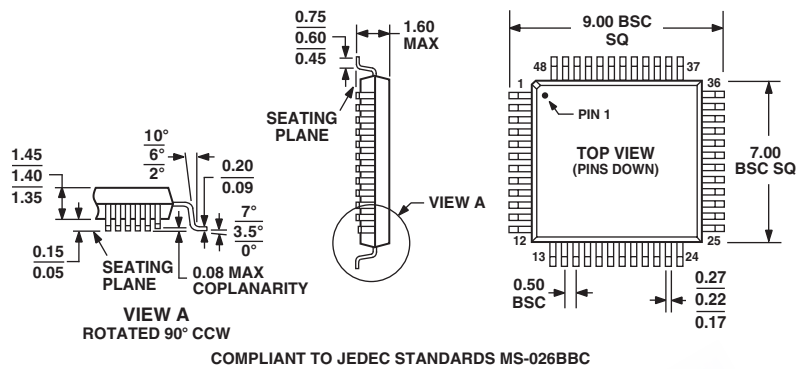
Note that internally, the  $\overline{ID}$  pins have weak pull-ups and are inverted.

AD1981BL

OUTLINE DIMENSIONS

48-Lead Low Profile Quad Flat Package [LQFP]  
(ST-48)

Dimensions shown in millimeters



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