Dual Fractional-N/Integer-N Frequency Synthesizer

ADF4252

FEATURES

- 3.0 GHz Fractional-N/1.2 GHz Integer-N
- 2.7 V to 3.3 V Power Supply
- Separate V_P Allows Extended Tuning Voltage to 5 V
- Programmable Dual Modulus Prescaler
  - RF: 4/5, 8/9
  - IF: 8/9, 16/17, 32/33, 64/65
- Programmable Charge Pump Currents
- 3-Wire Serial Interface
- Digital Lock Detect
- Power-Down Mode
- Programmable Modulus on Fractional-N Synthesizer
- Trade-Off Noise versus Spurious Performance

APPLICATIONS

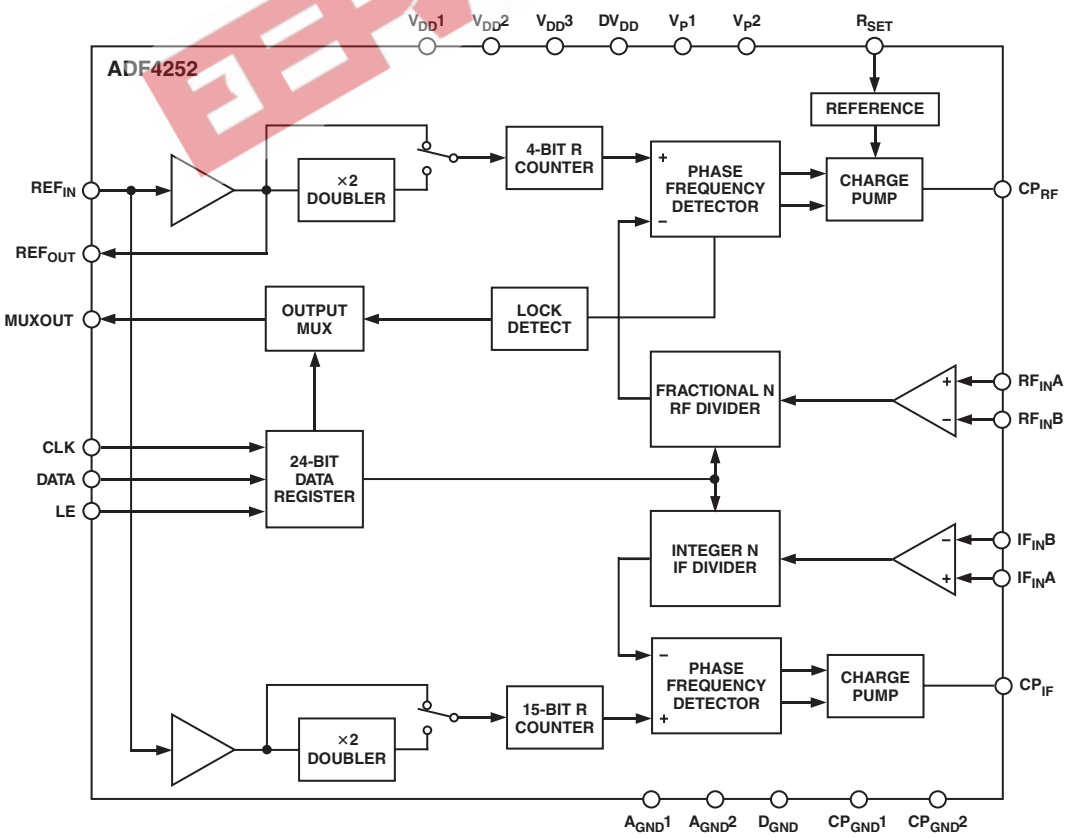
- Base Stations for Mobile Radio (GSM, PCS, DCS, CDMA, WCDMA)
- Wireless Handsets (GSM, PCS, DCS, CDMA, WCDMA)
- Wireless LANs
- Communications Test Equipment
- CATV Equipment

GENERAL DESCRIPTION

The ADF4252 is a dual fractional-N/integer-N frequency synthesizer that can be used to implement local oscillators (LO) in the upconversion and downconversion sections of wireless receivers and transmitters. Both the RF and IF synthesizers consist of a low noise digital PFD (phase frequency detector), a precision charge pump, and a programmable reference divider. The RF synthesizer has a Σ-Δ-based fractional interpolator that allows programmable fractional-N division. The IF synthesizer has programmable integer-N counters. A complete PLL (phase-locked loop) can be implemented if the synthesizer is used with an external loop filter and VCO (voltage controlled oscillator).

Control of all the on-chip registers is via a simple 3-wire interface. The devices operate with a power supply ranging from 2.7 V to 3.3 V and can be powered down when not in use.

FUNCTIONAL BLOCK DIAGRAM



REV. B

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ADF4252–SPECIFICATIONS[1] ($V_{DD}1 = V_{DD}2 = V_{DD}3 = DV_{DD} = 3$ V ± 10%, $DV_{DD} < V_P1$, $V_P2 < 5.5$ V, GND = 0 V, $R_{SET} = 2.7$ kΩ, dBm referred to 50 Ω, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

Parameter		B Version	Unit	Test Conditions/Comments
RF CHARACTERISTICS				
RF Input Frequency ($RF_{IN}A$, $RF_{IN}B$)[2]		0.25/3.0	GHz min/max	
RF Input Sensitivity		–10/0	dBm min/max	
RF Input Frequency ($RF_{IN}A$, $RF_{IN}B$)[2]		0.1/3.0	GHz min/max	Input Level = –8/0 dBm min/max
RF Phase Detector Frequency		30	MHz max	Guaranteed by Design
Allowable Prescaler Output Frequency		375	MHz max	
IF CHARACTERISTICS				
IF Input Frequency ($IF_{IN}A$, $IF_{IN}B$)[2]		50/1200	MHz min/max	
IF Input Sensitivity		–10/0	dBm min/max	
IF Phase Detector Frequency		55	MHz max	Guaranteed by Design
Allowable Prescaler Output Frequency		150	MHz max	
REFERENCE CHARACTERISTICS				
REF_{IN} Input Frequency		250	MHz max	For f < 10 MHz, use dc-coupled square wave (0 to V_{DD}).
REF_{IN} Input Sensitivity		0.5/V_{DD}1	V p-p min/max	AC-coupled. When dc-coupled, use 0 to V_{DD} max (CMOS compatible).
REF_{IN} Input Current		±100	µA max	
REF_{IN} Input Capacitance		10	pF max	
CHARGE PUMP				
RF I_{CP} Sink/Source	High Value	4.375	mA typ	See Table V
	Low Value	625	µA typ	
IF I_{CP} Sink/Source	High Value	5	mA typ	See Table IX
	Low Value	625	µA typ	
I_{CP} Three-State Leakage Current		1	nA typ	
RF Sink and Source Current Matching		2	% typ	0.5 V < V_{CP} < V_P – 0.5
R_{SET} Range		1.5/1.6	kΩ typ	See Table V
IF Sink and Source Current Matching		2	% typ	
I_{CP} vs. V_{CP}		2	% typ	0.5 V < V_{CP} < V_P – 0.5
I_{CP} vs. Temperature		2	% typ	$V_{CP} = V_P/2$
LOGIC INPUTS				
V_{INH}, Input High Voltage		1.35	V min	
V_{INL}, Input Low Voltage		0.6	V max	
I_{INH}/I_{INL}, Input Current		±1	µA max	
C_{IN} Input Capacitance		10	pF max	
LOGIC OUTPUTS				
V_{OH}, Output High Voltage		V_{DD} – 0.4	V min	I_{OH} = 0.2 mA
V_{OL}, Output Low Voltage		0.4	V max	I_{OL} = 0.2 mA
POWER SUPPLIES				
$V_{DD}1$, $V_{DD}2$, $V_{DD}3$		2.7/3.3	V min/V max	
DV_{DD}		$V_{DD}1$		
V_P1, V_P2		$V_{DD}1$/5.5	V min/V max	
I_{DD}[3]	RF + IF	13	mA typ	16 mA max
	RF Only	10	mA typ	13 mA max
	IF Only	4	mA typ	5.5 mA max
Power-Down Mode		1	µA typ	
RF NOISE AND SPURIOUS CHARACTERISTICS				
Noise Floor		–141	dBc/Hz typ	@ 20 MHz PFD Frequency
In-Band Phase Noise Performance[4]				@ VCO Output
Lowest Spur Mode		–90	dBc/Hz typ	RF_{OUT} = 1.8 GHz, PFD = 20 MHz
Low Noise and Spur Mode		–95	dBc/Hz typ	RF_{OUT} = 1.8 GHz, PFD = 20 MHz
Lowest Noise Mode		–103	dBc/Hz typ	RF_{OUT} = 1.8 GHz, PFD = 20 MHz
Spurious Signals				See Typical Performance Characteristics

NOTES

[1]Operating Temperature Range (B Version): –40°C to +85°C.

[2]Use a square wave for frequencies less than f_{MIN}.

[3]RF = 1 GHz, RF PFD = 10 MHz, MOD = 4095, IF = 500 MHz, IF PFD = 200 kHz, REF = 10 MHz, V_{DD} = 3 V, V_P1 = 5 V, and V_P2 = 3 V.

[4]The in-band phase noise is measured with the EVAL-ADF4252EB2 evaluation board and the HP5500E phase noise test system. The spectrum analyzer provides the REF_{IN} for the synthesizer (f_{REFOUT} = 10 MHz @ 0 dBm). f_{OUT} = 1.74 GHz, f_{REF} = 20 MHz, N = 87, Mod = 100, Channel Spacing = 200 kHz, V_{DD} = 3.3 V, and V_P = 5 V.

Specifications subject to change without notice.

TIMING CHARACTERISTICS* ($V_{DD}1 = V_{DD}2 = V_{DD}3 = DV_{DD}$ = 3 V ± 10%, $DV_{DD} < V_P1$, $V_P2 < 5.5$ V, GND = 0 V, unless otherwise noted.)

Parameter	Limit at T_{MIN} to T_{MAX} (B Version)	Unit	Test Conditions/Comments
t_1	10	ns min	LE Setup Time
t_2	10	ns min	DATA to CLOCK Setup Time
t_3	10	ns min	DATA to CLOCK Hold Time
t_4	25	ns min	CLOCK High Duration
t_5	25	ns min	CLOCK Low Duration
t_6	10	ns min	CLOCK to LE Setup Time
t_7	20	ns min	LE Pulse Width

*Guaranteed by design, but not production tested.

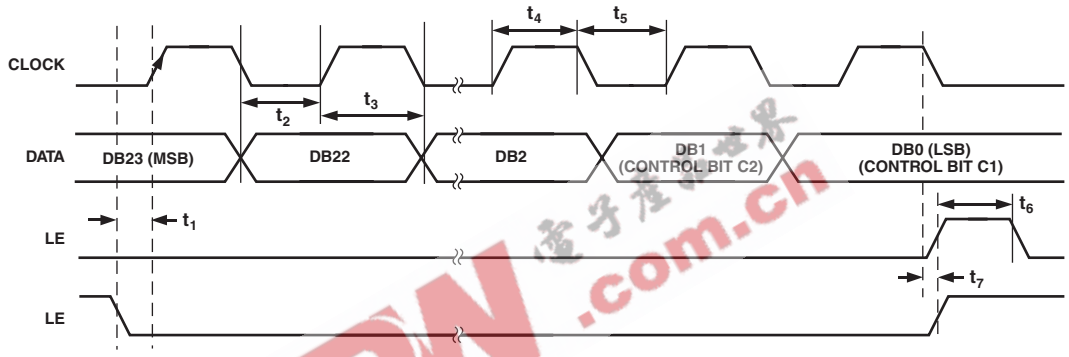


Figure 1. Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1, 2]

(T_A = 25°C, unless otherwise noted.)

$V_{DD}1$, $V_{DD}2$, $V_{DD}3$, DV_{DD} to GND[3] . . . . . –0.3 V to +4 V
REF_{IN}, $RF_{IN}A$, $RF_{IN}B$ to GND . . . . . –0.3 V to V_{DD} + 0.3 V
V_P1, V_P2 to GND . . . . . –0.3 V to +5.8 V
V_P1, V_P2 to $V_{DD}1$ . . . . . –3.3 V to +3.5 V
Digital I/O Voltage to GND . . . . . –0.3 V to V_{DD} + 0.3 V
Analog I/O Voltage to GND . . . . . –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
  Industrial (B Version) . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Maximum Junction Temperature . . . . . 150°C
CSP θ_{JA} Thermal Impedance . . . . . 122°C/W
Soldering Reflow Temperature
  Vapor Phase (60 sec max) . . . . . 240°C
  IR Reflow (20 sec max) . . . . . 240°C

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]This device is a high performance RF integrated circuit with an ESD rating of <2 kΩ, and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

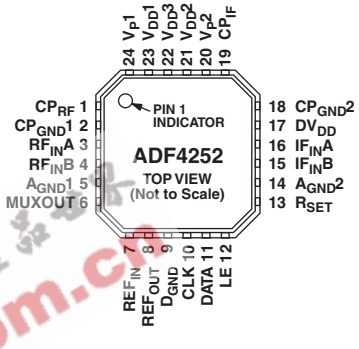
[3]GND = $CP_{GND}1$, $A_{GND}1$, D_{GND}, $A_{GND}2$, and $CP_{GND}2$.

ORDERING GUIDE

Mode	Temperature Range	Package Option*
ADF4252BCP	–40°C to +85°C	CP-24
ADF4252BCP-REEL	–40°C to +85°C	CP-24
ADF4252BCP-REEL7	–40°C to +85°C	CP-24
EVAL–ADF4252EB1		
EVAL–ADF4252EB2		

*CP = Chip Scale Package

PIN CONFIGURATION



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADF4252 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTIONS

Mnemonic	Function
CP_{RF}	RF Charge Pump Output. This is normally connected to a loop filter that drives the input to an external VCO.
$CP_{GND}1$	RF Charge Pump Ground.
$RF_{IN}A$	Input to the RF Prescaler. This small signal input is normally taken from the VCO.
$RF_{IN}B$	Complementary Input to the RF Prescaler.
$A_{GND}1$	Analog Ground for the RF Synthesizer.
MUXOUT	This multiplexer output allows either the RF or IF lock detect, the scaled RF or IF, or the scaled reference frequency to be accessed externally.
REF_{IN}	Reference Input. This is a CMOS input with a nominal threshold of $V_{DD}/2$ and an equivalent input resistance of 100 kΩ. This input can be driven from a TTL or CMOS crystal oscillator.
REF_{OUT}	Reference Output.
D_{GND}	Digital Ground for the Fractional Interpolator.
CLK	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the shift register on the CLK rising edge. This input is a high impedance CMOS input.
DATA	Serial Data Input. The serial data is loaded MSB first with the three LSBs being the control bits. This input is a high impedance CMOS input.
LE	Load Enable, CMOS Input. When LE goes high, the data stored in the shift registers is loaded into one of the seven latches, the latch being selected using the control bits.
R_{SET}	Connecting a resistor between this pin and ground sets the minimum charge pump output current. The relationship between I_{CP} and R_{SET} is $I_{CPmin} = \frac{1.6875}{R_{SET}}$ Therefore, with R_{SET} = 2.7 kΩ, I_{CPmin} = 0.625 mA.
$A_{GND}2$	Ground for the IF Synthesizer.
$IF_{IN}B$	Complementary Input to the IF Prescaler.
$IF_{IN}A$	Input to the IF Prescaler. This small signal input is normally taken from the IF VCO.
DV_{DD}	Positive Power Supply for the Fractional Interpolator Section. Decoupling capacitors to the ground plane should be placed as close as possible to this pin. DV_{DD} must have the same voltage as $V_{DD}1$, $V_{DD}2$, and $V_{DD}3$.
$CP_{GND}2$	IF Charge Pump Ground.
CP_{IF}	IF Charge Pump Output. This is normally connected to a loop filter that drives the input to an external VCO.
V_P2	IF Charge Pump Power Supply. Decoupling capacitors to the ground plane should be placed as close as possible to this pin. This voltage should be greater than or equal to $V_{DD}2$.
$V_{DD}2$	Positive Power Supply for the IF Section. Decoupling capacitors to the ground plane should be placed as close as possible to this pin. $V_{DD}2$ has a value 3 V ± 10%. $V_{DD}2$ must have the same voltage as $V_{DD}1$, $V_{DD}3$, and DV_{DD}.
$V_{DD}3$	Positive Power Supply for the RF Digital Section. Decoupling capacitors to the ground plane should be placed as close as possible to this pin. $V_{DD}3$ has a value 3 V ± 10%. $V_{DD}3$ must have the same voltage as $V_{DD}1$, $V_{DD}2$, and DV_{DD}.
$V_{DD}1$	Positive Power Supply for the RF Analog Section. Decoupling capacitors to the ground plane should be placed as close as possible to this pin. $V_{DD}1$ has a value 3 V ± 10%. $V_{DD}1$ must have the same voltage as $V_{DD}2$, $V_{DD}3$, and DV_{DD}.
V_P1	RF Charge Pump Power Supply. Decoupling capacitors to the ground plane should be placed as close as possible to this pin. This voltage should be greater than or equal to $V_{DD}1$.

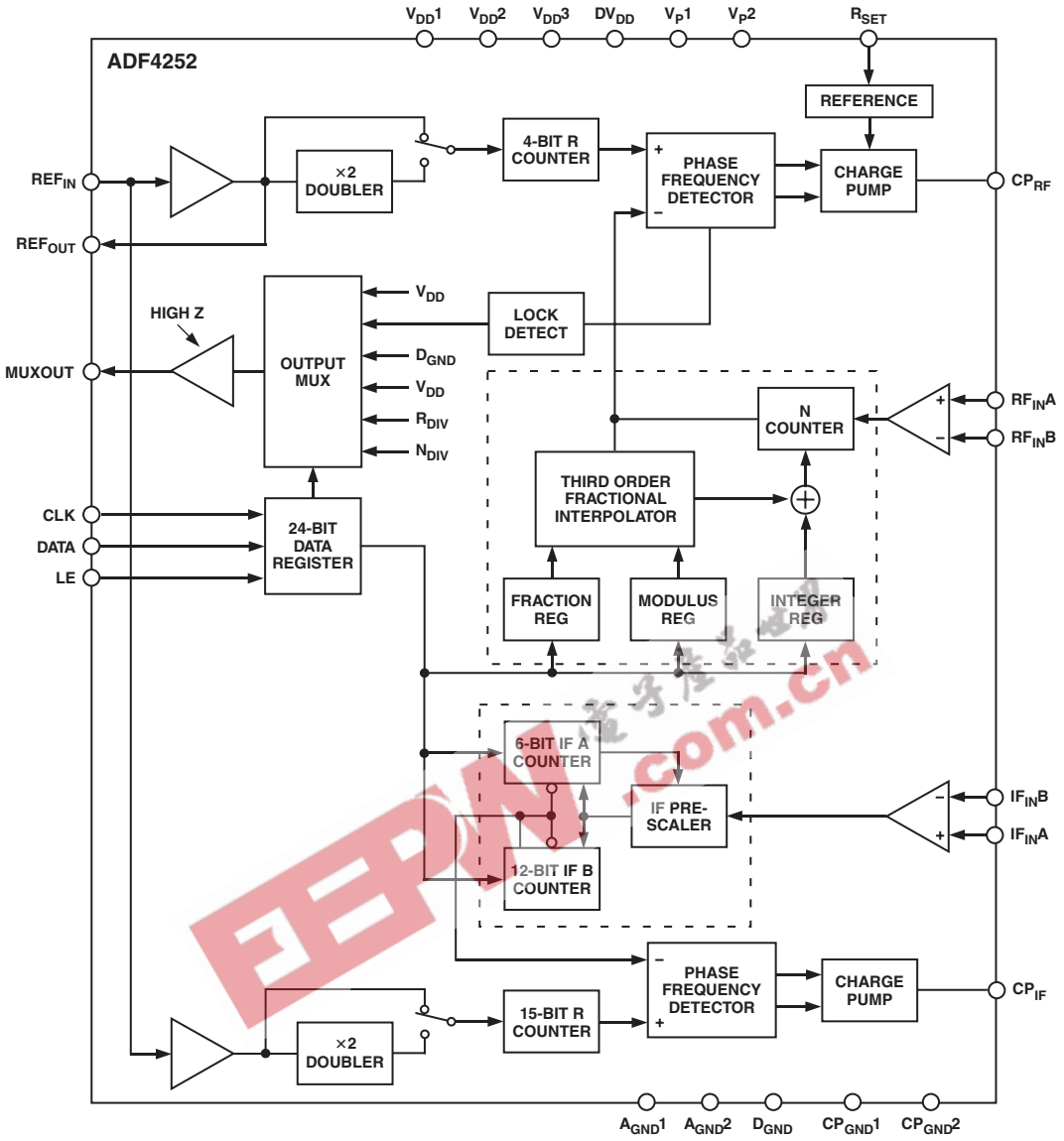
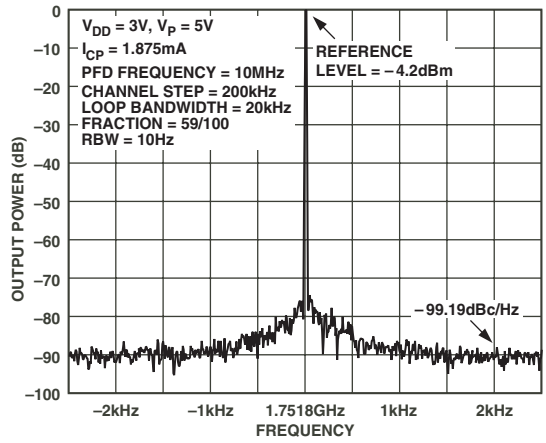
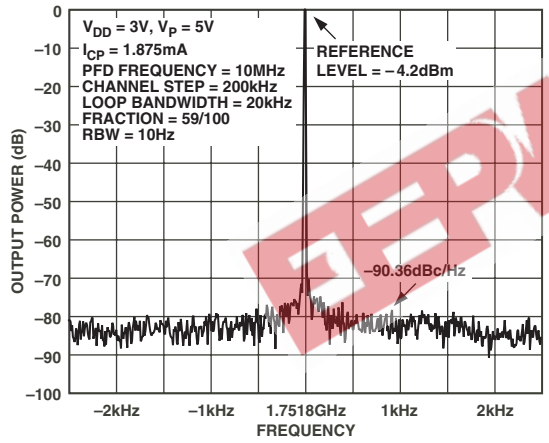


Figure 2. Detailed Functional Block Diagram

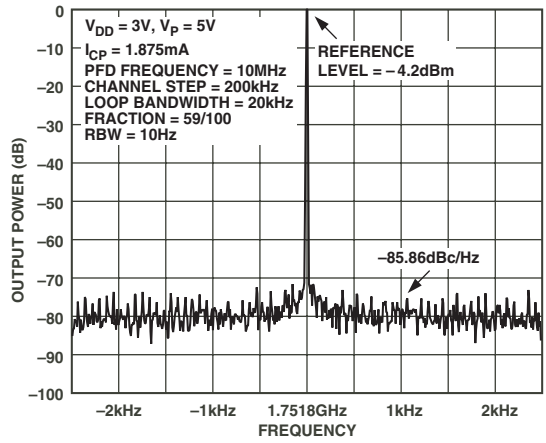
TPC plots 1 to 12 attained using EVAL-ADF4252EB1; measurements from HP8562E spectrum analyzer.



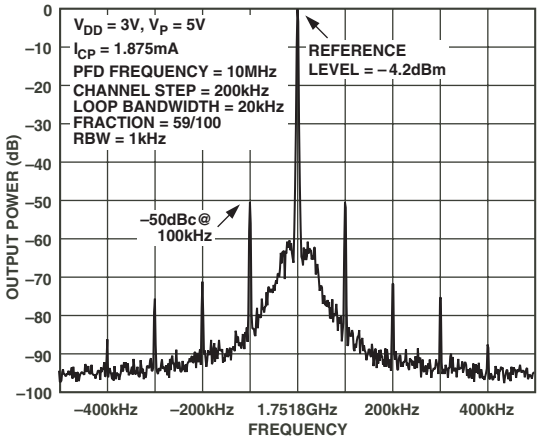
TPC 1. Phase Noise Plot, Lowest Noise Mode, 1.7518 GHz RF_{OUT}, 10 MHz PFD Frequency, 200 kHz Channel Step Resolution



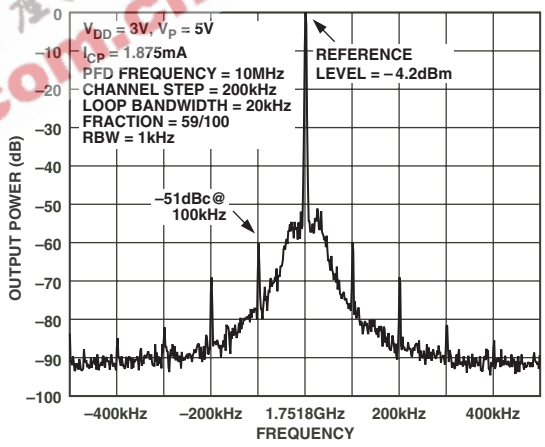
TPC 2. Phase Noise Plot, Low Noise and Spur Mode, 1.7518 GHz RF_{OUT}, 10 MHz PFD Frequency, 200 kHz Channel Step Resolution



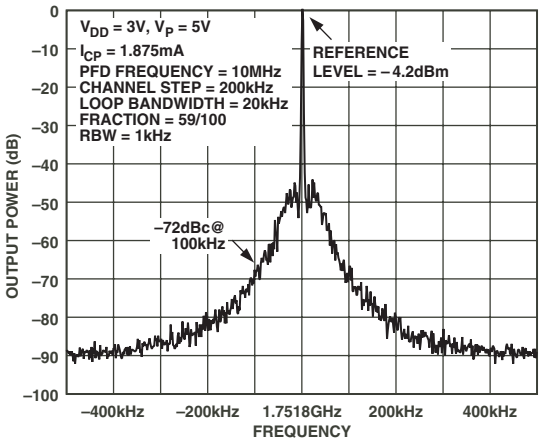
TPC 3. Phase Noise Plot, Lowest Spur Mode, 1.7518 GHz RF_{OUT}, 10 MHz PFD Frequency, 200 kHz Channel Step Resolution



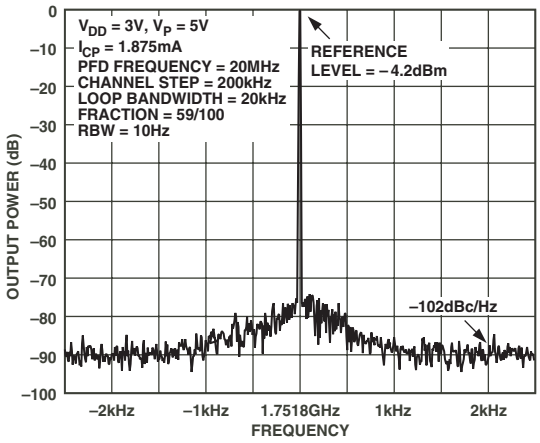
TPC 4. Spurious Plot, Lowest Noise Mode, 1.7518 GHz RF_{OUT}, 10 MHz PFD Frequency, 200 kHz Channel Step Resolution



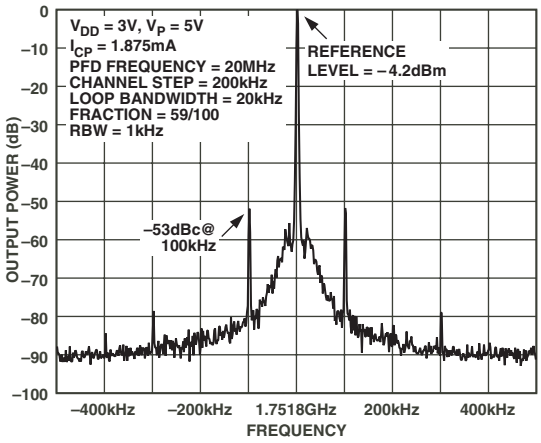
TPC 5. Spurious Plot, Low Noise and Spur Mode, 1.7518 GHz RF_{OUT}, 10 MHz PFD Frequency, 200 kHz Channel Step Resolution



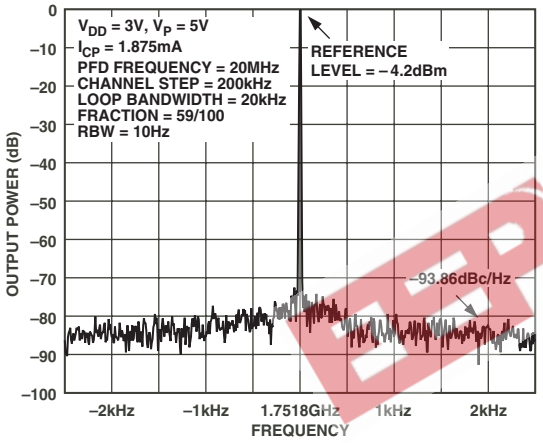
TPC 6. Spurious Plot, Lowest Spur Mode, 1.7518 GHz RF_{OUT}, 10 MHz PFD Frequency, 200 kHz Channel Step Resolution



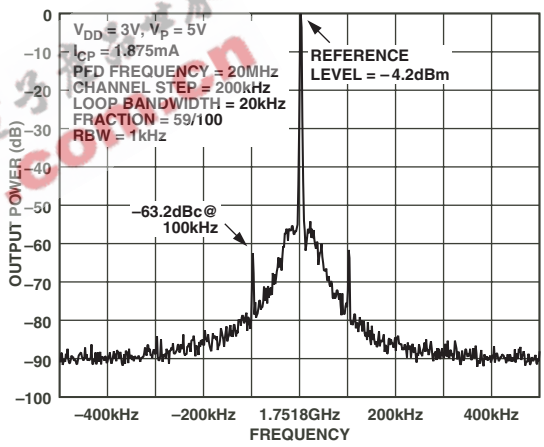
TPC 7. Phase Noise Plot, Lowest Noise Mode, 1.7518 GHz RF_{OUT}, 20 MHz PFD Frequency, 200 kHz Channel Step Resolution



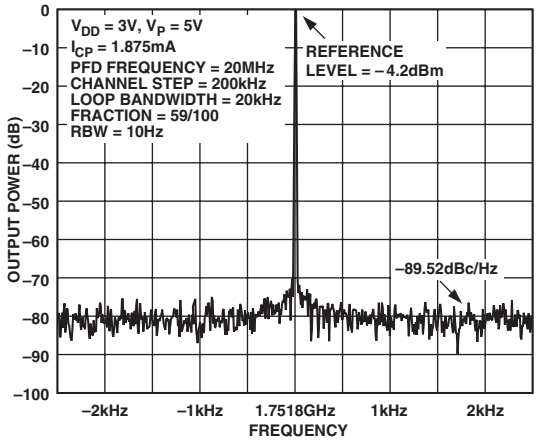
TPC 10. Spurious Plot, Lowest Noise Mode, 1.7518 GHz RF_{OUT}, 20 MHz PFD Frequency, 200 kHz Channel Step Resolution



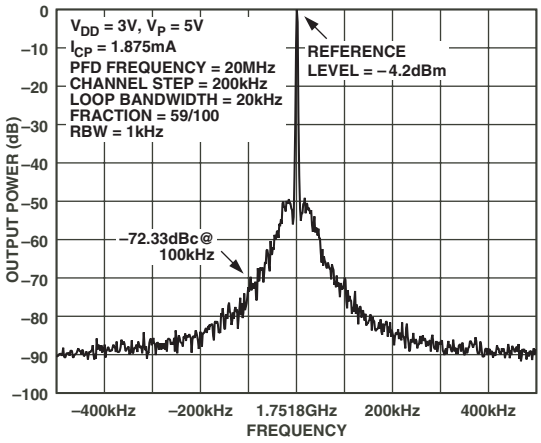
TPC 8. Phase Noise Plot, Low Noise and Spur Mode, 1.7518 GHz RF_{OUT}, 20 MHz PFD Frequency, 200 kHz Channel Step Resolution



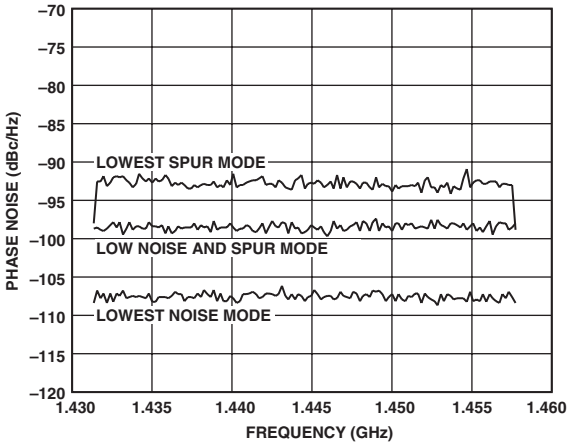
TPC 11. Spurious Plot, Low Noise and Spur Mode, 1.7518 GHz RF_{OUT}, 20 MHz PFD Frequency, 200 kHz Channel Step Resolution



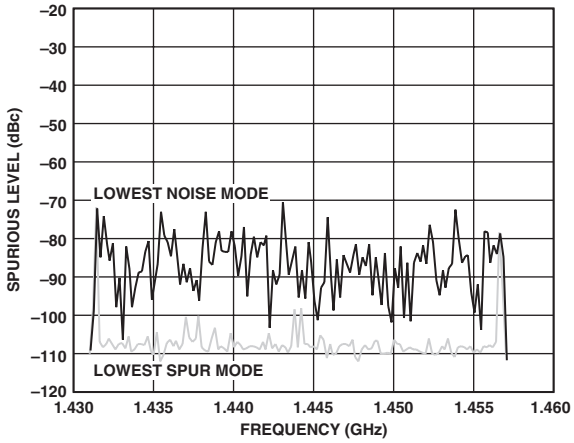
TPC 9. Phase Noise Plot, Lowest Spur Mode, 1.7518 GHz RF_{OUT}, 20 MHz PFD Frequency, 200 kHz Channel Step Resolution



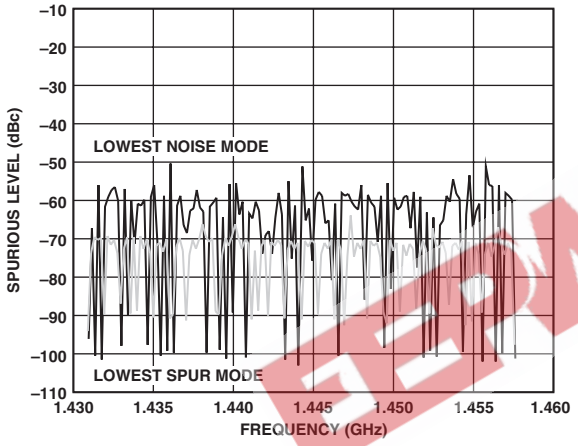
TPC 12. Spurious Plot, Lowest Spur Mode, 1.7518 GHz RF_{OUT}, 20 MHz PFD Frequency, 200 kHz Channel Step Resolution



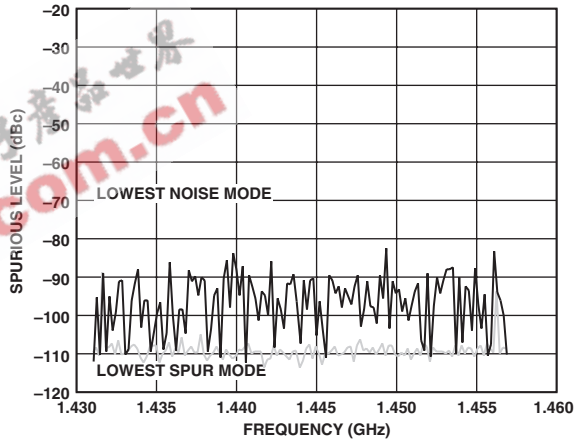
*TPC 13. In-Band Phase Noise vs. Frequency**



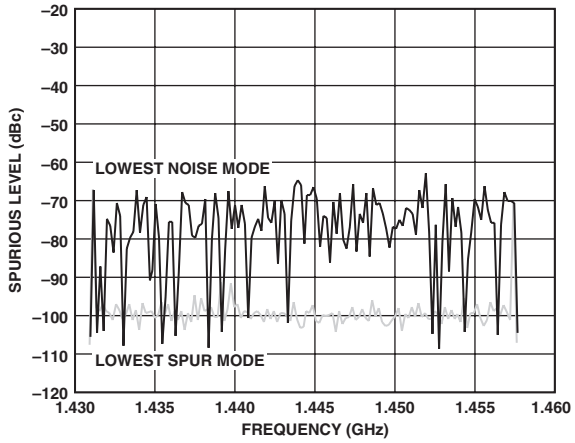
*TPC 16. 400 kHz Spur vs. Frequency**



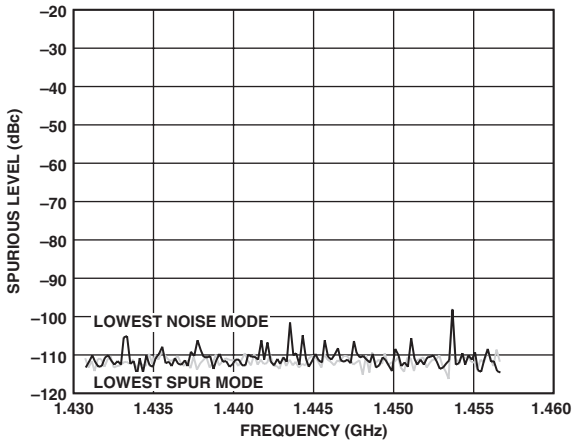
*TPC 14. 100 kHz Spur vs. Frequency**



*TPC 17. 600 kHz Spur vs. Frequency**

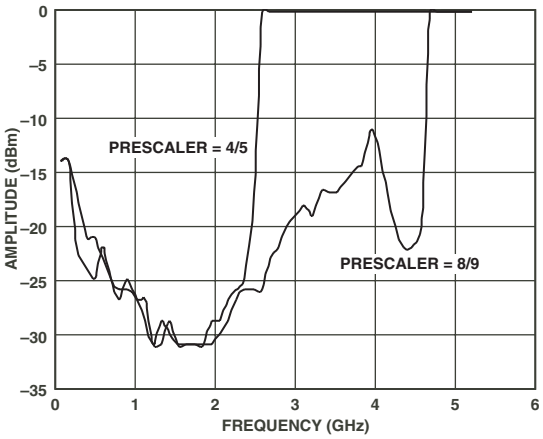


*TPC 15. 200 kHz Spur vs. Frequency**

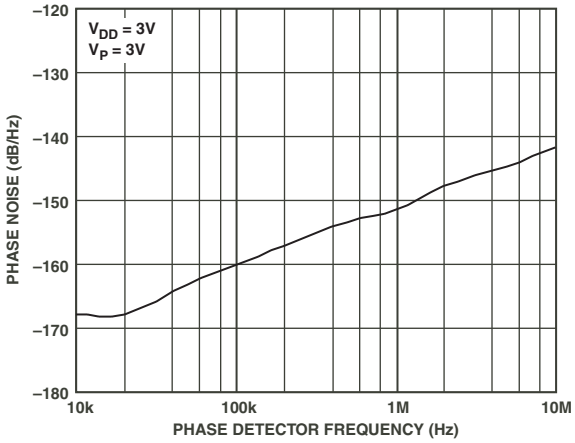


*TPC 18. 3 MHz Spur vs. Frequency**

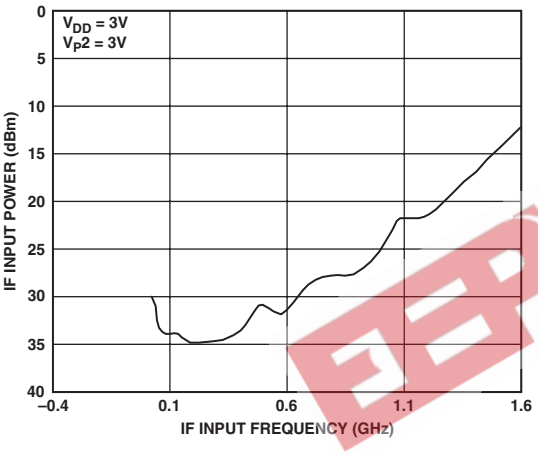
*Across all fractional channel steps from f = 0/130 to f = 129/130.
RF_{OUT} = 1.45 GHz, Int Reg = 55, Ref = 26 MHz, and LBW = 40 kHz. Plots attained using EVAL-ADF4252EB2 evaluation board.



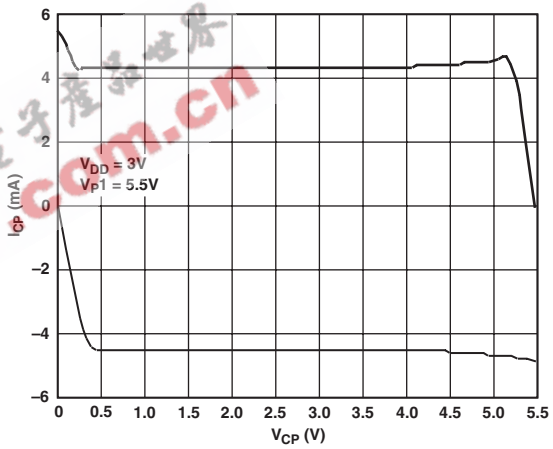
TPC 19. RF Input Sensitivity



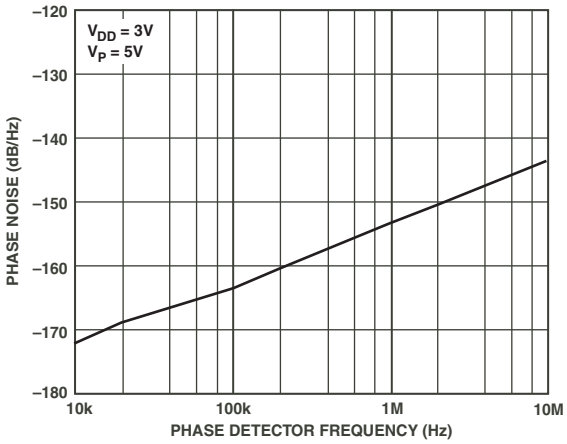
TPC 22. Phase Noise (Referred to CP Output) vs. PFD Frequency, IF Side



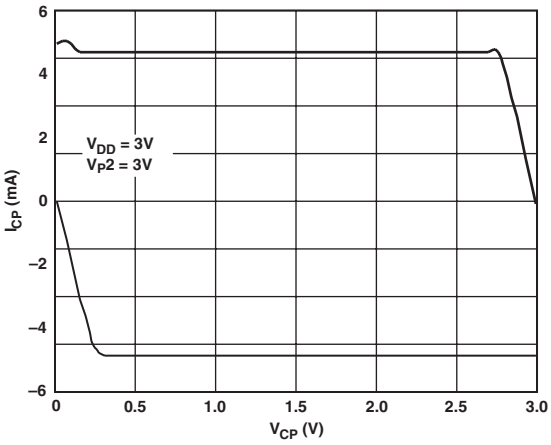
TPC 20. IF Input Sensitivity



TPC 23. RF Charge Pump Output Characteristics



TPC 21. Phase Noise (Referred to CP Output) vs. PFD Frequency, RF Side



TPC 24. IF Charge Pump Output Characteristics

CIRCUIT DESCRIPTION

Reference Input Section

The reference input stage is shown in Figure 3. SW1 and SW2 are normally closed switches. SW3 is normally open. When power-down is initiated, SW3 is closed and SW1 and SW2 are opened. This ensures that there is no loading of the REF_{IN} pin on power-down.

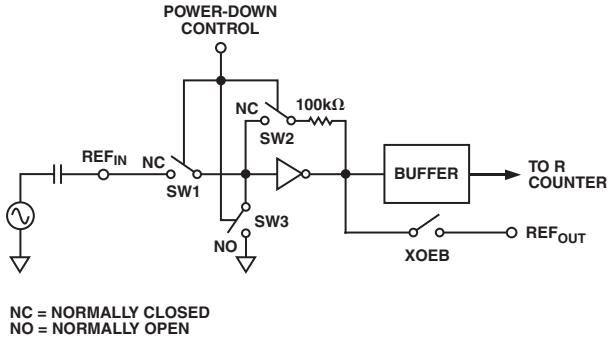


Figure 3. Reference Input Stage

RF and IF Input Stage

The RF input stage is shown in Figure 4. The IF input stage is the same. It is followed by a two-stage limiting amplifier to generate the CML clock levels needed for the N counter.

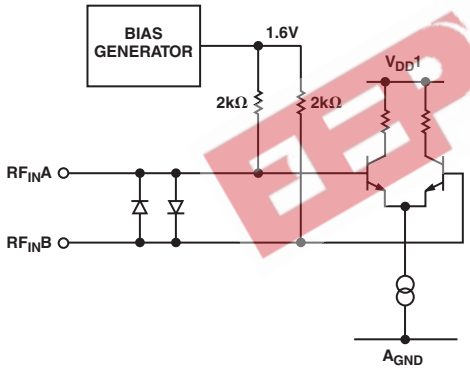


Figure 4. RF Input Stage

RF INT Divider

The RF INT CMOS counter allows a division ratio in the PLL feedback counter. Division ratios from 31 to 255 are allowed.

INT, FRAC, MOD, and R Relationship

The INT, FRAC, and MOD values, in conjunction with the RF R counter, make it possible to generate output frequencies that are spaced by fractions of the RF phase frequency detector (PFD). The equation for the RF VCO frequency (RF_{OUT}) is

$$RF_{OUT} = F_{PFD} \times \left(INT + \frac{FRAC}{MOD} \right) \quad (1)$$

where RF_{OUT} is the output frequency of external voltage controlled oscillator (VCO).

$$F_{PFD} = REF_{IN} \times \frac{(1+D)}{R} \quad (2)$$

REF_{IN} = the reference input frequency, D = RF REF_{IN} doubler bit, R = the preset divide ratio of the binary 4-bit programmable reference counter (1 to 15), INT = the preset divide ratio of the binary 8-bit counter (31 to 255), MOD = the preset modulus ratio of binary 12-bit programmable FRAC counter (2 to 4095), and $FRAC$ = the preset fractional ratio of the binary 12-bit programmable FRAC counter (0 to MOD).

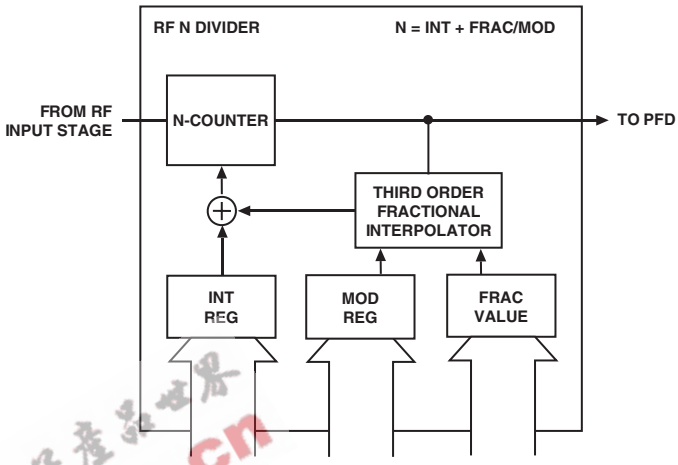


Figure 5. N Counter

RF R Counter

The 4-bit RF R counter allows the input reference frequency (REF_{IN}) to be divided down to produce the reference clock to the RF PFD. Division ratios from 1 to 15 are allowed.

IF R Counter

The 15-bit IF R counter allows the input reference frequency (REF_{IN}) to be divided down to produce the reference clock to the IF PFD. Division ratios from 1 to 32767 are allowed.

IF Prescaler (P/P + 1)

The dual modulus IF prescaler (P/P + 1), along with the IF A and B counters, enables the large division ratio, N, to be realized (N = PB + A). Operating at CML levels, it takes the clock from the IF input stage and divides it down to a manageable frequency for the CMOS IF A and B counters.

IF A and B Counters

The IF A and B CMOS counters combine with the dual modulus IF prescaler to allow a wide ranging division ratio in the PLL feedback counter. The counters are guaranteed to work when the prescaler output is 150 MHz or less.

Pulse Swallow Function

The IF A and B counters, in conjunction with the dual modulus IF prescaler, make it possible to generate output frequencies that are spaced only by the reference frequency divided by R. See Device Programming after Initial Power-Up section for examples. The equation for the IF VCO (IF_{OUT}) frequency is

$$IF_{OUT} = \left[(P \times B) + A \right] \times F_{PFD} \quad (3)$$

where IF_{OUT} = the output frequency of the external voltage controlled oscillator (VCO), P = the preset modulus of IF dual modulus prescaler, B = the preset divide ratio of the binary 12-bit counter (3 to 4095), and A = the preset divide ratio of the binary 6-bit swallow counter (0 to 63). F_{PFD} is obtained using Equation 2.

Phase Frequency Detector (PFD) and Charge Pump
The PFD takes inputs from the R counter and N counter and produces an output proportional to the phase and frequency difference between them. Figure 6 is a simplified schematic. The

antibacklash pulse. This pulse ensures that there is no dead zone in the PFD transfer function and minimizes phase noise and reference spurs.

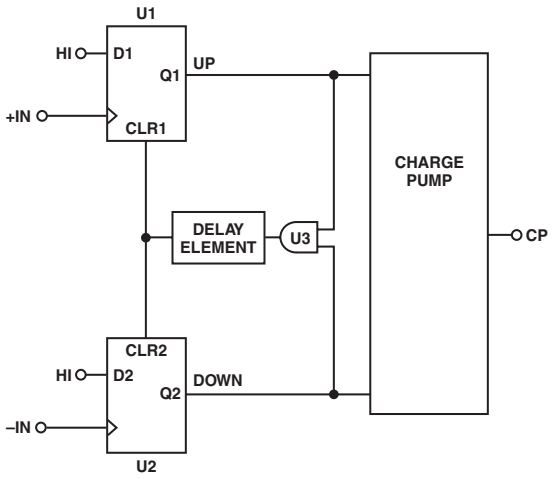


Figure 6. PFD Simplified Schematic

MUXOUT and Lock Detect
The output multiplexer on the ADF4252 allows the user to access various internal points on the chip. The state of MUXOUT is controlled by M4, M3, M2, and M1 in the master register. Table I shows the full truth table. Figure 7 shows the MUXOUT section in block diagram format.

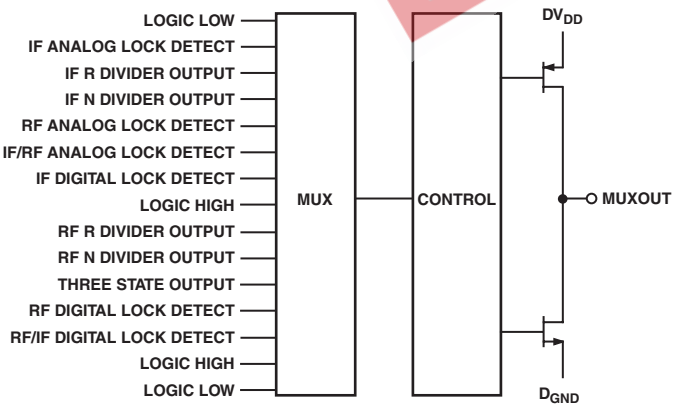


Figure 7. MUXOUT Circuit

Lock Detect
MUXOUT can be programmed for two types of lock detect: digital and analog. Digital is active high. The N-channel open-drain analog lock detect should be operated with an external pull-up resistor of 10 kΩ nominal. When lock has been detected, this output will be high with narrow low going pulses.

Input Shift Register
Data is clocked in on each rising edge of CLK. The data is clocked in MSB first. Data is transferred from the input register to one of seven latches on the rising edge of LE. The destination latch is determined by the state of the three control bits (C2, C1, and C0) in the shift register. These are the three LSBs: DB2, DB1, and DB0, as shown in Figure 1. The truth table for these bits is shown in Table I. Table II summarizes how the registers are programmed.

Table I. Control Bit Truth Table

C2	C1	C0	Data Latch
0	0	0	RF N Divider Reg
0	0	1	RF R Divider Reg
0	1	0	RF Control Reg
0	1	1	Master Reg
1	0	0	IF N Divider Reg
1	0	1	IF R Divider Reg
1	1	0	IF Control Reg

Table II. Register Summary

RF N DIVIDER REG

RESERVED	8-BIT RF INTEGER VALUE (INT)								12-BIT RF FRACTIONAL VALUE (FRAC)													CONTROL BITS		
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P1	N8	N7	N6	N5	N4	N3	N2	N1	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	C3 (0)	C2 (0)	C1 (0)

RF R DIVIDER REG

PRESCALER	RF REF_{IN} DOUBLER	4-BIT RF R COUNTER				12-BIT INTERPOLATOR MODULUS VALUE (MOD)												CONTROL BITS		
DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P3	P2	R4	R3	R2	R1	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	C3 (0)	C2 (0)	C1 (1)

RF CONTROL REG

NOISE AND SPUR SETTING 3	RESERVED			NOISE AND SPUR SETTING 2	RF CP CURRENT SETTING		RESERVED	RF PD POLARITY	NOISE AND SPUR SETTING 1	RF POWER-DOWN	RF CP THREE-STATE	RF COUNTER RESET	CONTROL BITS		
DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
N3	T3	T2	T1	N2	CP2	CP1	0	P8	N1	P6	P5	P4	C3 (0)	C2 (1)	C1 (0)

MASTER REG

MUXOUT				XO DISABLE	POWER-DOWN	CP THREE-STATE	COUNTER RESET	CONTROL BITS		
DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
M4	M3	M2	M1	P12	P11	P10	P9	C3 (0)	C2 (1)	C1 (1)

IF N DIVIDER REG

IF CP GAIN	IF PRESCALER		12-BIT IF B COUNTER											6-BIT IF A COUNTER						CONTROL BITS		
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P15	P14	P13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	A6	A5	A4	A3	A2	A1	C3 (1)	C2 (0)	C1 (0)

IF R DIVIDER REG

IF REF_{IN} DOUBLER	15-BIT IF R COUNTER														CONTROL BITS		
DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P16	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C3 (1)	C2 (0)	C1 (1)

IF CONTROL REG

RF PHASE RESYNC		RESERVED		RF PHASE RESYNC	IF CP CURRENT SETTING			IF PD POLARITY	IF LDP	IF POWER-DOWN	IF CP THREE-STATE	IF COUNTER RESET	CONTROL BITS		
DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
PR3	PR2	T8	T7	PR1	CP3	CP2	CP1	P21	P20	P19	P18	P17	C3 (1)	C2 (1)	C1 (0)

Table III. RF N Divider Register Map

RESERVED	8-BIT RF INTEGER VALUE (INT)								12-BIT RF FRACTIONAL VALUE (FRAC)												CONTROL BITS		
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P1	N8	N7	N6	N5	N4	N3	N2	N1	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	C3 (0)	C2 (0)	C1 (0)

P1	RESERVED
0	RESERVED

F12	F11	F10	.....	F3	F2	F1	FRACTIONAL VALUE (FRAC)
0	0	0	.....	0	0	0	0
0	0	0	.....	0	0	1	1
0	0	0	.....	0	1	0	2
0	0	0	.....	0	1	1	3
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
1	1	1	.....	1	0	0	4092
1	1	1	.....	1	0	1	4093
1	1	1	.....	1	1	0	4094
1	1	1	.....	1	1	1	4095

N8	N7	N6	N5	N4	N3	N2	N1	RF INTEGER VALUE (INT)*
0	0	0	1	1	1	1	1	31
0	0	1	0	0	0	0	0	32
0	0	1	0	0	0	0	1	33
0	0	1	0	0	0	1	0	34
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	0	1	253
1	1	1	1	1	1	1	0	254
1	1	1	1	1	1	1	1	255

*WHEN P = 8/9, N_{MIN} = 91

Table IV. RF R Divider Register Map

PRE-SCALER	RF REF_{IN} DOUBLER	4-BIT RF R COUNTER				12-BIT INTERPOLATOR MODULUS VALUE (MOD)												CONTROL BITS		
DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P3	P2	R4	R3	R2	R1	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	C3 (0)	C2 (0)	C1 (1)

P2	RF REF_{IN} DOUBLER
0	DISABLED
1	ENABLED

P3	RF PRESCALER
0	4/5
1	8/9

M12	M11	M10		M3	M2	M1	INTERPOLATOR MODULUS VALUE (MOD) DIVIDE RATIO
0	0	0	.....	0	1	0	2
0	0	0	.....	0	1	1	3
0	0	0	.....	1	0	0	4
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
1	1	1	.....	1	0	0	4092
1	1	1	.....	1	0	1	4093
1	1	1	.....	1	1	0	4094
1	1	1	.....	1	1	1	4095

R4	R3	R2	R1	RF R COUNTER DIVIDE RATIO
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

Table V. RF Control Register Map

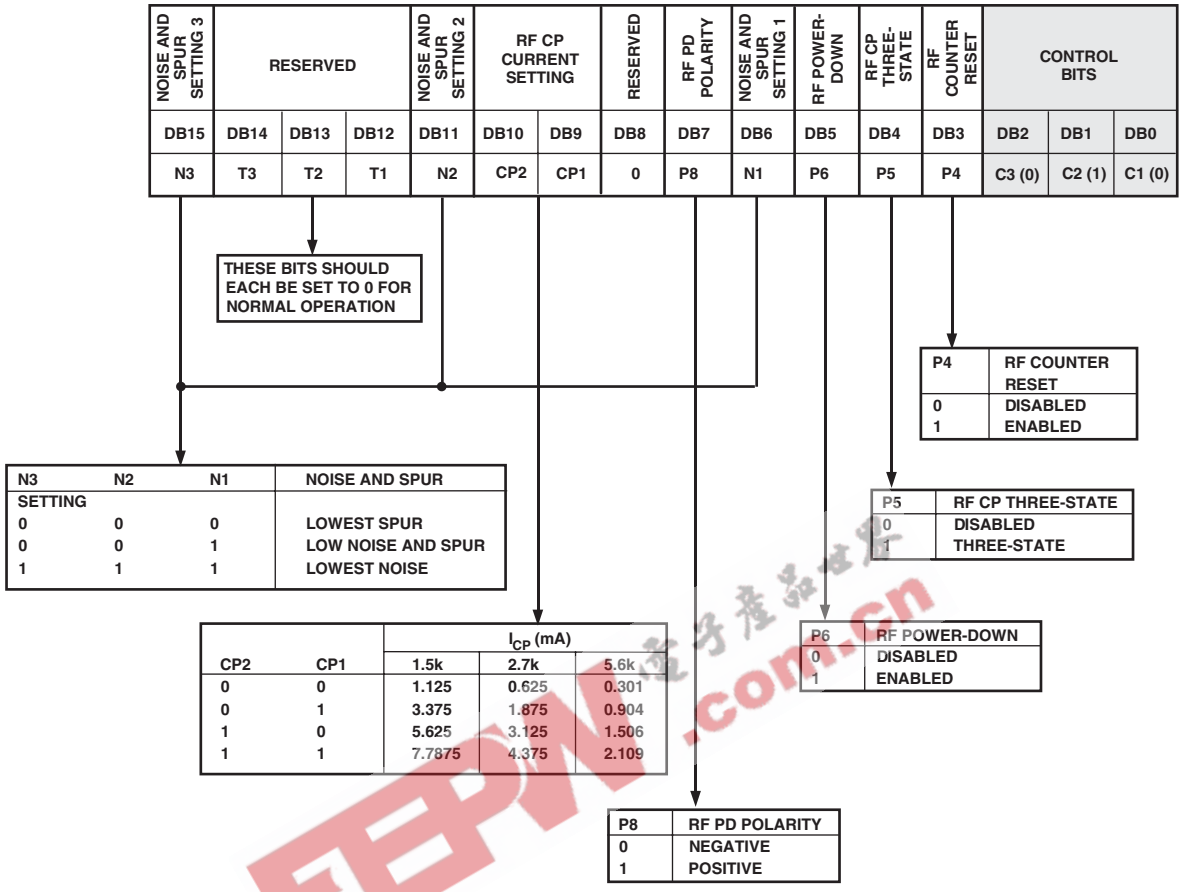


Table VI. Master Register Map

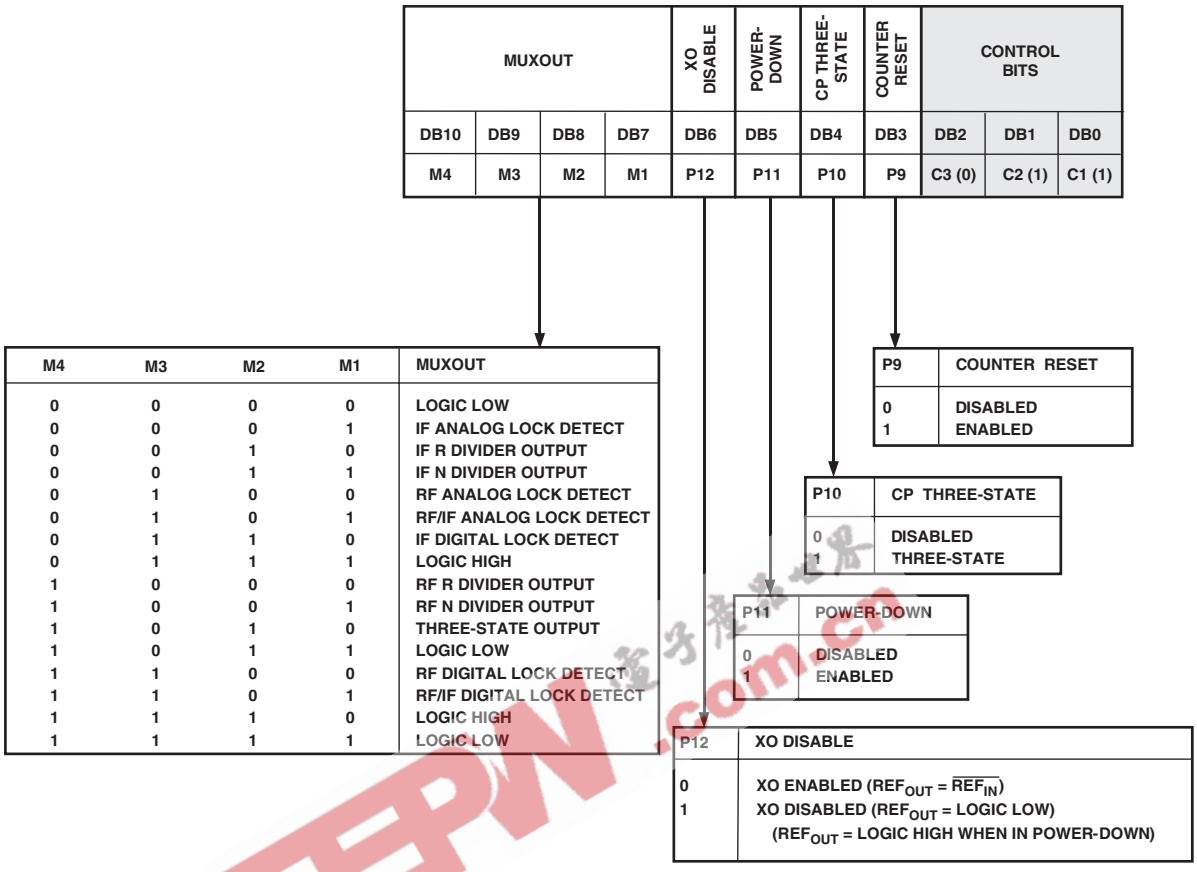


Table VII. IF N Divider Register Map

IF CP GAIN	IF PRESCALER*		12-BIT IF B COUNTER*												6-BIT IF A COUNTER*						CONTROL BITS		
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P15	P14	P13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	A6	A5	A4	A3	A2	A1	C3 (1)	C2 (0)	C1 (0)

P14	P13	PRESCALER VALUE
0	0	8/9
0	1	16/17
1	0	32/33
1	1	64/65

P15	IF CP GAIN
0	DISABLED
1	ENABLED

A6	A5	.....	A2	A1	A COUNTER DIVIDE RATIO
0	0	.....	0	0	0
0	0	.....	0	1	1
0	0	.....	1	0	2
0	0	.....	1	1	3
.	.	.....	.	.	.
.	.	.....	.	.	.
.	.	.....	.	.	.
1	1	.....	0	0	60
1	1	.....	0	1	61
1	1	.....	1	0	62
1	1	.....	1	1	63

B12	B11	B10	.....	B3	B2	B1	B COUNTER DIVIDE RATIO
0	0	0	.....	0	1	1	3
0	0	0	.....	1	0	0	4
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
1	1	1	.....	1	0	0	4092
1	1	1	.....	1	0	1	4093
1	1	1	.....	1	1	0	4094
1	1	1	.....	1	1	1	4095

*N = BP + A, P IS PRESCALER VALUE. B MUST BE GREATER THAN OR EQUAL TO A FOR CONTIGUOUS VALUES OF N, N_{MIN} IS $(P^2 - P)$.

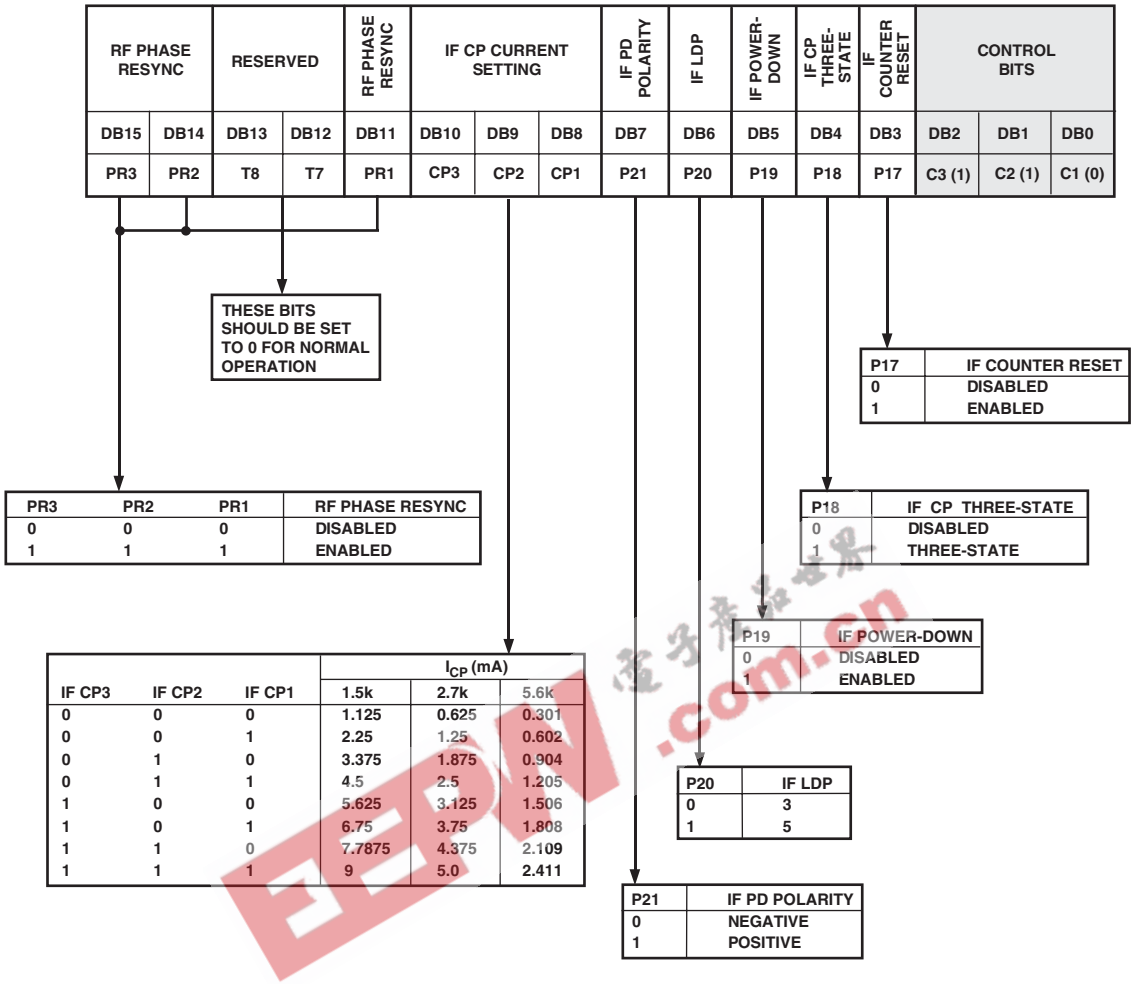
Table VIII. IF R Divider Register Map

IF REF_{IN} DOUBLER	15-BIT IF R COUNTER															CONTROL BITS		
DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P16	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C3 (1)	C2 (0)	C1 (1)

R15	R14	R13	R12	.....	R3	R2	R1	DIVIDE RATIO
0	0	0	0	.....	0	0	1	1
0	0	0	0	.....	0	1	0	2
0	0	0	0	.....	0	1	1	3
0	0	0	0	.....	1	0	0	4
.	.	.	.	.....	.	.	.	.
.	.	.	.	.....	.	.	.	.
.	.	.	.	.....	.	.	.	.
32764	1	1	1	.....	1	0	0	16380
32765	1	1	1	.....	1	0	1	16381
32766	1	1	1	.....	1	1	0	16382
32767	1	1	1	.....	1	1	1	16383

P16	IF REF_{IN} DOUBLER
0	DISABLED
1	ENABLED

Table IX. IF Control Register Map



RF N DIVIDER REGISTER
(Address R0)

With R0[2, 1, 0] set to [0, 0, 0], the on-chip RF N divider register will be programmed. Table III shows the input data format for programming this register.

8-Bit RF INT Value
These eight bits control what is loaded as the INT value. This is used to determine the overall feedback division factor. It is used in Equation 1.

12-Bit RF FRAC Value
These 12 bits control what is loaded as the FRAC value into the fractional interpolator. This is part of what determines the overall feedback division factor. It is used in Equation 1. The FRAC value must be less than or equal to the value loaded into the MOD register.

RF R DIVIDER REGISTER
(Address R1)

With R1[2, 1, 0] set to [0, 0, 1], the on-chip RF R divider register will be programmed. Table IV shows the input data format for programming this register.

RF Prescaler (P/P + 1)
The RF dual-modulus prescaler (P/P +1), along with the INT, FRAC, and MOD counters, determine the overall division ratio from the RF_{IN} to the PFD input. Operating at CML levels, it takes the clock from the RF input stage and divides it down to a manageable frequency for the CMOS counters. It is based on a synchronous 4/5 core (see Table IV).

RF REF_{IN} Doubler
Setting this bit to 0 feeds the REF_{IN} signal directly to the 4-bit RF R counter, disabling the doubler. Setting this bit to 1 multiplies the REF_{IN} frequency by a factor of 2 before feeding into the 4-bit RF R counter. When the doubler is disabled, the REF_{IN} falling edge is the active edge at the PFD input to the fractional-N synthesizer. When the doubler is enabled, both the rising and falling edges of REF_{IN} become active edges at the PFD input.

When the doubler is enabled and lowest spur mode is chosen, the in-band phase noise performance is sensitive to the REF_{IN} duty cycle. The phase noise degradation can be as much as 5 dB for REF_{IN} duty cycles outside a 45% to 55% range. The phase noise is insensitive to REF_{IN} duty cycle in the lowest noise mode and in low noise and spur mode. The phase noise is insensitive to REF_{IN} duty cycle when the doubler is disabled.

4-Bit RF R Counter
The 4-bit RF R counter allows the input reference frequency (REF_{IN}) to be divided down to produce the reference clock to the phase frequency detector (PFD). Division ratios from 1 to 15 are allowed.

12-Bit Interpolator Modulus
This programmable register sets the fractional modulus. This is the ratio of the PFD frequency to the channel step resolution on the RF output.

RF CONTROL REGISTER
(Address R2)

With R2[2, 1, 0] set to [0, 1, 0], the on-chip RF control register will be programmed. Table V shows the input data format for programming this register. Upon initialization, DB15–DB11 should all be set to 0.

Noise and Spur Setting
The noise and spur setting (R2[15, 11, 06]) is a feature that allows the user to optimize his or her design either for improved spurious performance or for improved phase noise performance. When set to [0, 0, 0], the lowest spurs setting is chosen. Here, dither is enabled. This randomizes the fractional quantization noise so that it looks more like white noise than spurious noise. This means that the part is optimized for improved spurious performance. This operation would normally be used when the PLL closed-loop bandwidth is wide[1], for fastlocking applications. A wide-loop filter does not attenuate the spurs to a level that a narrow-loop[2] bandwidth would. When this bit is set to [0, 0, 1], the low noise and spur setting is enabled. Here, dither is disabled. This optimizes the synthesizer to operate with improved noise performance. However, the spurious performance is degraded in this mode compared to lowest spurs setting. To improve noise performance even further, another option is available that reduces the phase noise. This is the lowest noise setting [1, 1, 1]. As well as disabling the dither, it also ensures the charge pump is operating in an optimum region for noise performance. This setting is extremely useful where a narrow-loop filter bandwidth is available. The synthesizer ensures extremely low noise and the filter attenuates the spurs. The Typical Performance Characteristics (TPCs) give the user an idea of the trade-off in a typical WCDMA setup for the different noise and spur settings.

RF Counter Reset
DB3 is the RF counter reset bit for the ADF4252. When this is 1, the RF synthesizer counters are held in reset. For normal operation, this bit should be 0.

RF Charge Pump Three-State
This bit puts the charge pump into three-state mode when programmed to a 1. It should be set to 0 for normal operation.

RF Power-Down
DB5 on the ADF4252 provides the programmable power-down mode. Setting this bit to a 1 will perform a power-down on both the RF and IF sections. Setting this bit to 0 will return the RF and IF sections to normal operation. While in software power-down, the part will retain all information in its registers. Only when supplies are removed will the register contents be lost.

When a power-down is activated, the following events occur:

1. All active RF dc current paths are removed.
2. The RF synthesizer counters are forced to their load state conditions.
3. The RF charge pump is forced into three-state mode.
4. The RF digital lock detect circuitry is reset.
5. The RF_{IN} input is debiased.
6. The input register remains active and capable of loading and latching data.

NOTES
[1]Wide-loop bandwidth is seen as a loop bandwidth greater than 1/10th of the RF_{OUT} channel step resolution (F_{RES}).
[2]Narrow-loop bandwidth is seen as a loop bandwidth less than 1/10th of the RF_{OUT} channel step resolution (F_{RES}).

RF Phase Detector Polarity
DB7 in the ADF4252 sets the RF phase detector polarity. When the VCO characteristics are positive, this should be set to 1. When they are negative, it should be set to 0.

RF Charge Pump Current Setting
DB9 and DB10 set the RF charge pump current setting. This should be set to whatever charge pump current the loop filter has been designed with (see Table V).

RF Test Modes
These bits should be set to 0, 0, 0 for normal operation.

MASTER REGISTER
(Address R3)
With R3[2, 1, 0] set to 0, 1, 1, the on-chip master register will be programmed. Table VI shows the input data format for programming the master register.

RF and IF Counter Reset
DB3 is the counter reset bit for the ADF4252. When this is 1, both the RF and IF R, INT, and MOD counters are held in reset. For normal operation, this bit should be 0. Upon power-up, the DB3 bit needs to be disabled, the INT counter resumes counting in "close" alignment with the R counter. (The maximum error is one prescaler cycle).

Charge Pump Three-State
This bit puts both the RF and IF charge pump into three-state mode when programmed to a 1. It should be set to 0 for normal operation.

Power-Down
R3[3] on the ADF4252 provides the programmable power-down mode. Setting this bit to a 1 will perform a power-down on both the RF and IF sections. Setting this bit to 0 will return the RF and IF sections to normal operation. While in software power-down, the part will retain all information in its registers. Only when supplies are removed will the register contents be lost.

When a power-down is activated, the following events occur:

1. All active dc current paths are removed.
2. The RF and IF counters are forced to their load state conditions.
3. The RF and IF charge pumps are forced into three-state mode.
4. The digital lock detect circuitry is reset.
5. The RF_{IN} input and IF_{IN} input are debiased.
6. The oscillator input buffer circuitry is disabled.
7. The input register remains active and capable of loading and latching data.

XO Disable
Setting this bit to 1 disables the REF_{OUT} circuitry. This will be set to 1 when using an external TCXO, VCXO, or other reference sources. This will be set to 0 when using the REF_{IN} and REF_{OUT} pins to form an oscillator circuit.

MUXOUT Control
The on-chip multiplexer is controlled by R3[10–7] on the ADF4252. Table VI shows the truth table.

If the user updates the RF control register or the IF control register, the MUXOUT contents will be lost. To retrieve the MUXOUT signal, the user must write to the master register.

Lock Detect
The digital lock detect output goes high if there are 40 successive PFD cycles with an input error of less than 15 ns. It stays high until a new channel is programmed or until the error at the PFD input exceeds 30 ns for one or more cycles. If the loop bandwidth is narrow compared to the PFD frequency, the error at the PFD inputs may drop below 15 ns for 40 cycles around a cycle slip; thus the digital lock detect may go falsely high for a short period until the error again exceeds 30 ns. In this case the digital lock detect is reliable only as a "loss of lock" indicator.

IF N DIVIDER REGISTER
(Address R4)
With R4[2, 1, 0] set to [1, 0, 0], the on-chip IF N divider register will be programmed. Table VII shows the input data format for programming this register.

IF CP Gain
When set to 1, this bit changes the IF charge pump current setting to its maximum value. When the bit is set to 0, the charge pump current reverts back to its previous state.

IF Prescaler
The dual-modulus prescaler (P/P + 1), along with the IF A and B counters, determine the overall division ratio, N, to be realized (N = PB + A) from the IF_{IN} to the IF PFD input. Operating at CML levels, it takes the clock from the IF input stage and divides it down to a manageable frequency for the CMOS counters. It is based on a synchronous 4/5 core. See Equation 2 and Table VII.

IF B and A Counter
The IF A and B counters, in conjunction with the dual modulus prescaler, make it possible to generate output frequencies that are spaced only by the reference frequency (REF_{IN}) divided by R. The equation for the IF_{OUT} VCO frequency is given in Equation 2.

IF R DIVIDER REGISTER
(Address R5)
With R5[2, 1, 0] set to [1, 0, 1], the on-chip IF R divider register will be programmed. Table VIII shows the input data format for programming this register.

IF REF_{IN} Doubler
Setting this bit to 0 feeds the REF_{IN} signal directly to the 15-bit IF R counter. Setting this bit to 1 multiplies the REF_{IN} frequency by a factor of 2 before feeding into the 15-bit IF R counter.

15-Bit IF R Counter
The 15-bit IF R counter allows the input reference frequency (REF_{IN}) to be divided down to produce the reference clock to the IF phase frequency detector (PFD). Division ratios from 1 to 32767 are allowed.

IF CONTROL REGISTER
(Address R6)
With R6[2, 1, 0] set to [1, 1, 0], the on-chip IF control register will be programmed. Table IX shows the input data format for programming this register. Upon initialization, DB15–DB11 should all be set to 0.

IF Counter Reset
DB3 is the IF counter reset bit for the ADF4252. When this is 1, the IF synthesizer counters are held in reset. For normal operation, this bit should be 0.

IF Charge Pump Three-State
This bit puts the IF charge pump into three-state mode when programmed to a 1. It should be set to 0 for normal operation.

IF Power-Down
DB5 on the ADF4252 provides the programmable power-down mode. Setting this bit to a 1 will perform a power-down on the IF section. Setting this bit to 0 will return the section to normal operation. While in software power-down, the part will retain all information in its registers. Only when supplies are removed will the register contents be lost.

When a power-down is activated, the following events occur:

1. All active IF dc current paths are removed.
2. The IF synthesizer counters are forced to their load state conditions.
3. The IF charge pump is forced into three-state mode.
4. The IF digital lock detect circuitry is reset.
5. The IF_{IN} input is debiased.
6. The input register remains active and capable of loading and latching data.

IF Phase Detector Polarity
DB7 in the ADF4252 sets the IF phase detector polarity. When the VCO characteristics are positive, this should be set to 1. When they are negative, it should be set to 0.

IF Charge Pump Current Setting
DB8, DB9, and DB10 set the IF charge pump current setting. This should be set to whatever charge pump current the loop filter has been designed with (see Table VII).

IF Test Modes
These bits should be set to [0, 0] for normal operation.

RF Phase Resync
Setting the phase resync bits [15, 14, 11] to [1, 1, 1] enables the phase resync feature. With a fractional modulus of M, a fractional-N PLL can settle with any one of (2 × π)/M valid phase offsets with respect to the reference input. This is different to integer-N (where the RF output always settles to the same static phase offset with respect to the input reference, which is zero ideally) but does not matter in most applications where all that is required is consistent frequency lock.

For applications where a consistent phase relationship between the output and reference is required (i.e., digital beamforming), the ADF4252 fractional-N synthesizer can be used with the phase resync feature enabled. This ensures that if the user programs the PLL to jump from Frequency (and Phase) A to Frequency (and Phase) B and back again to Frequency A, the PLL will return to the original phase (Phase A).

When enabled, it will activate every time the user programs Register R0 or R1 to set a new output frequency. However if a cycle slip occurs in the settling transient after the phase re-resync operation, the phase resync will be lost. This can be avoided by delaying the resync activation until the locking transient is close to its final frequency. In the IF R divider register, Bits R5[17–3] are used to set a time interval from when the new channel is programmed to the time the resync is activated. Although the time interval resolution available from the 15-bit IF R register is one REF_{IN} clock cycle, IF R should be programmed to be a value that is an integer multiple of the programmed MOD value to set a time interval that is at least as long as the RF PLL loop's lock time.

For example, if REF_{IN} = 26 MHz, MOD = 130 to give 200 kHz output steps (F_{RES}), and the RF loop has a settling time of 150 µs, then IF_R should be programmed to 3900, as

$$26\ MHz \times 150\ \mu s = 3900$$

Note that if it is required to use the IF synthesizer with phase resync enabled on the RF synth, the IF synth must operate with a PFD frequency of 26 MHz/3900. In an application where the IF synth is not required, the user should ensure that Registers R4 and R6 are not programmed so that the rest of the IF circuitry remains in power-down.

DEVICE PROGRAMMING AFTER INITIAL POWER-UP

After initially applying power to the supply pins, there are three ways to operate the device.

RF and IF Synthesizers Operational
All registers must be written to when powering up both the RF and IF synthesizer.

RF Synthesizer Operational, IF Power-Down
It is necessary to write only to Registers R3, R2, R1, and R0 when powering up the RF synthesizer only. The IF side will remain in power-down until Registers R6, R5, R4, and R3 are written to.

IF Synthesizer Operational, RF Power-Down
It is necessary to write to only Registers R6, R5, R4, and R3 when powering up the IF synthesizer only. The RF side will remain in power-down until registers R3, R2, R1, and R0 are written to.

RF Synthesizer: An Example
The RF synthesizer should be programmed as follows:

$$RF_{OUT} = \left(INT + \frac{FRAC}{MOD} \right) \times F_{PFD} \tag{4}$$

where RF_{OUT} = the RF frequency output, INT = the integer division factor, $FRAC$ = the fractionality, and MOD = the modulus.

$$F_{PFD} = \left(REF_{IN} \times \frac{1+D}{R} \right) \tag{5}$$

where REF_{IN} = the reference frequency input, D = the RF REF_{IN} doubler bit, and R = the RF reference division factor.

For example, in a GSM 1800 system where 1.8 GHz RF frequency output (RF_{OUT}) is required, a 13 MHz reference frequency input (REF_{IN}) is available and a 200 kHz channel resolution (F_{RES}) is required on the RF output.

$$MOD = \frac{REF_{IN}}{F_{RES}}$$

$$MOD = \frac{13\ MHz}{200\ kHz} = 65$$

So, from Equation 5:

$$F_{PFD} = 13\ MHz \times \frac{1+0}{1} = 13\ MHz$$

$$1.8\ GHz = 13\ MHz \times \left(INT + \frac{FRAC}{65} \right)$$

where INT = 138 and $FRAC$ = 30.

IF Synthesizer: An Example

The IF synthesizer should be programmed as follows:

$$IF_{OUT} = \left[\left(P \times B \right) + A \right] \times F_{PFD} \quad (6)$$

where IF_{OUT} = the output frequency of external voltage controlled oscillator (VCO), P = the IF prescaler, B = the B counter value, and A = the A counter value.

Equation 5 applies in this example as well.

For example, in a GSM1800 system, where 540 MHz IF frequency output (IF_{OUT}) is required, a 13 MHz reference frequency input (REF_{IN}) is available and a 200 kHz channel resolution (F_{RES}) is required on the IF output. The prescaler is set to 16/17. IF REF_{IN} doubler is disabled.

By Equation 5,

$$200\ kHz = 13\ MHz \times \frac{1+0}{R}$$

if R = 65.

By Equation 6,

$$540\ MHz = 200\ kHz \times \left[\left(16 \times B \right) + A \right]$$

if B = 168 and A = 12.

Modulus

The choice of modulus (MOD) depends on the reference signal (REF_{IN}) available and the channel resolution (F_{RES}) required at the RF output. For example, a GSM system with 13 MHz REF_{IN} would set the modulus to 65. This means that the RF output resolution (F_{RES}) is the 200 kHz (13 MHz/65) necessary for GSM.

Reference Doubler and Reference Divider

There is a reference doubler on-chip, which allows the input reference signal to be doubled. This is useful for increasing the PFD comparison frequency. Making the PFD frequency higher improves the noise performance of the system. Doubling the PFD frequency will usually result in an improvement in noise performance of 3 dB. It is important to note that the PFD cannot be operated above 30 MHz due to a limitation in the speed of the Σ-Δ circuit of the N divider.

12-Bit Programmable Modulus

Unlike most other fractional-N PLLs, the ADF4252 allows the user to program the modulus over a 12-bit range. This means that the user can set up the part in many different configurations for a specific application, when combined with the reference doubler and the 4-bit R counter.

For example, in an application that requires 1.75 GHz RF and 200 kHz channel step resolution, the system has a 13 MHz reference signal.

One possible setup is feeding the 13 MHz directly to the PFD and programming the modulus to divide by 65. This results in the required 200 kHz resolution.

Another possible setup is using the reference doubler to create 26 MHz from the 13 MHz input signal. This 26 MHz is then fed into the PFD. The modulus is now programmed to divide by 130, which also results in 200 kHz resolution. This offers superior phase noise performance over the previous setup.

The programmable modulus is also very useful for multistandard applications. If a dual-mode phone requires PDC and GSM1800 standards, the programmable modulus is a huge benefit. PDC requires 25 kHz channel step resolution, whereas GSM1800 requires 200 kHz channel step resolution. A 13 MHz reference signal could be fed directly to the PFD. The modulus would then be programmed to 520 when in PDC mode (13 MHz /520 = 25 kHz). The modulus would be reprogrammed to 65 for GSM1800 operation (13 MHz/65 = 200 kHz). It is important that the PFD frequency remains constant (13 MHz). This allows the user to design one loop filter that can be used in both setups without any stability issues. It is the ratio of the RF frequency to the PFD frequency that affects the loop design. Keeping this relationship constant, and instead changing the modulus factor, results in a stable filter.

Spurious Optimization and Fastlock

As mentioned in the Noise and Spur Setting section, the part can be optimized for spurious performance. However, in fastlocking applications, the loop bandwidth needs to be wide. Therefore, the filter does not provide much attenuation of the spurious. The programmable charge pump can be used to avoid this issue. The filter is designed for a narrow-loop bandwidth so that steady-state spurious specifications are met. This is designed using the lowest charge pump current setting. To implement fastlock during a frequency jump, the charge pump current is set to the maximum setting for the duration of the jump. This has the effect of widening the loop bandwidth, which improves lock time. When the PLL has locked to the new frequency, the charge pump is again programmed to the lowest charge pump current setting. This will narrow the loop bandwidth to its original cutoff frequency to allow for better attenuation of the spurious than the wide-loop bandwidth.

Spurious Signals—Predicting Where They Will Appear

Just as in integer-N PLLs, spurs will appear at PFD frequency offsets on either side of the carrier (and multiples of the PFD frequency). In a fractional-N PLL, spurs will also appear at frequencies equal to the RF_{OUT} channel step resolution (F_{RES}). The ADF4252 uses a high order fractional interpolator engine, which results in spurs also appearing at frequencies equal to half of the channel step resolution. For example, examine the GSM1800 setup with a 26 MHz PFD and 200 kHz resolution. Spurs will appear at ±26 MHz from the RF carrier (at an extremely low level due to filtering). Also, there will be spurs at ±200 kHz from the RF carrier. Due to the fractional interpolator architecture used in the ADF4252, spurs will also appear at

±100 kHz from the RF carrier. Harmonics of all spurs mentioned will also appear. With the lowest spur setting enabled, the spurs will be attenuated into the noise floor.

Prescaler

The prescaler limits the INT value. With P = 4/5, Nmin = 31. With P = 8/9, Nmin = 91.

The prescaler can also influence the phase noise performance. If INT < 91, a prescaler of 4/5 should be used. For applications where INT > 91, P = 8/9 should be used for optimum noise performance.

Filter Design—ADIsimPLL

A filter design and analysis program is available to help users implement their PLL design. Visit www.analog.com/pll for a free download of the ADIsimPLL software. The software designs, simulates, and analyzes the entire PLL frequency domain and time domain response. Various passive and active filter architectures are allowed.

INTERFACING

The ADF4252 has a simple SPI compatible serial interface for writing to the device. SCLK, SDATA, and LE control the data transfer. When LE (latch enable) goes high, the 24 bits that have been clocked into the input register on each rising edge of SCLK will be transferred to the appropriate latch. See Figure 1 for the Timing Diagram and Table I for the Control Bit Truth Table.

The maximum allowable serial clock rate is 20 MHz, which means that the maximum update rate possible for the device is 833 kHz or one update every 1.2 µs. This is certainly more than adequate for systems that will have typical lock times in hundreds of microseconds.

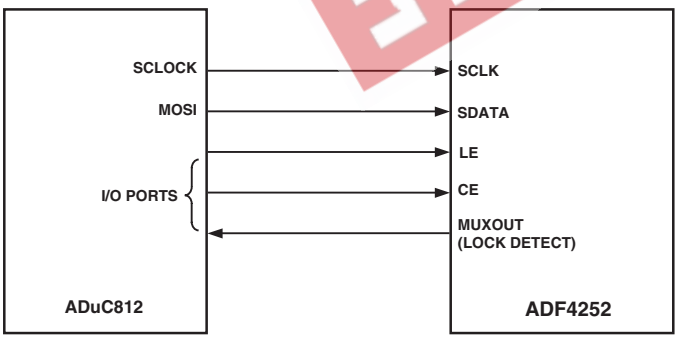


Figure 8. ADuC812 to ADF4252 Interface

ADuC812 Interface

Figure 8 shows the interface between the ADF4252 and the ADuC812 microconverter. Since the ADuC812 is based on an 8051 core, this interface can be used with any 8051 based microcontroller. The microconverter is set up for SPI master mode with CPHA = 0. To initiate the operation, the I/O port driving LE is brought low. Each latch of the ADF4252 needs (at most) a 24-bit word. This is accomplished by writing three 8-bit bytes from the microconverter to the device. When the third byte has been written, the LE input should be brought high to complete the transfer.

I/O port lines on the ADuC812 are also used to control power-down (CE input) and to detect lock (MUXOUT configured as lock detect and polled by the port input).

When operating in the mode described, the maximum SCLOCK rate of the ADuC812 is 4 MHz. This means that the maximum rate at which the output frequency can be changed will be 166 kHz.

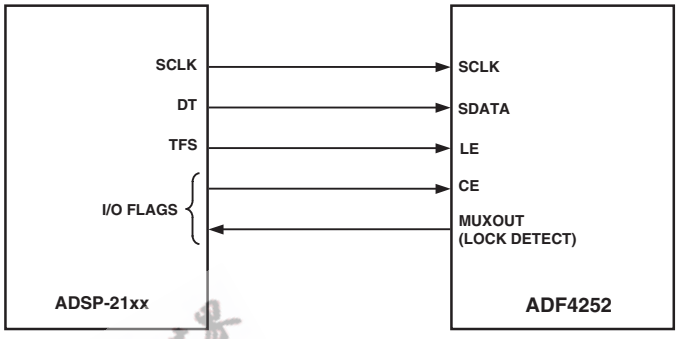


Figure 9. ADSP-21xx to ADF4252 Interface

ADSP-2181 Interface

Figure 9 shows the interface between the ADF4252 and the ADSP-21xx digital signal processor. Each latch of the ADF4252 needs (at most) a 24-bit word. The easiest way to accomplish this using the ADSP-21xx family is to use the autobuffered transmit mode of operation with alternate framing. This provides a means for transmitting an entire block of serial data before an interrupt is generated. Set up the word length for eight bits and use three memory locations for each 24-bit word. To program each 24-bit latch, store the three 8-bit bytes, enable the autobuffered mode, and then write to the transmit register of the DSP. This last operation initiates the autobuffer transfer.

PCB DESIGN GUIDELINES FOR CHIP SCALE PACKAGE

The leads on the chip scale package (CP-24) are rectangular. The printed circuit board pad for these should be 0.1 mm longer than the package land length and 0.05 mm wider than the package land width. The land should be centered on the pad. This will ensure that the solder joint size is maximized.

The bottom of the chip scale package has a central thermal pad. The thermal pad on the printed circuit board should be at least as large as this exposed pad. On the printed circuit board, there should be a clearance of at least 0.25 mm between the thermal pad and the inner edges of the pad pattern. This will ensure that shorting is avoided.

Thermal vias may be used on the printed circuit board thermal pad to improve thermal performance of the package. If vias are used, they should be incorporated in the thermal pad at 1.2 mm pitch grid. The via diameter should be between 0.3 mm and 0.33 mm, and the via barrel should be plated with 1 oz copper to plug the via.

The user should connect the printed circuit board to A_{GND}.

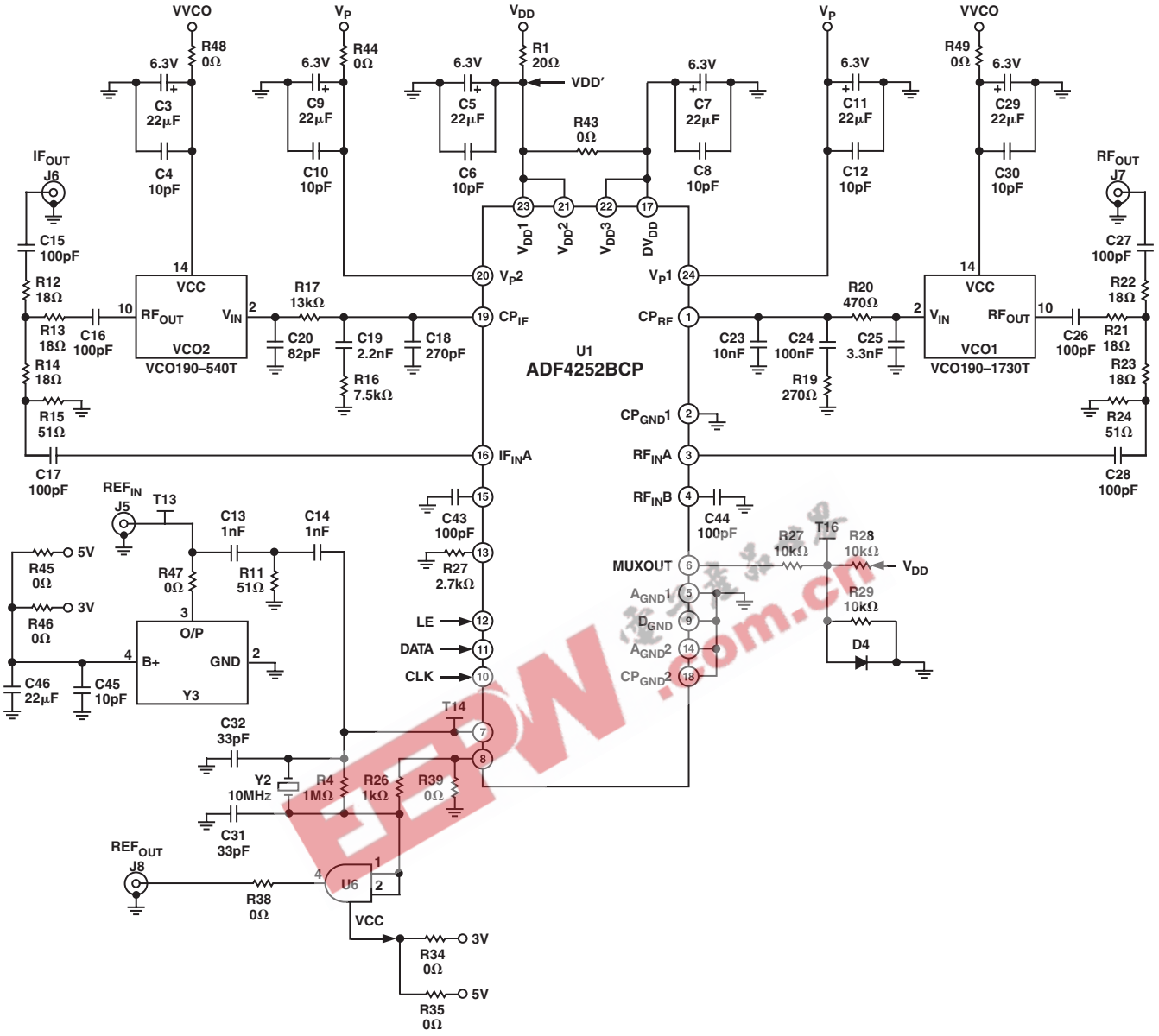
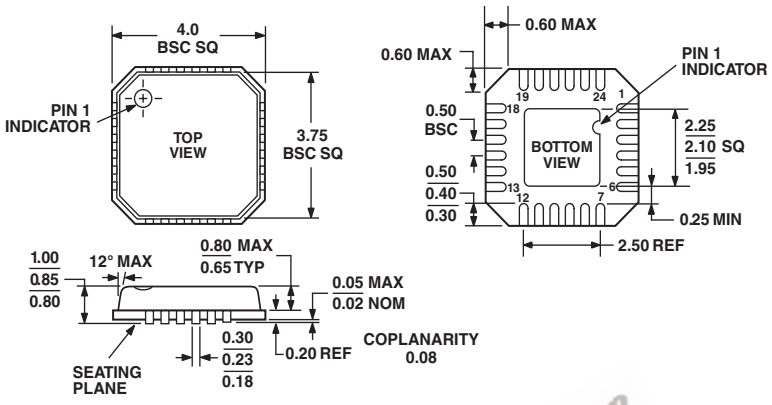


Figure 10. Typical PLL Circuit Schematic

OUTLINE DIMENSIONS

24-Lead Lead Frame Chip Scale Package [LFCSP]
(CP-24)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VGGD-2

Revision History

Location	Page
10/03—Data Sheet changed from REV. A to REV. B.	
Change to SPECIFICATIONS	2
Change to TIMING CHARACTERISTICS	3
Change to ABSOLUTE MAXIMUM RATINGS	4
Change to ORDERING GUIDE	4
Inserted Lock Detect section	22
Change to OUTLINE DIMENSIONS	27