Monolithic 16-Bit Serial/Byte DACPORT

AD660

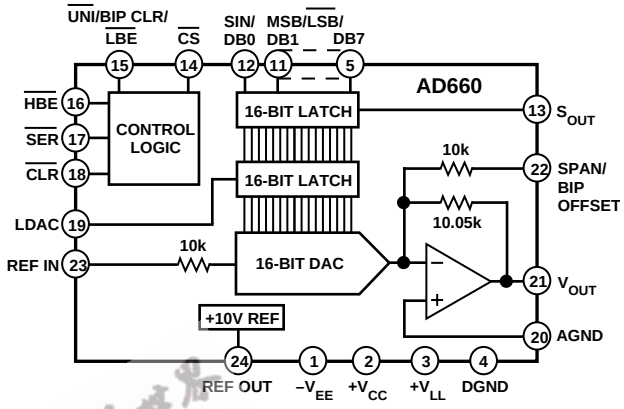
FEATURES

Complete 16-Bit D/A Function
- **On-Chip Output Amplifier**
- **On-Chip Buried Zener Voltage Reference**

±1 LSB Integral Linearity
15-Bit Monotonic over Temperature
Microprocessor Compatible
- **Serial or Byte Input**
- **Double Buffered Latches**
- **Fast (40 ns) Write Pulse**

Asynchronous Clear (to 0 V) Function
Serial Output Pin Facilitates Daisy Chaining
Unipolar or Bipolar Output
Low Glitch: 15 nV-s
Low THD+N: 0.009%

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD660 DACPORT® is a complete 16-bit monolithic D/A converter with an on-board voltage reference, double buffered latches and output amplifier. It is manufactured on Analog Devices' BiMOS II process. This process allows the fabrication of low power CMOS logic functions on the same chip as high precision bipolar linear circuitry.

The AD660's architecture ensures 15-bit monotonicity over time and temperature. Integral and differential nonlinearity is maintained at ±0.003% max. The on-chip output amplifier provides a voltage output settling time of 10 µs to within 1/2 LSB for a full-scale step.

The AD660 has an extremely flexible digital interface. Data can be loaded into the AD660 in serial mode or as two 8-bit bytes. This is made possible by two digital input pins which have dual functions. The serial mode input format is pin selectable to be MSB or LSB first. The serial output pin allows the user to daisy chain several AD660s by shifting the data through the input latch into the next DAC thus minimizing the number of control lines required to SIN, $\overline{CS}$ and LDAC. The byte mode input format is also flexible in that the high byte or low byte data can be loaded first. The double buffered latch structure eliminates data skew errors and provides for simultaneous updating of DACs in a multi-DAC system.

The AD660 is available in five grades. AN and BN versions are specified from –40°C to +85°C and are packaged in a 24-pin 300 mil plastic DIP. AR and BR versions are also specified from –40°C to +85°C and are packaged in a 24-pin SOIC. The SQ version is packaged in a 24-pin 300 mil cerdip package and is also available compliant to MIL-STD-883. Refer to the AD660/883B data sheet for specifications and test conditions.

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REV. A

PRODUCT HIGHLIGHTS

1. The AD660 is a complete 16-bit DAC, with a voltage reference, double buffered latches and output amplifier on a single chip.
2. The internal buried Zener reference is laser trimmed to 10.000 volts with a ±0.1% maximum error and a temperature drift performance of ±15 ppm/°C. The reference is available for external applications.
3. The output range of the AD660 is pin programmable and can be set to provide a unipolar output range of 0 V to +10 V or a bipolar output range of –10 V to +10 V. No external components are required.
4. The AD660 is both dc and ac specified. DC specifications include ±1 LSB INL and ±1 LSB DNL errors. AC specifications include 0.009% THD+N and 83 dB SNR.
5. The double buffered latches on the AD660 eliminate data skew errors and allow simultaneous updating of DACs in multi-DAC applications.
6. The CLEAR function can asynchronously set the output to 0 V regardless of whether the DAC is in unipolar or bipolar mode.
7. The output amplifier settles within 10 µs to ±1/2 LSB for a full-scale step and within 2.5 µs for a 1 LSB step over temperature. The output glitch is typically 15 nV-s when a full-scale step is loaded.

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AD660—SPECIFICATIONS (T_A = +25°C, V_{CC} = +15 V, V_{EE} = –15 V, V_{LL} = +5 V unless otherwise noted)

Parameter	AD660AN/AR/SQ Min	Typ	Max	AD660BN/BR Min	Typ	Max	Units
RESOLUTION	16			16			Bits
DIGITAL INPUTS (T_{MIN} to T_{MAX})							
V_{IH} (Logic "1")	2.0		5.5	*		*	Volts
V_{IL} (Logic "0")	0		0.8	*		*	Volts
I_{IH} (V_{IH} = 5 5 V)			±10			*	µA
I_{IL} (V_{IL} = 0 V)			±10			*	µA
TRANSFER FUNCTION CHARACTERISTICS[1]							
Integral Nonlinearity			±2			±1	LSB
T_{MIN} to T_{MAX}			±4			±2	LSB
Differential Nonlinearity			±2			±1	LSB
T_{MIN} to T_{MAX}			±4			±2	LSB
Monotonicity Over Temperature	14			15			Bits
Gain Error[2, 3]			±0.10			*	% of FSR
Gain Drift (T_{MIN} to T_{MAX})			25			15	ppm/°C
DAC Gain Error[4]			±0.05			*	% of FSR
DAC Gain Drift[4]			10			*	ppm/°C
Unipolar Offset			±2.5			*	mV
Unipolar Offset Drift (T_{MIN} to T_{MAX})			3			*	ppm/°C
Bipolar Zero Error			±7.5			*	mV
Bipolar Zero Error Drift (T_{MIN} to T_{MAX})			5			*	ppm/°C
REFERENCE INPUT							
Input Resistance	7	10	13	*	*	*	kΩ
Bipolar Offset Input Resistance	7	10	13	*	*	*	kΩ
REFERENCE OUTPUT							
Voltage	9.99	10.00	10.01	*	*	*	Volts
Drift			25			15	ppm/°C
External Current[5]	2	4		*	*		mA
Capacitive Load			1000			*	pF
Short Circuit Current		25			*		mA
OUTPUT CHARACTERISTICS							
Output Voltage Range							
Unipolar Configuration	0		+10	*		*	Volts
Bipolar Configuration	–10		+10	*		*	Volts
Output Current	5			*			mA
Capacitive Load			1000			*	pF
Short Circuit Current		25			*		mA
POWER SUPPLIES							
Voltage							
V_{CC}[6]	+13.5		+16.5	*		*	Volts
V_{EE}[6]	–13.5		–16.5	*		*	Volts
V_{LL}	+4.5		+5.5	*		*	Volts
Current (No Load)							
I_{CC}		+12	+18		*	*	mA
I_{EE}		–12	–18		*	*	mA
I_{LL}							
@ V_{IH}, V_{IL} = 5, 0 V		0.3	2		*	*	mA
@ V_{IH}, V_{IL} = 2.4, 0.4 V		3	7.5		*	*	mA
Power Supply Sensitivity		1	2		*	*	ppm/%
Power Dissipation (Static, No Load)		365	625		*	*	mW
TEMPERATURE RANGE							
Specified Performance (A, B)	–40		+85	*		*	°C
Specified Performance (S)	–55		+125				°C

NOTES

[1]For 16-bit resolution, 1 LSB = 0.0015% of FSR. For 15-bit resolution, 1 LSB = 0.003% of FSR. For 14-bit resolution, 1 LSB = 0.006% of FSR. FSR stands for Full-Scale Range and is 10 V in a Unipolar Mode and 20 V in Bipolar Mode.

[2]Gain error and gain drift are measured using the internal reference. The internal reference is the main contributor to gain drift. If lower gain drift is required, the AD660 can be used with a precision external reference such as the AD587, AD586 or AD688.

[3]Gain Error is measured with fixed 50 Ω resistors as shown in the Application section. Eliminating these resistors increases the gain error by 0.25% of FSR (Unipolar mode) or 0.50% of FSR (Bipolar mode).

[4]DAC Gain Error and Drift are measured with an external voltage reference. They represent the error contributed by the DAC alone, for use with an external reference.

[5]External current is defined as the current available in addition to that supplied to REF IN and SPAN/BIPOLAR OFFSET on the AD660.

[6]Operation on ±12 V supplies is possible using an external reference such as the AD586 and reducing the output range. Refer to the Internal/External Reference section.

*Indicates that the specification is the same as AD660AN/AR/SQ.

Specifications subject to change without notice.

AC PERFORMANCE CHARACTERISTICS

(With the exception of Total Harmonic Distortion + Noise and Signal-to-Noise Ratio, these characteristics are included for design guidance only and are not subject to test. THD+N and SNR are 100% tested. $T_{MIN} \le T_A \le T_{MAX}$, V_{CC} = +15 V, V_{EE} = –15 V, V_{LL} = +5 V except where noted.)

Parameter	Limit	Units	Test Conditions/Comments
Output Settling Time	13	µs max	20 V Step, T_A = +25°C
(Time to ±0.0008% FS	8	µs typ	20 V Step, T_A = +25°C
with 2 kΩ, 1000 pF Load)	10	µs typ	20 V Step, $T_{MIN} \le T_A \le T_{MAX}$
	6	µs typ	10 V Step, T_A = +25°C
	8	µs typ	10 V Step, $T_{MIN} \le T_A \le T_{MAX}$
	2.5	µs typ	1 LSB Step, $T_{MIN} \le T_A \le T_{MAX}$
Total Harmonic Distortion + Noise			
A, B, S Grade	0.009	% max	0 dB, 990.5 Hz; Sample Rate = 96 kHz; T_A = +25°C
A, B, S Grade	0.056	% max	–20 dB, 990.5 Hz; Sample Rate = 96 kHz; T_A = +25°C
A, B, S Grade	5.6	% max	–60 dB, 990.5 Hz; Sample Rate = 96 kHz; T_A = +25°C
Signal-to-Noise Ratio	83	dB min	T_A = +25°C
Digital-to-Analog Glitch Impulse	15	nV-s typ	DAC Alternately Loaded with 8000_H and $7FFF_H$
Digital Feedthrough	2	nV-s typ	DAC Alternately Loaded with 0000_H and $FFFF_H$; $\overline{CS}$ High
Output Noise Voltage Density (1 kHz – 1 MHz)	120	nV/√Hz typ	Measured at V_{OUT}; 20 V Span; Excludes Reference
Reference Noise	125	nV/√Hz typ	Measured at REF OUT

Specifications subject to change without notice.

CAUTION

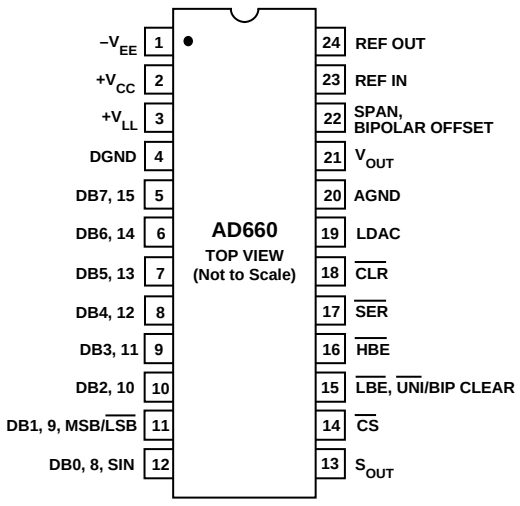
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD660 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ABSOLUTE MAXIMUM RATINGS*

V_{CC} to AGND ..... –0.3 V to +17.0 V
V_{EE} to AGND ..... +0.3 V to –17.0 V
V_{LL} to DGND .....–0.3 V to +7 V
AGND to DGND ..... ±1 V
Digital Inputs (Pins 5 through 23) to DGND ..... –1.0 V to +7.0 V
REF IN to AGND .....±10.5 V
Span/Bipolar Offset to AGND .....±10.5 V
Ref Out, V_{OUT} ..... Indefinite Short to AGND, DGND, V_{CC}, V_{EE}, and V_{LL}
Power Dissipation (Any Package)
To +60°C .....1000 mW
Derates above +60°C ..... 8.7 mW/°C
Storage Temperature .....–65°C to +150°C
Lead Temperature Range
(Soldering 10 sec) ..... +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATION



ORDERING GUIDE

Model	Temperature Range	Linearity Error Max +25°C	Linearity Error Max T_{MIN} – T_{MAX}	Gain TC max ppm/°C	Package Description	Package Option*
AD660AN	–40°C to +85°C	±2 LSB	±4 LSB	25	Plastic DIP	N-24
AD660AR	–40°C to +85°C	±2 LSB	±4 LSB	25	SOIC	R-24
AD660BN	–40°C to +85°C	±1 LSB	±2 LSB	15	Plastic DIP	N-24
AD660BR	–40°C to +85°C	±1 LSB	±2 LSB	15	SOIC	R-24
AD660SQ	–55°C to +125°C	±2 LSB	±4 LSB	25	Cerdip	Q-24
AD660SQ/883B**	–55°C to +125°C	±2 LSB	**	**	**	**

*N = Plastic DIP; Q = Cerdip; R = SOIC.
**Refer to AD660/883B military data sheet.

TIMING CHARACTERISTICS V_{CC} = +15 V, V_{EE} = –15 V, V_{LL} = +5 V, V_{HI} = 2.4 V, V_{LO} = 0.4 V

Parameter	Limit +25°C	Limit –55°C to +125°C	Units
(Figure la)			
$t_{\overline{CS}}$	40	50	ns min
t_{DS}	40	50	ns min
t_{DH}	0	10	ns min
t_{BES}	40	50	ns min
t_{BEH}	0	10	ns min
t_{LH}	80	100	ns min
t_{LW}	40	50	ns min
(Figure lb)			
t_{CLK}	80	100	ns min
t_{LO}	30	50	ns min
t_{HI}	30	50	ns min
t_{SS}	0	10	ns min
t_{DS}	40	50	ns min
t_{DH}	0	10	ns min
t_{SH}	0	10	ns min
t_{LH}	80	100	ns min
t_{LW}	40	50	ns min
(Figure lc)			
$t_{\overline{CLR}}$	80	110	ns min
t_{SET}	80	110	ns min
t_{HOLD}	0	10	ns min
(Figure ld)			
t_{PROP}	50	100	ns min
t_{DS}	50	80	ns min

Specifications subject to change without notice.

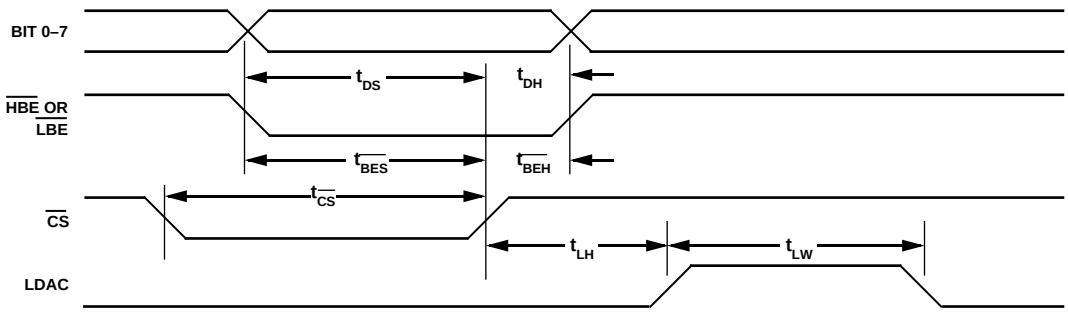


Figure 1a. AD660 Byte Load Timing

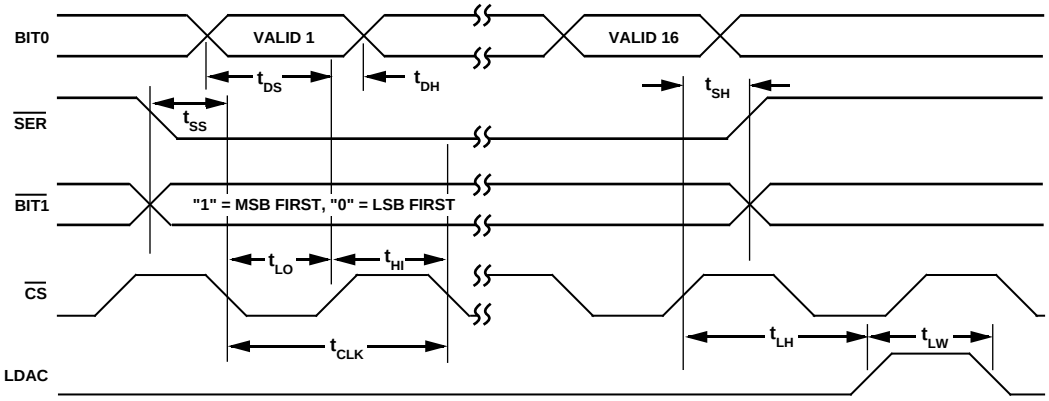


Figure 1b. AD660 Serial Load Timing

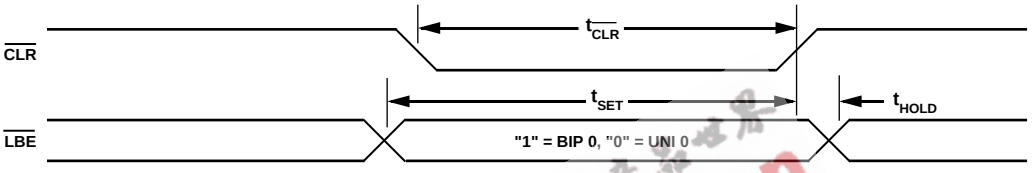


Figure 1c. Asynchronous Clear to Bipolar or Unipolar Zero

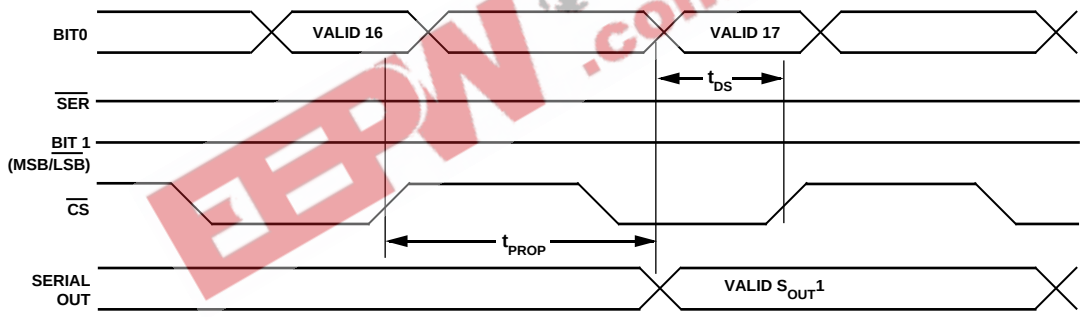


Figure 1d. Serial Out Timing

DEFINITIONS OF SPECIFICATIONS

INTEGRAL NONLINEARITY: Analog Devices defines integral nonlinearity as the maximum deviation of the actual, adjusted DAC output from the ideal analog output (a straight line drawn from 0 to FS–1 LSB) for any bit combination. This is also referred to as relative accuracy.

DIFFERENTIAL NONLINEARITY: Differential nonlinearity is the measure of the change in the analog output, normalized to full scale, associated with a 1 LSB change in the digital input code. Monotonic behavior requires that the differential linearity error be greater than or equal to –1 LSB over the temperature range of interest.

MONOTONICITY: A DAC is monotonic if the output either increases or remains constant for increasing digital inputs with the result that the output will always be a single-valued function of the input.

GAIN ERROR: Gain error is a measure of the output error between an ideal DAC and the actual device output with all 1s loaded after offset error has been adjusted out.

OFFSET ERROR: Offset error is a combination of the offset errors of the voltage-mode DAC and the output amplifier and is measured with all 0s loaded in the DAC.

BIPOLAR ZERO ERROR: When the AD660 is connected for bipolar output and 10 . . . 000 is loaded in the DAC, the deviation of the analog output from the ideal midscale value of 0 V is called the bipolar zero error.

DRIFT: Drift is the change in a parameter (such as gain, offset and bipolar zero) over a specified temperature range. The drift temperature coefficient, specified in ppm/°C, is calculated by measuring the parameter at T_{MIN}, 25°C and T_{MAX} and dividing the change in the parameter by the corresponding temperature change.

TOTAL HARMONIC DISTORTION + NOISE: Total harmonic distortion + noise (THD+N) is defined as the ratio of the square root of the sum of the squares of the values of the harmonics and noise to the value of the fundamental input frequency. It is usually expressed in percent (%).

THD+N is a measure of the magnitude and distribution of linearity error, differential linearity error, quantization error and noise. The distribution of these errors may be different, depending upon the amplitude of the output signal. Therefore, to be the most useful, THD+N should be specified for both large and small signal amplitudes.

SIGNAL-TO-NOISE RATIO: The signal-to-noise ratio is defined as the ratio of the amplitude of the output when a full-scale signal is present to the output with no signal present. This is measured in dB.

DIGITAL-TO-ANALOG GLITCH IMPULSE: This is the amount of charge injected from the digital inputs to the analog output when the inputs change state. This is measured at half scale when the DAC switches around the MSB and as many as possible switches change state, i.e., from 011 . . . 111 to 100 . . . 000.

DIGITAL FEEDTHROUGH: When the DAC is not selected (i.e., $\overline{CS}$ is held high), high frequency logic activity on the digital inputs is capacitively coupled through the device to show up as noise on the V_{OUT} pin. This noise is digital feedthrough.

THEORY OF OPERATION

The AD660 uses an array of bipolar current sources with MOS current steering switches to develop a current proportional to the applied digital word, ranging from 0 to 2 mA. A segmented architecture is used, where the most significant four data bits are thermometer decoded to drive 15 equal current sources. The lesser bits are scaled using a R-2R ladder, then applied together with the segmented sources to the summing node of the output amplifier. The internal span/bipolar offset resistor can be connected to the DAC output to provide a 0 V to +10 V span, or it can be connected to the reference input to provide a –10 V to +10 V span.

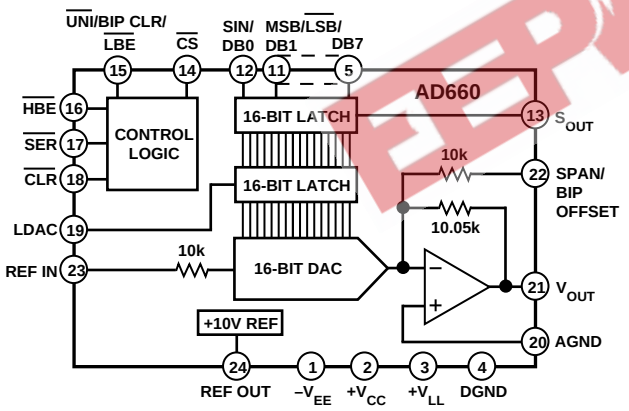


Figure 2. AD660 Functional Block Diagram

ANALOG CIRCUIT CONNECTIONS

Internal scaling resistors provided in the AD660 may be connected to produce a unipolar output range of 0 V to +10 V or a bipolar output range of –10 V to +10 V. Gain and offset drift are minimized in the AD660 because of the thermal tracking of the scaling resistors with other device components.

UNIPOLAR CONFIGURATION

The configuration shown in Figure 3a will provide a unipolar 0 V to +10 V output range. In this mode, 50 Ω resistors are tied between the span/bipolar offset terminal (Pin 22) and V_{OUT} (Pin 21), and between REF OUT (Pin 24) and REF IN (Pin 23). It is possible to use the AD660 without any external components by tying Pin 24 directly to Pin 23 and Pin 22 directly to Pin 21. Eliminating these resistors will increase the gain error by 0.25% of FSR.

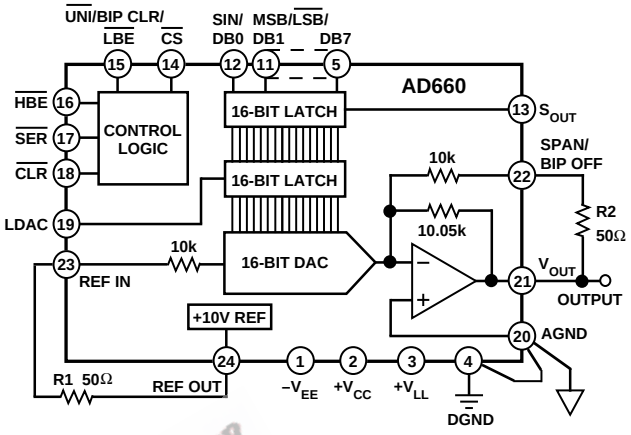


Figure 3a. 0 V to +10 V Unipolar Voltage Output

If it is desired to adjust the gain and offset errors to zero, this can be accomplished using the circuit shown in Figure 3b. The adjustment procedure is as follows:

STEP 1 . . . ZERO ADJUST

Turn all bits OFF and adjust zero trimmer, R4, until the output reads 0.000000 volts (1 LSB = 153 μV).

STEP 2 . . . GAIN ADJUST

Turn all bits ON and adjust gain trimmer, R1, until the output is 9.999847 volts. (Full scale is adjusted to 1 LSB less than the nominal full scale of 10.000000 volts).

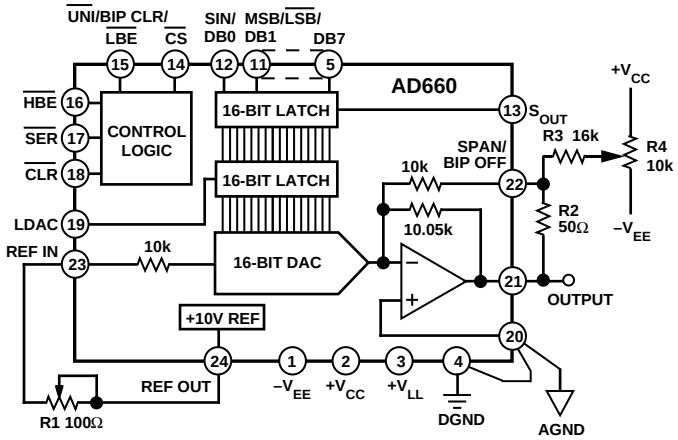


Figure 3b. 0 V to +10 V Unipolar Voltage Output with Gain and Offset Adjustment

BIPOLAR CONFIGURATION

The circuit shown in Figure 4a will provide a bipolar output voltage from –10.000000 V to +9.999694 V with positive full scale occurring with all bits ON. As in the unipolar mode, resistors R1 and R2 may be eliminated altogether to provide AD660 bipolar operation without any external components. Eliminating these resistors will increase the gain error by 0.50% of FSR in the bipolar mode.

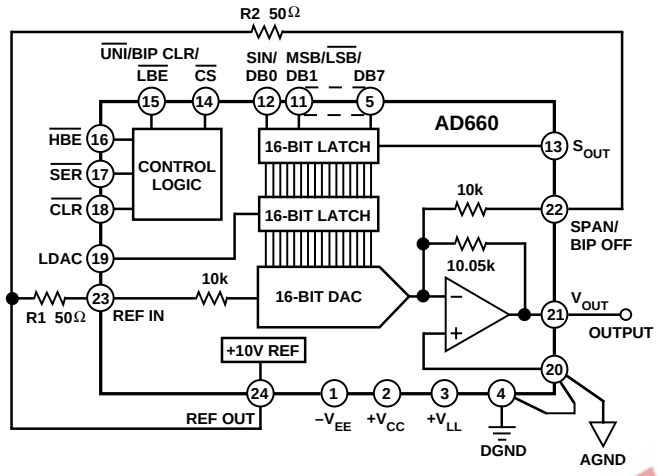


Figure 4a. ±10 V Bipolar Voltage Output

Gain offset and bipolar zero errors can be adjusted to zero using the circuit shown in Figure 4b as follows:

STEP I . . . OFFSET ADJUST
Turn OFF all bits. Adjust trimmer R2 to give 10.000000 volts output.

STEP II . . . GAIN ADJUST
Turn all bits ON and adjust R1 to give a reading of +9.999694 volts.

STEP III . . . BIPOLAR ZERO ADJUST (Optional)
In applications where an accurate zero output is required, set the MSB ON, all other bits OFF, and readjust R2 for zero volts output.

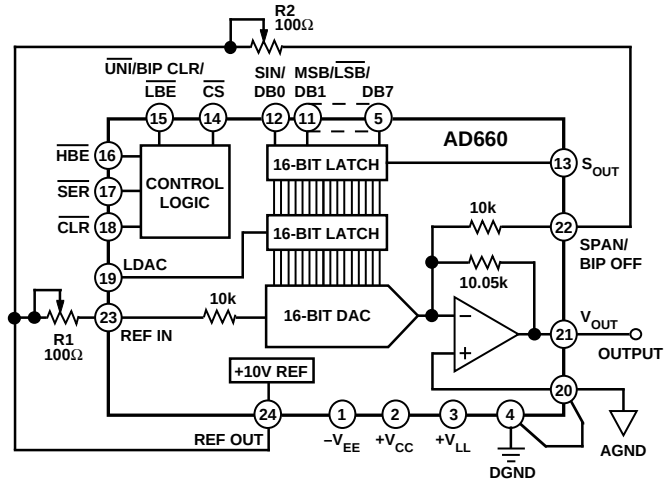


Figure 4b. ±10 V Bipolar Voltage Output with Gain and Offset Adjustment

It should be noted that using external resistors will introduce a small temperature drift component beyond that inherent in the AD660. The internal resistors are trimmed to ratio-match and temperature-track other resistors on chip, even though their absolute tolerances are ±20% and absolute temperature coefficients are approximately –50 ppm/°C . In the case that external resistors are used, the temperature coefficient mismatch between internal and external resistors, multiplied by the sensitivity of the circuit to variations in the external resistor value, will be the resultant additional temperature drift.

INTERNAL/EXTERNAL REFERENCE USE

The AD660 has an internal low noise buried Zener diode reference which is trimmed for absolute accuracy and temperature coefficient. This reference is buffered and optimized for use in a high speed DAC and will give long-term stability equal or superior to the best discrete Zener diode references. The performance of the AD660 is specified with the internal reference driving the DAC and with the DAC alone (for use with a precision external reference).

The internal reference has sufficient buffering to drive external circuitry in addition to the reference currents required for the DAC (typically 1 mA to REF IN and 1 mA to BIPOLAR OFFSET). A minimum of 2 mA is available for driving external loads. The AD660 reference output should be buffered with an external op amp if it is required to supply more than 4 mA total current. The reference is tested and guaranteed to ±0.2% max error.

It is also possible to use external references other than 10 volts with slightly degraded linearity specifications. The recommended range of reference voltages is +5 V to +10.24 V, which allows 5 V, 8.192 V and 10.24 V ranges to be used. For example, by using the AD586 5 V reference, outputs of 0 V to +5 V unipolar or ±5 V bipolar can be realized. Using the AD586 voltage reference makes it possible to operate the AD660 with ±12 V supplies with 10% tolerances.

Figure 5 shows the AD660 using the AD586 precision 5 V reference in the bipolar configuration. The highest grade AD586MN is specified with a drift of 2 ppm/°C which is a 7.5× improvement over the AD660's internal reference. This circuit includes two optional potentiometers and one optional resistor that can be used to adjust the gain, offset and bipolar zero errors in a manner similar to that described in the BIPOLAR CONFIGURATION section. Use –5.000000 V and +4.999847 as the output values.

The AD660 can also be used with the AD587 10 V reference, using the same configuration shown in Figure 5 to produce a ±10 V output. The highest grade AD587LR, N is specified at 5 ppm/°C, which is a 3× improvement over the AD660's internal reference.

Figure 6 shows the AD660 using the AD680 precision ±10 V reference, in the unipolar configuration. The highest grade AD688BQ is specified with a temperature coefficient of 1.5 ppm/°C. The ±10 V output is also ideal for providing precise biasing for the offset trim resistor R4.

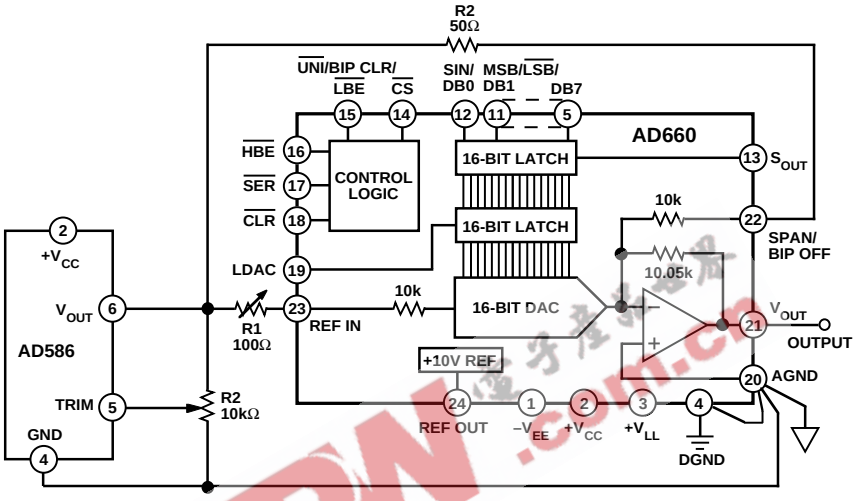


Figure 5. Using the AD660 with the AD586 5 V Reference

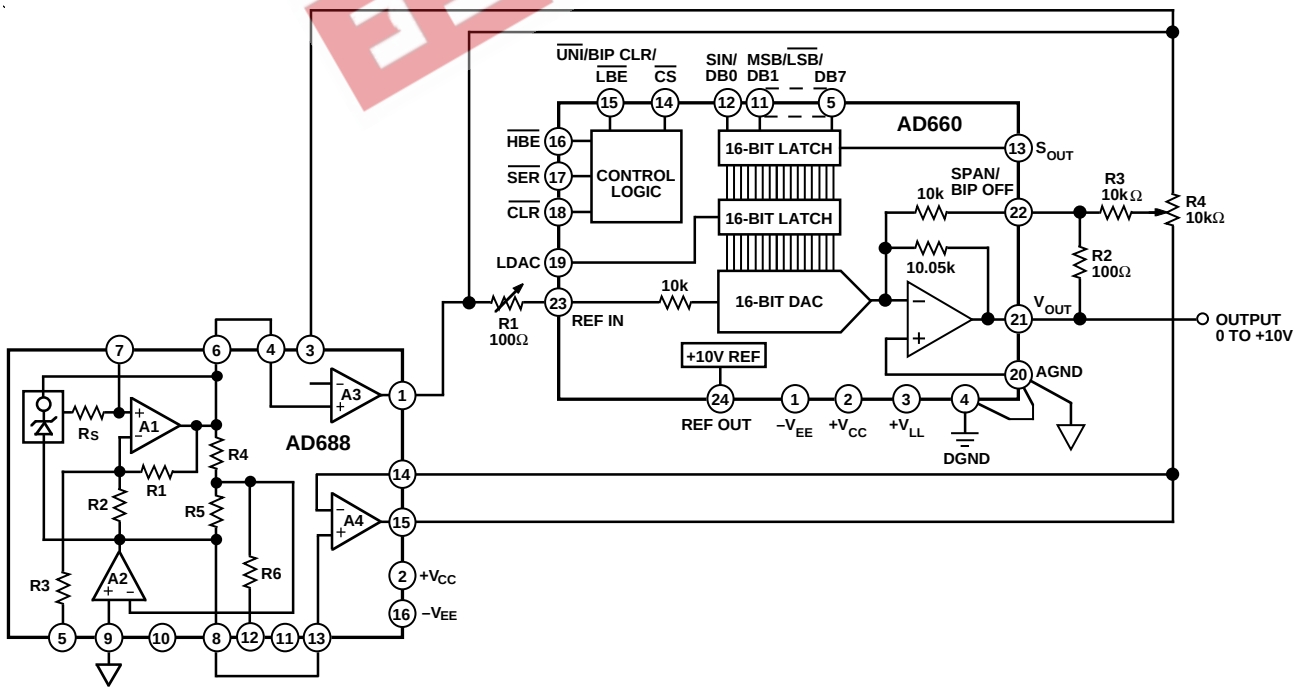
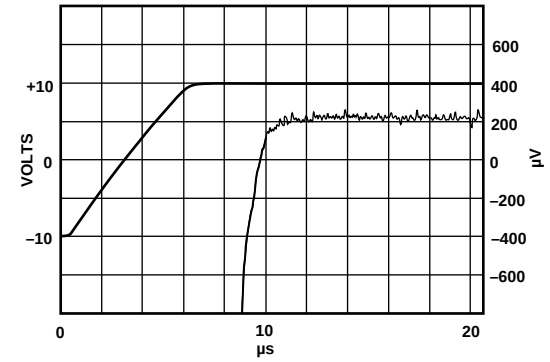


Figure 6. Using the AD660 with the AD688 High Precision ±10 V Reference

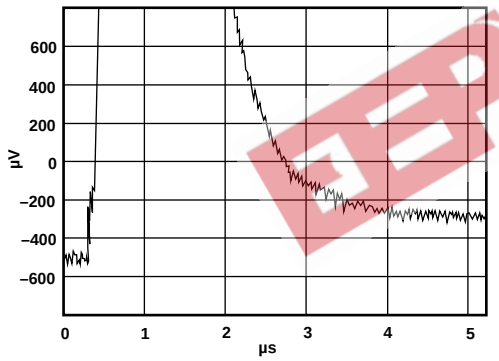
OUTPUT SETTLING AND GLITCH

The AD660's output buffer amplifier typically settles to within 0.0008% FS (1/2 LSB) of its final value in 8 µs for a full-scale step. Figures 7a and 7b show settling for a full-scale and an LSB step, respectively, with a 2 kΩ, 1000 pF load applied. The guaranteed maximum settling time at +25°C for a full-scale step is 13 µs with this load. The typical settling time for a 1 LSB step is 2.5 µs.

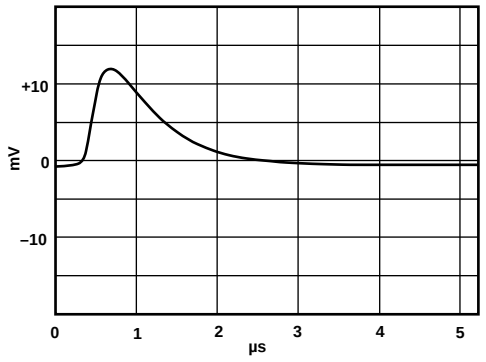
The digital-to-analog glitch impulse is specified as 15 nV-s typical. Figure 7c shows the typical glitch impulse characteristic at the code 011 . . . 111 to 100 . . . 000 transition when loading the second rank register from the first rank register.



a. –10 V to +10 V Full-Scale Step Settling



b. LSB Step Settling



c. D-to-A Glitch Impulse

Figure 7. Output Characteristics

DIGITAL CIRCUIT DETAILS

The AD660 has several "dual-use" pins which allow flexible operation while maintaining the lowest possible pin count and consequently the smallest package size. The user should, therefore, pay careful attention to the following information when applying the AD660.

Data can be loaded into the AD660 in serial or byte mode as described below.

Serial Mode Operation is enabled by bringing $\overline{\text{SER}}$ (Pin 17) low. This changes the function of DB0 (Pin 12) to that of the serial input pin, SIN. It also changes the function of DB1 (Pin 11) to a control input that tells the AD660 whether the serial data is going to be loaded MSB or $\overline{\text{LSB}}$ first.

In serial mode $\overline{\text{HBE}}$ and $\overline{\text{LBE}}$ are effectively disabled except for $\overline{\text{LBE}}$'s dual function which is to control whether the user wishes to have the asynchronous clear function go to unipolar or bipolar zero. (A low on $\overline{\text{LBE}}$, when $\overline{\text{CLR}}$ is strobed, sends the DAC output to unipolar zero, a high to bipolar zero.) The AD660 does not care about the status of HBE when in serial mode.

Data is clocked into the input register on the rising edge of $\overline{\text{CS}}$ as shown in Figure 1b. The data is then resident in the first rank latch and can be loaded into the DAC latch by taking LDAC high. This will cause the DAC to change to the appropriate output value.

It should be noted that the clear function clears the DAC latch but does not clear the first rank latch. Therefore, the data that was previously resident in the first rank latch can be reloaded simply by bringing LDAC high after the event that necessitated $\overline{\text{CLR}}$ to be strobed has ended. Alternatively, new data can be loaded into the first rank latch if desired.

The serial out pin (SOUT) can be used to daisy chain several DACs together in multi-DAC applications to minimize the number of isolators being used to cross an intrinsic safety barrier. The first rank latch simply acts like a 16-bit shift register, and repeated strobing of $\overline{\text{CS}}$ will shift the data out through SOUT and into the next DAC. Each DAC in the chain will require its own LDAC signal unless all of the DACs are to be updated simultaneously.

Byte Mode Operation is enabled simply by keeping $\overline{\text{SER}}$ high, which configures DB0–DB7 as data inputs. In this mode $\overline{\text{HBE}}$ and $\overline{\text{LBE}}$ are used to identify the data as either the high byte or low byte of the 16-bit input word. (The user can load the data, in any order, into the first rank latch.) As in the serial mode case, the status of $\overline{\text{LBE}}$, when $\overline{\text{CLR}}$ is strobed determines whether the AD660 clears to unipolar or bipolar zero. Therefore, when in byte mode, the user must take care to set $\overline{\text{LBE}}$ to the desired status before strobing $\overline{\text{CLR}}$. (In serial mode the user can simply hardware $\overline{\text{LBE}}$ to the desired state.)

NOTE: $\overline{\text{CS}}$ is edge triggered. $\overline{\text{HBE}}$, $\overline{\text{LBE}}$ and $\overline{\text{LDAC}}$ are level triggered.

AD660–Microprocessor Interface Section

AD660 TO MC68HC11 (SPI BUS) INTERFACE

The AD660 interface to the Motorola SPI (serial peripheral interface) is shown in Figure 8. The MOSI, SCK, and $\overline{SS}$ pins of the HC11 are respectively connected to the BIT0, $\overline{CS}$ and LDAC pins of the AD660. The $\overline{SER}$ pin of the AD660 is tied low causing the first rank latch to be transparent. The majority of the interfacing issues are taken care of in the software initialization. A typical routine such as the one shown below begins by initializing the state of the various SPI data and control registers.

The most significant data byte (MSBY) is then retrieved from memory and processed by the SENDAT subroutine. The $\overline{SS}$ pin is driven low by indexing into the PORTD data register and clear Bit 5. This causes the 2nd rank latch of the AD660 to become transparent. The MSBY is then set to the SPI data register where it is automatically transferred to the AD660.

The HC11 generates the requisite 8 clock pulses with data valid on the rising edges. After the most significant byte is transmitted, the least significant byte (LSBY) is loaded from memory and transmitted in a similar fashion. To complete the transfer, the LDAC pin is driven high latching the complete 16-bit word into the AD660.

```
INIT    LDAA    #$2F     ;SS = I; SCK = 0; MOSI = I
        STAA    PORTD    ;SEND TO SPI OUTPUTS
        LDAA    #$38     ;SS, SCK,MOSI = OUTPUTS
        STAA    DDRD     ;SEND DATA DIRECTION INFO
        LDAA    #$50     ;DABL INTRPTS,SPI IS MASTER & ON
        STAA    SPCR     ;CPOL=0, CPHA = 0,1MHZ BAUD RATE
NEXTPT  LDAA    MSBY     ;LOAD ACCUM W/UPPER 8 BITS
        BSR     SENDAT   ;JUMP TO DAC OUTPUT ROUTINE
        JMP     NEXTPT   ;INFINITE LOOP
SENDAT  LDY     #$1000   ;POINT AT ON-CHIP REGISTERS
        BCLR    $08,Y,$20 ;DRIVE SS (LDAC) LOW
        STAA    SPDR     ;SEND MS-BYTE TO SPI DATA REG
WAIT1   LDAA    SPSR     ;CHECK STATUS OF SPIE
        BPL     WAIT1    ;POLL FOR END OF X-MISSION
        LDAA    LSBY     ;GET LOW 8 BITS FROM MEMORY
        STAA    SPDR     ;SEND LS-BYTE TO SPI DATA REG
WAIT2   LDAA    SPSR     ;CHECK STATUS OF SPIE
        BPL     WAIT2    ;POLL FOR END OF X-MISSION
        BSET    $08,Y,$20 ;DRIV SS HIGH TO LATCH DATA
        RTS
```

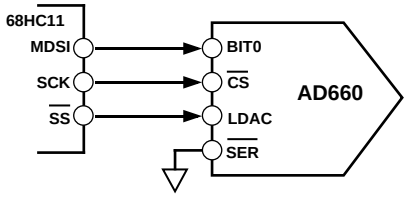


Figure 8. AD660 to 68HC11 (SPI) Interface

AD660 TO MICROWIRE INTERFACE

The flexible serial interface of the AD660 is also compatible with the National Semiconductor MICROWIRE™ interface. The MICROWIRE interface is used on microcontrollers such as the COP400 and COP800 series of processors. A generic interface to the MICROWIRE interface is shown in Figure 9. The G1, SK, And SO pins of the MICROWIRE interface are respectively connected to the LDAC, $\overline{CS}$ and BIT0 pins of the AD660.

MICROWIRE is a registered trademark of National Semiconductor.

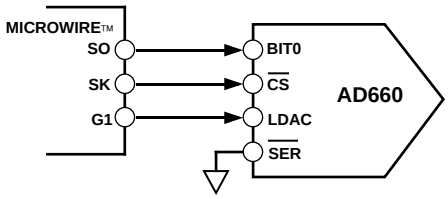


Figure 9. AD660 to MICROWIRE Interface

AD660 TO ADSP-210x FAMILY INTERFACE

The serial mode of the AD660 minimizes the number of control and data lines required to interface to digital signal processors (DSPs) such as the ADSP-210x family. The application in Figure 10 shows the interface between an ADSP-2101 and the AD660. Both the TFS pin and the DT pins of the ADSP-2101 should be connected to the $\overline{SER}$ and BIT0 pins of the AD660, respectively. An inverter is required between the SCLK output and the $\overline{CS}$ input of the AD660 in order to assure that data transmitted to the BIT0 pin is valid on the rising edge of $\overline{CS}$.

The serial port (SPORT) of the DSP should be configured for alternate framing mode so that TFS complies with the word-length framing requirement of $\overline{SER}$. Note that the INVTFS bit in the SPORT control register should be set to invert the TFS signal so that $\overline{SER}$ is the correct polarity. The LDAC signal, which must meet the minimum hold specification of t_{IH}, is easily generated by delaying the rising edge of $\overline{SER}$ with a 74HC74 flip-flop. The $\overline{CS}$ signal clocks the flip-flop resulting in a delay of approximately one $\overline{CS}$ clock cycle.

In applications such as waveform generation, accurate timing of the output samples is important to avoid noise that would be induced by jitter on the LDAC signal. In this example, the ADSP-2101 is set up to use the internal timer to interrupt the processor at the precise and desired sample rate. When the timer interrupt occurs, the processors's 16-bit data word is written to the transmit register (TXn). This causes the DSP to automatically generate the TFS signal and begin transmission of the data.

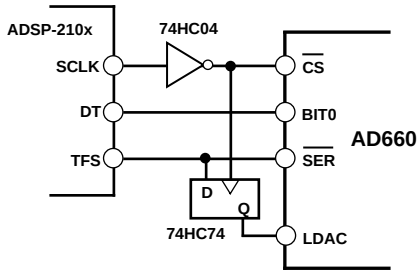


Figure 10. AD660 to ADSP-210x Interface

AD660 TO Z80 INTERFACE

Figure 11 shows a Zilog Z-80 8-bit microprocessor connected to the AD660 using the byte mode interface. The double-buffered capability of the AD660 allows the microprocessor to independently write to the low and high byte registers, and update the DAC output. Processor speeds up to 6 MHz on Z-80B require no extra wait states to interface with the AD660 using a 74ALS138 as the address decoder.

The address decoder analyzes the input-output address produced by the processor to select the function to be performed by the AD660, qualified by the coincidence of the Input-Output Request (IORQ*) and Write (WR*) pins. The least significant address bit (A0) determines if the low or high byte register of the AD660 is active. More significant address bits select between input register loading, DAC output update, and unipolar or bipolar clear.

A typical Z-80 software routine begins by writing the low byte of the desired 16-bit DAC data to address 0, followed by the high byte to address 1. The DAC output is then updated by activating LDAC with a write to address 2 (or 3). A clear to unipolar zero occurs on a write to address 4, and a clear to bipolar zero is performed by a write to address 5. The actual data written to addresses 2 through 5 is irrelevant. The decoder can easily be expanded to control as many AD660s as required.

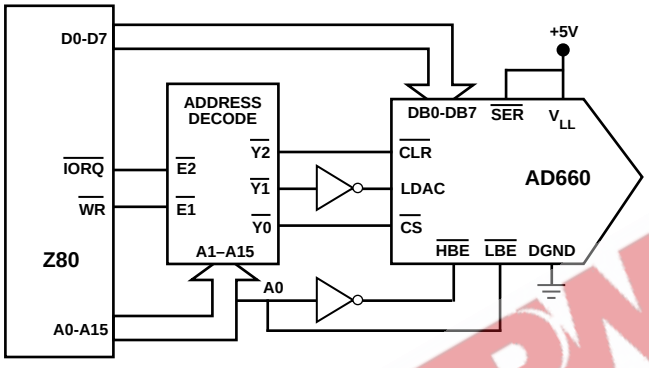


Figure 11. Connections for 8-Bit Bus Interface

NOISE

In high resolution systems, noise is often the limiting factor. A 16-bit DAC with a 10 volt span has an LSB size of 153 µV (–96 dB). Therefore, the noise floor must remain below this level in the frequency range of interest. The AD660's noise spectral density is shown in Figures 12 and 13. Figure 12 shows the DAC output noise voltage spectral density for a 20 V span excluding the reference. This figure shows the 1/f corner frequency at 100 Hz and the wideband noise to be below 120 nV/√Hz. Figure 13 shows the reference noise voltage spectral density. This figure shows the reference wideband noise to be below 125 nV/√Hz.

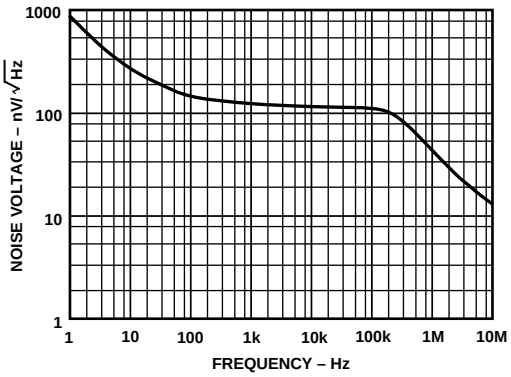


Figure 12. DAC Output Noise Voltage Spectral Density

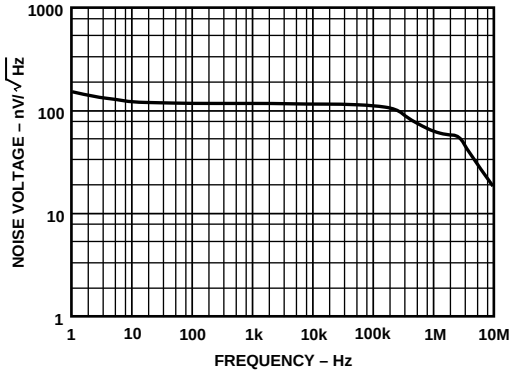


Figure 13. Reference Noise Voltage Spectral Density

BOARD LAYOUT

Designing with high resolution data converters requires careful attention to board layout. Trace impedance is the first issue. A 306 µA current through a 0.5 Ω trace will develop a voltage drop of 153 µV, which is 1 LSB at the 16-bit level for a 10 V full-scale span. In addition to ground drops, inductive and capacitive coupling need to be considered, especially when high accuracy analog signals share the same board with digital signals. Finally, power supplies need to be decoupled in order to filter out ac noise.

Analog and digital signals should not share a common path. Each signal should have an appropriate analog or digital return routed close to it. Using this approach, signal loops enclose a small area, minimizing the inductive coupling of noise. Wide PC tracks, large gauge wire, and ground planes are highly recommended to provide low impedance signal paths. Separate analog and digital ground planes should also be used, with a single interconnection point to minimize ground loops. Analog signals should be routed as far as possible from digital signals and should cross them at right angles.

One feature that the AD660 incorporates to help the user layout is that the analog pins (V_{CC}, V_{EE}, REF OUT, REF IN, SPAN/BIP OFFSET, V_{OUT} and AGND) are adjacent to help isolate analog signals from digital signals.

SUPPLY DECOUPLING

The AD660 power supplies should be well filtered, well regulated, and free from high frequency noise. Switching power supplies are not recommended due to their tendency to generate spikes which can induce noise in the analog system.

Decoupling capacitors should be used in very close layout proximity between all power supply pins and ground. A 10 µF tantalum capacitor in parallel with a 0.1 µF ceramic capacitor provides adequate decoupling. V_{CC} and V_{EE} should be bypassed to analog ground, while V_{LL} should be decoupled to digital ground.

An effort should be made to minimize the trace length between the capacitor leads and the respective converter power supply and common pins. The circuit layout should attempt to locate the AD660, associated analog circuitry and interconnections as far as possible from logic circuitry. A solid analog ground plane around the AD660 will isolate large switching ground currents. For these reasons, the use of wire wrap circuit construction is not recommended; careful printed circuit construction is preferred.

GROUNDING

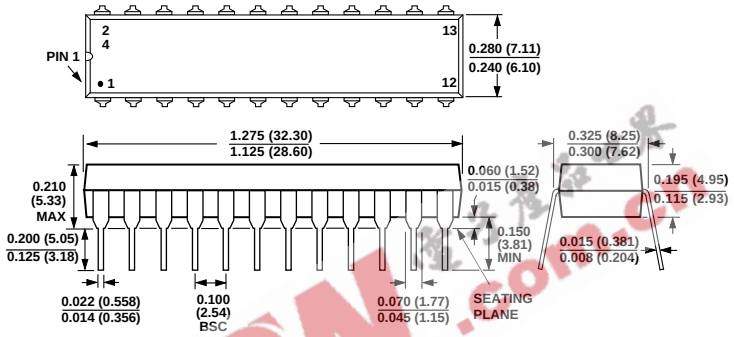
The AD660 has two pins, designated analog ground (AGND) and digital ground (DGND.) The analog ground pin is the "high quality" ground reference point for the device. Any external loads on the output of the AD660 should be returned to analog ground. If an external reference is used, this should also be returned to the analog ground.

If a single AD660 is used with separate analog and digital ground planes, connect the analog ground plane to AGND and the digital ground plane to DGND keeping lead lengths as short as possible. Then connect AGND and DGND together at the AD660. If multiple AD660s are used or the AD660 shares analog supplies with other components, connect the analog and digital returns together once at the power supplies rather than at each chip. This single interconnection of grounds prevents large ground loops and consequently prevents digital currents from flowing through the analog ground.

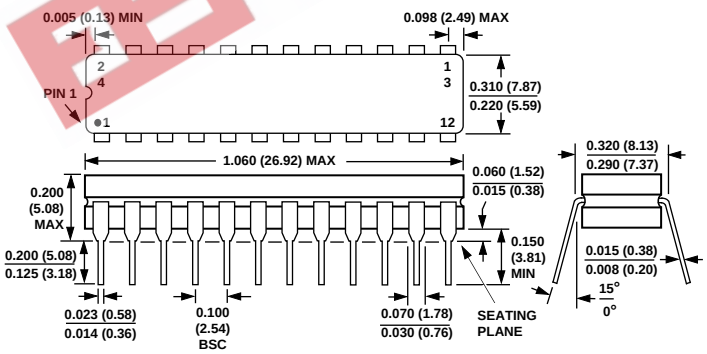
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

N-24
24-Lead Plastic DIP



Q-24
24-Lead Cerdip



R-24
24-Lead Small Outline (SOIC)