Low Noise, High Speed Amplifier for 16-Bit Systems

AD8021

FEATURES

Low noise
- **2.1 nV/√Hz input voltage noise**
- **2.1 pA/√Hz input current noise**

Custom compensation
- **Constant bandwidth from G = −1 to G = −10**

High speed
- **200 MHz (G = −1)**
- **190 MHz (G = −10)**

Low power
- **34 mW or 6.7 mA typical for 5 V supply**

Output disable feature, 1.3 mA

Low distortion
- **−93 dBc second harmonic, f_C = 1 MHz**
- **−108 dBc third harmonic, f_C = 1 MHz**

DC precision
- **1 mV maximum input offset voltage**
- **0.5 μV/°C input offset voltage drift**

Wide supply range, 5 V to 24 V

Low price

Small packaging
- **Available in SOIC-8 and MSOP-8**

APPLICATIONS

ADC preamps and drivers

Instrumentation preamps
- **Active filters**

Portable instrumentation

Line receivers

Precision instruments
- **Ultrasound signal processing**
- **High gain circuits**

GENERAL DESCRIPTION

The AD8021 is an exceptionally high performance, high speed voltage feedback amplifier that can be used in 16-bit resolution systems. It is designed to have both low voltage and low current noise (2.1 nV/√Hz typical and 2.1 pA/√Hz typical) while operating at the lowest quiescent supply current (7 mA @ ±5 V) among today's high speed, low noise op amps. The AD8021 operates over a wide range of supply voltages from ±2.25 V to ±12 V, as well as from single 5 V supplies, making it ideal for high speed, low power instruments. An output disable pin allows further reduction of the quiescent supply current to 1.3 mA.

CONNECTION DIAGRAM

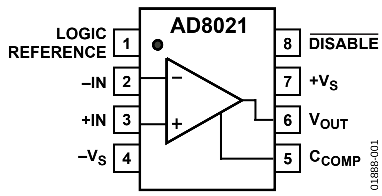

Figure 1. SOIC-8 (R-8) and MSOP-8 (RM-8)

The AD8021 allows the user to choose the gain bandwidth product that best suits the application. With a single capacitor, the user can compensate the AD8021 for the desired gain with little trade-off in bandwidth. The AD8021 is a well-behaved amplifier that settles to 0.01% in 23 ns for a 1 V step. It has a fast overload recovery of 50 ns.

The AD8021 is stable over temperature with low input offset voltage drift and input bias current drift, 0.5 μV/°C and 10 nA/°C, respectively. The AD8021 is also capable of driving a 75 Ω line with ±3 V video signals.

The AD8021 is both technically superior and priced considerably less than comparable amps drawing much higher quiescent current. The AD8021 is a high speed, general-purpose amplifier, ideal for a wide variety of gain configurations and can be used throughout a signal processing chain and in control loops. The AD8021 is available in both standard 8-lead SOIC and MSOP packages in the industrial temperature range of −40°C to +85°C.

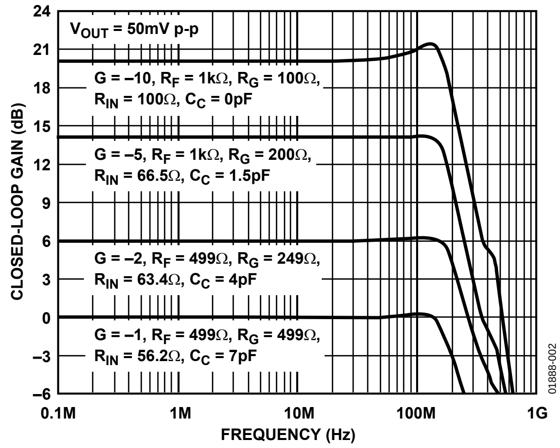

Figure 2. Small Signal Frequency Response

Rev. F

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TABLE OF CONTENTS

REVISION HISTORY

5/06—Rev. E to Rev. F
Updated Format .... Universal
Changes to General Description 1
Changes to Figure 3 7
Changes to Figure 60 19
Changes to Table 9 23

3/05—Rev. D to Rev. E
Updated Format .... Universal
Change to Figure 19 11
Change to Figure 25 12
Change to Table 7 and Table 8 22
Change to Driving 16-Bit ADCs Section 22

10/03—Rev. C to Rev. D
Updated Format .... Universal

7/03—Rev. B to Rev. C
Deleted All References to Evaluation Board .... Universal
Replaced Figure 2 5
Updated Outline Dimensions 20

2/03—Rev. A to Rev. B
Edits to Evaluation Board Applications 20
Edits to Figure 17 20

6/02—Rev. 0 to Rev. A
Edits to Specifications 2

SPECIFICATIONS

V_S = ±5 V, @ T_A = 25°C, R_L = 1 kΩ, gain = +2, unless otherwise noted.

Table 1.

Parameter	Conditions	AD8021AR/AD8021ARM			Unit
		Min	Typ	Max	
DYNAMIC PERFORMANCE					
−3 dB Small Signal Bandwidth	G = +1, C_C = 10 pF, V_O = 0.05 V p-p	355	490		MHz
	G = +2, C_C = 7 pF, V_O = 0.05 V p-p	160	205		MHz
	G = +5, C_C = 2 pF, V_O = 0.05 V p-p	150	185		MHz
	G = +10, C_C = 0 pF, V_O = 0.05 V p-p	110	150		MHz
Slew Rate, 1 V Step	G = +1, C_C = 10 pF	95	120		V/µs
	G = +2, C_C = 7 pF	120	150		V/µs
	G = +5, C_C = 2 pF	250	300		V/µs
	G = +10, C_C = 0 pF	380	420		V/µs
Settling Time to 0.01%	V_O = 1 V step, R_L = 500 Ω		23		ns
Overload Recovery (50%)	±2.5 V input step, G = +2		50		ns
DISTORTION/NOISE PERFORMANCE					
f = 1 MHz					
HD2	V_O = 2 V p-p		−93		dBc
HD3	V_O = 2 V p-p		−108		dBc
f = 5 MHz					
HD2	V_O = 2 V p-p		−70		dBc
HD3	V_O = 2 V p-p		−80		dBc
Input Voltage Noise	f = 50 kHz		2.1	2.6	nV/√Hz
Input Current Noise	f = 50 kHz		2.1		pA/√Hz
Differential Gain Error	NTSC, R_L = 150 Ω		0.03		%
Differential Phase Error	NTSC, R_L = 150 Ω		0.04		Degrees
DC PERFORMANCE					
Input Offset Voltage			0.4	1.0	mV
Input Offset Voltage Drift	T_{MIN} to T_{MAX}		0.5		µV/°C
Input Bias Current	+Input or −input		7.5	10.5	µA
Input Bias Current Drift			10		nA/°C
Input Offset Current			0.1	0.5	±µA
Open-Loop Gain		82	86		dB
INPUT CHARACTERISTICS					
Input Resistance			10		MΩ
Common-Mode Input Capacitance			1		pF
Input Common-Mode Voltage Range			−4.1 to +4.6		V
Common-Mode Rejection Ratio	V_{CM} = ±4 V	−86	−98		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing		−3.5 to +3.2	−3.8 to +3.4		V
Linear Output Current			60		mA
Short-Circuit Current			75		mA
Capacitive Load Drive for 30% Overshoot	V_O = 50 mV p-p/1 V p-p		15/120		pF
DISABLE CHARACTERISTICS					
Off Isolation	f = 10 MHz		−40		dB
Turn-On Time	V_O = 0 V to 2 V, 50% logic to 50% output		45		ns
Turn-Off Time	V_O = 0 V to 2 V, 50% logic to 50% output		50		ns
$\overline{\text{DISABLE}}$ Voltage—Off/On	$V_{DISABLE}$ − $V_{LOGIC\ REFERENCE}$		1.75/1.90		V
Enabled Leakage Current	LOGIC REFERENCE = 0.4 V		70		µA
	$\overline{\text{DISABLE}}$ = 4.0 V		2		µA

Parameter	Conditions	AD8021AR/AD8021ARM			Unit
		Min	Typ	Max	
Disabled Leakage Current	LOGIC REFERENCE = 0.4 V		30		µA
	$\overline{\text{DISABLE}}$ = 0.4 V		33		µA
POWER SUPPLY					
Operating Range		±2.25	±5	±12.0	V
Quiescent Current	Output enabled		7.0	7.7	mA
	Output disabled		1.3	1.6	mA
+Power Supply Rejection Ratio	V_{CC} = 4 V to 6 V, V_{EE} = −5 V	−86	−95		dB
−Power Supply Rejection Ratio	V_{CC} = 5 V, V_{EE} = −6 V to −4 V	−86	−95		dB

V_S = ±12 V, @ T_A = 25°C, R_L = 1 kΩ, gain = +2, unless otherwise noted.

Table 2.

Parameter	Conditions	AD8021AR/AD8021ARM			Unit
		Min	Typ	Max	
DYNAMIC PERFORMANCE					
−3 dB Small Signal Bandwidth	G = +1, C_C = 10 pF, V_O = 0.05 V p-p	520	560		MHz
	G = +2, C_C = 7 pF, V_O = 0.05 V p-p	175	220		MHz
	G = +5, C_C = 2 pF, V_O = 0.05 V p-p	170	200		MHz
	G = +10, C_C = 0 pF, V_O = 0.05 V p-p	125	165		MHz
Slew Rate, 1 V Step	G = +1, C_C = 10 pF	105	130		V/µs
	G = +2, C_C = 7 pF	140	170		V/µs
	G = +5, C_C = 2 pF	265	340		V/µs
	G = +10, C_C = 0 pF	400	460		V/µs
Settling Time to 0.01%	V_O = 1 V step, R_L = 500 Ω		21		ns
Overload Recovery (50%)	±6 V input step, G = +2		90		ns
DISTORTION/NOISE PERFORMANCE					
f = 1 MHz					
HD2	V_O = 2 V p-p		−95		dBc
HD3	V_O = 2 V p-p		−116		dBc
f = 5 MHz					
HD2	V_O = 2 V p-p		−71		dBc
HD3	V_O = 2 V p-p		−83		dBc
Input Voltage Noise	f = 50 kHz		2.1	2.6	nV/√Hz
Input Current Noise	f = 50 kHz		2.1		pA/√Hz
Differential Gain Error	NTSC, R_L = 150 Ω		0.03		%
Differential Phase Error	NTSC, R_L = 150 Ω		0.04		Degrees
DC PERFORMANCE					
Input Offset Voltage			0.4	1.0	mV
Input Offset Voltage Drift	T_{MIN} to T_{MAX}		0.2		µV/°C
Input Bias Current	+Input or −input		8	11.3	µA
Input Bias Current Drift			10		nA/°C
Input Offset Current			0.1	0.5	±µA
Open-Loop Gain		84	88		dB
INPUT CHARACTERISTICS					
Input Resistance			10		MΩ
Common-Mode Input Capacitance			1		pF
Input Common-Mode Voltage Range			−11.1 to +11.6		V
Common-Mode Rejection Ratio	V_{CM} = ±10 V	−86	−96		dB

Parameter	Conditions	AD8021AR/AD8021ARM Min	Typ	Max	Unit
OUTPUT CHARACTERISTICS					
Output Voltage Swing		−10.2 to +9.8	−10.6 to +10.2		V
Linear Output Current			70		mA
Short-Circuit Current			115		mA
Capacitive Load Drive for 30% Overshoot	V_O = 50 mV p-p/1 V p-p		15/120		pF
DISABLE CHARACTERISTICS					
Off Isolation	f = 10 MHz		−40		dB
Turn-On Time	V_O = 0 V to 2 V, 50% logic to 50% output		45		ns
Turn-Off Time	V_O = 0 V to 2 V, 50% logic to 50% output		50		ns
$\overline{\text{DISABLE}}$ Voltage—Off/On	$V_{DISABLE} - V_{LOGIC\ REFERENCE}$		1.80/1.95		V
Enabled Leakage Current	LOGIC REFERENCE = 0.4 V		70		μA
	$\overline{\text{DISABLE}}$ = 4.0 V		2		μA
Disabled Leakage Current	LOGIC REFERENCE = 0.4 V		30		μA
	$\overline{\text{DISABLE}}$ = 0.4 V		33		μA
POWER SUPPLY					
Operating Range		±2.25	±5	±12.0	V
Quiescent Current	Output enabled		7.8	8.6	mA
	Output disabled		1.7	2.0	mA
+Power Supply Rejection Ratio	V_{CC} = 11 V to 13 V, V_{EE} = −12 V	−86	−96		dB
−Power Supply Rejection Ratio	V_{CC} = 12 V, V_{EE} = −13 V to −11 V	−86	−100		dB

V_S = 5 V, @ T_A = 25°C, R_L = 1 kΩ, gain = +2, unless otherwise noted.

Table 3.

Parameter	Conditions	AD8021AR/AD8021ARM Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Small Signal Bandwidth	G = +1, C_C = 10 pF, V_O = 0.05 V p-p	270	305		MHz
	G = +2, C_C = 7 pF, V_O = 0.05 V p-p	155	190		MHz
	G = +5, C_C = 2 pF, V_O = 0.05 V p-p	135	165		MHz
	G = +10, C_C = 0 pF, V_O = 0.05 V p-p	95	130		MHz
Slew Rate, 1 V Step	G = +1, C_C = 10 pF	80	110		V/μs
	G = +2, C_C = 7 pF	110	140		V/μs
	G = +5, C_C = 2 pF	210	280		V/μs
	G = +10, C_C = 0 pF	290	390		V/μs
Settling Time to 0.01%	V_O = 1 V step, R_L = 500 Ω		28		ns
Overload Recovery (50%)	0 V to 2.5 V input step, G = +2		40		ns
DISTORTION/NOISE PERFORMANCE					
f = 1 MHz					
HD2	V_O = 2 V p-p		−84		dBc
HD3	V_O = 2 V p-p		−91		dBc
f = 5 MHz					
HD2	V_O = 2 V p-p		−68		dBc
HD3	V_O = 2 V p-p		−81		dBc
Input Voltage Noise	f = 50 kHz		2.1	2.6	nV/√Hz
Input Current Noise	f = 50 kHz		2.1		pA/√Hz

Parameter	Conditions	AD8021AR/AD8021ARM Min	Typ	Max	Unit
DC PERFORMANCE					
Input Offset Voltage			0.4	1.0	mV
Input Offset Voltage Drift	T_{MIN} to T_{MAX}		0.8		μV/°C
Input Bias Current	+Input or −input		7.5	10.3	μA
Input Bias Current Drift			10		nA/°C
Input Offset Current			0.1	0.5	±μA
Open-Loop Gain		72	76		dB
INPUT CHARACTERISTICS					
Input Resistance			10		MΩ
Common-Mode Input Capacitance			1		pF
Input Common-Mode Voltage Range			0.9 to 4.6		V
Common-Mode Rejection Ratio	1.5 V to 3.5 V	−84	−98		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing		1.25 to 3.38	1.10 to 3.60		V
Linear Output Current			30		mA
Short-Circuit Current			50		mA
Capacitive Load Drive for 30% Overshoot	V_O = 50 mV p-p/1 V p-p		10/120		pF
DISABLE CHARACTERISTICS					
Off Isolation	f = 10 MHz		−40		dB
Turn-On Time	V_O = 0 V to 1 V, 50% logic to 50% output		45		ns
Turn-Off Time	V_O = 0 V to 1 V, 50% logic to 50% output		50		ns
$\overline{\text{DISABLE}}$ Voltage—Off/On	$V_{DISABLE} - V_{LOGIC\ REFERENCE}$		1.55/1.70		V
Enabled Leakage Current	LOGIC REFERENCE = 0.4 V		70		μA
	$\overline{\text{DISABLE}}$ = 4.0 V		2		μA
Disabled Leakage Current	LOGIC REFERENCE = 0.4 V		30		μA
	$\overline{\text{DISABLE}}$ = 0.4 V		33		μA
POWER SUPPLY					
Operating Range		±2.25	±5	±12.0	V
Quiescent Current	Output enabled		6.7	7.5	mA
	Output disabled		1.2	1.5	mA
+Power Supply Rejection Ratio	V_{CC} = 4.5 V to 5.5 V, V_{EE} = 0 V	−74	−82		dB
−Power Supply Rejection Ratio	V_{CC} = 5 V, V_{EE} = −0.5 V to +0.5 V	−76	−84		dB

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	26.4 V
Power Dissipation	Observed power derating curves
Input Voltage (Common Mode)	$\pm V_S \pm 1$ V
Differential Input Voltage[1]	±0.8 V
Differential Input Current	±10 mA
Output Short-Circuit Duration	Observed power derating curves
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C

[1] The AD8021 inputs are protected by diodes. Current-limiting resistors are not used to preserve the low noise. If a differential input exceeds ±0.8 V, the input current should be limited to ±10 mA.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8021 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately 150°C. Temporarily exceeding this limit can cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure.

While the AD8021 is internally short-circuit protected, this can not be sufficient to guarantee that the maximum junction temperature (150°C) is not exceeded under all conditions. To ensure proper operation, it is necessary to observe the maximum power derating curves.

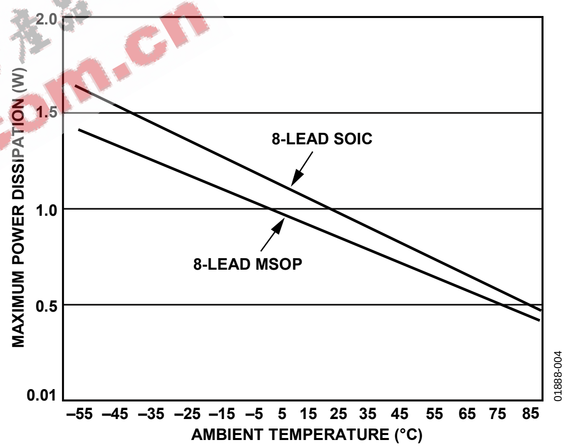


Figure 3. Maximum Power Dissipation vs. Temperature[1]

[1] Specification is for device in free air: 8-lead SOIC: θ_{JA} = 125°C/W; 8-lead MSOP: θ_{JA} = 145°C/W.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

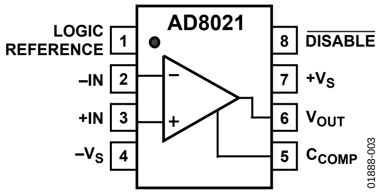


Figure 4. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	LOGIC REFERENCE	Reference for Pin 8[1] Voltage Level. Connect to logic low supply.
2	−IN	Inverting Input.
3	+IN	Noninverting Input.
4	$-V_S$	Negative Supply Voltage.
5	C_{COMP}	Compensation Capacitor. Tie to $-V_S$. (See the Applications section for value.)
6	V_{OUT}	Output.
7	$+V_S$	Positive Supply Voltage.
8	$\overline{\text{DISABLE}}$	Disable, Active Low.

[1] When Pin 8 ($\overline{\text{DISABLE}}$) is higher than Pin 1 (LOGIC REFERENCE) by approximately 2 V or more, the part is enabled. When Pin 8 is brought down to within about 1.5 V of Pin 1, the part is disabled. (See the Specifications tables for exact disable and enable voltage levels.) If the disable feature is not going to be used, Pin 8 can be tied to $+V_S$ or a logic high source, and Pin 1 can be tied to ground or logic low. Alternatively, if Pin 1 and Pin 8 are not connected, the part is in an enabled state.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_S = ±5 V, R_L = 1 kΩ, G = +2, R_F = R_G = 499 Ω, R_S = 49.9 Ω, R_O = 976 Ω, R_D = 53.6 Ω, C_C = 7 pF, C_L = 0, C_F = 0, V_{OUT} = 2 V p-p, frequency = 1 MHz, unless otherwise noted.

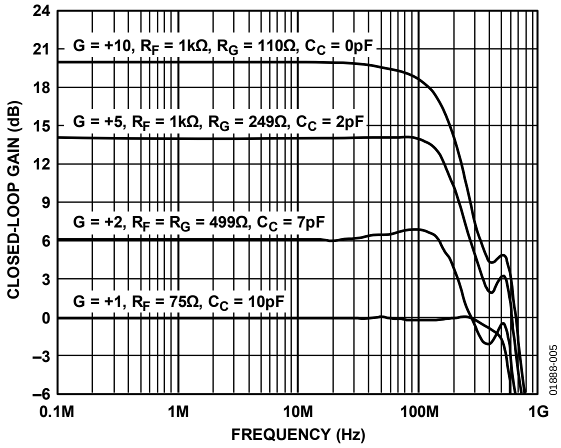


Figure 5. Small Signal Frequency Response vs. Frequency and Gain, V_{OUT} = 50 mV p-p, Noninverting (See Figure 48)

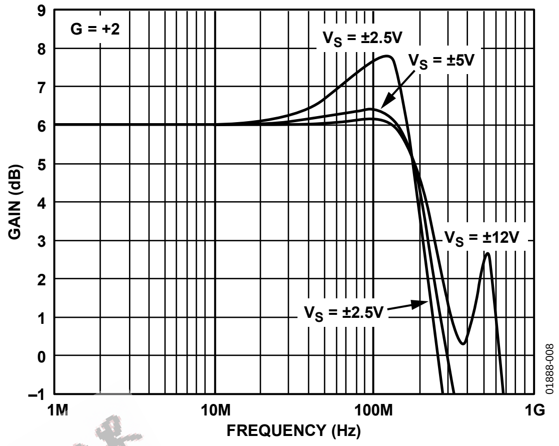


Figure 8. Small Signal Frequency Response vs. Frequency and Supply, V_{OUT} = 50 mV p-p, Noninverting (See Figure 48)

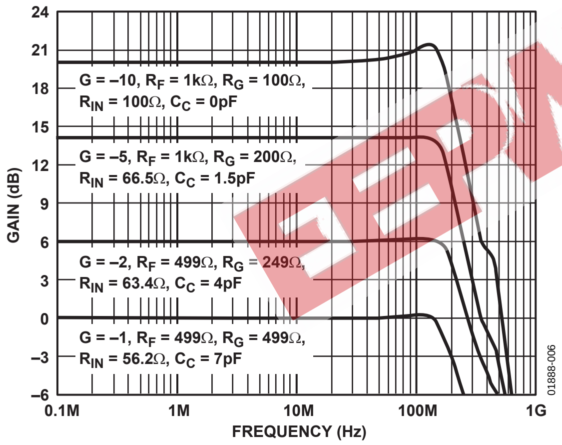


Figure 6. Small Signal Frequency Response vs. Frequency and Gain, V_{OUT} = 50 mV p-p Inverting (See Figure 48)

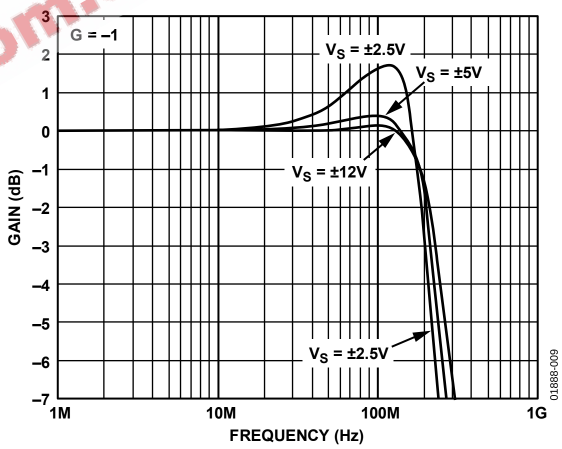


Figure 9. Small Signal Frequency Response vs. Frequency and Supply, V_{OUT} = 50 mV p-p, Inverting (See Figure 50)

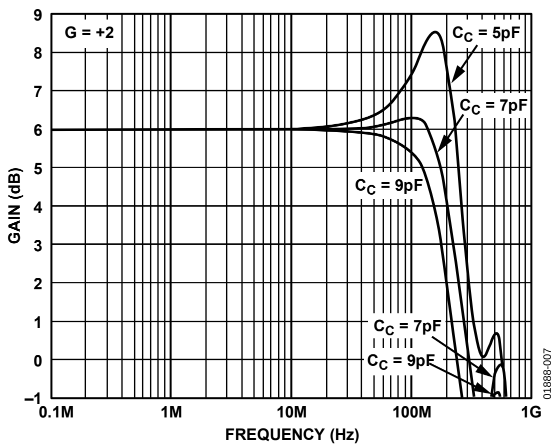


Figure 7. Small Signal Frequency Response vs. Frequency and Compensation Capacitor, V_{OUT} = 50 mV p-p (See Figure 48)

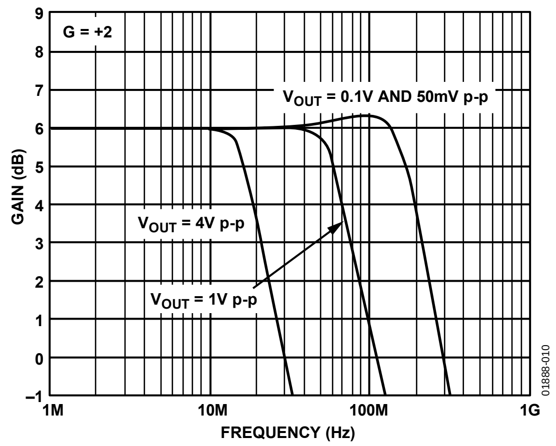


Figure 10. Frequency Response vs. Frequency and V_{OUT}, Noninverting (See Figure 48)

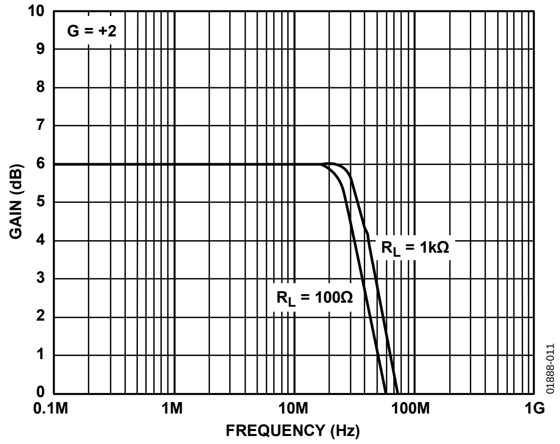


Figure 11. Large Signal Frequency Response vs. Frequency and Load, Noninverting (See Figure 49)

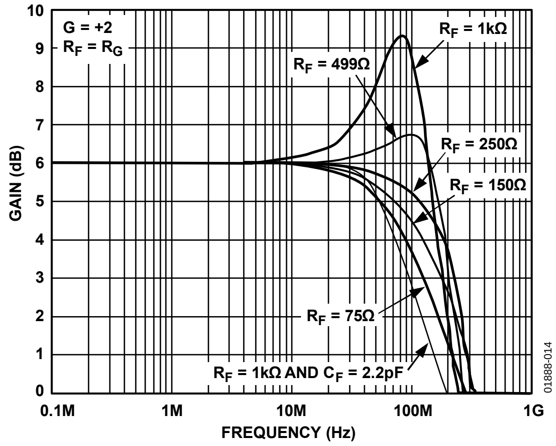


Figure 14. Small Signal Frequency Response vs. Frequency and R_F, Noninverting, V_{OUT} = 50 mV p-p (See Figure 48)

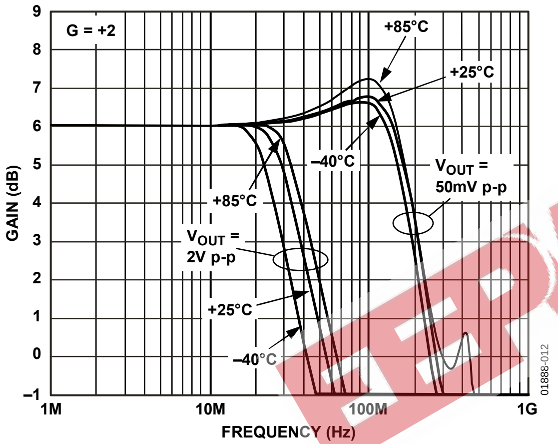


Figure 12. Frequency Response vs. Frequency, Temperature, and V_{OUT}, Noninverting (See Figure 48)

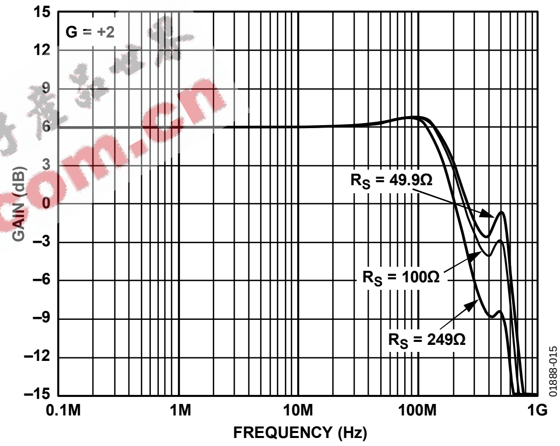


Figure 15. Small Signal Frequency Response vs. Frequency and R_S, Noninverting, V_{OUT} = 50 mV p-p (See Figure 48)

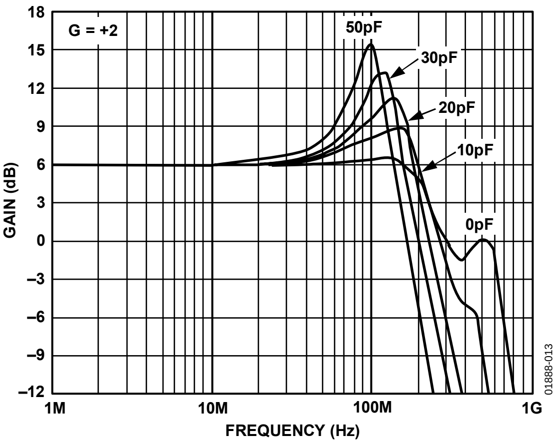


Figure 13. Small Signal Frequency Response vs. Frequency and Capacitive Load, Noninverting, V_{OUT} = 50 mV p-p (See Figure 49 and Figure 71)

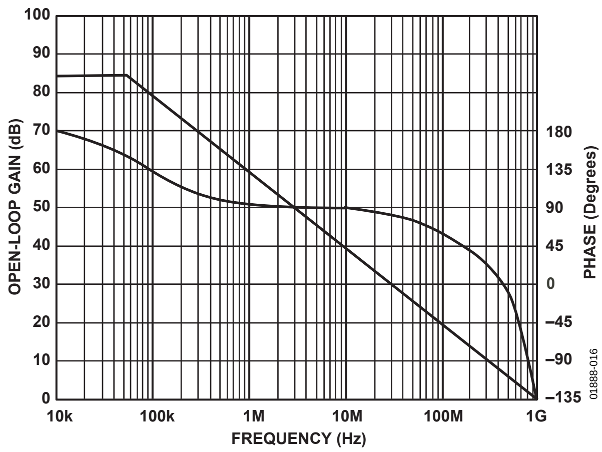


Figure 16. Open-Loop Gain and Phase vs. Frequency, R_G = 100 Ω, R_F = 1 kΩ, R_O = 976 Ω, R_D = 53.6 Ω, C_C = 0 pF (See Figure 50)

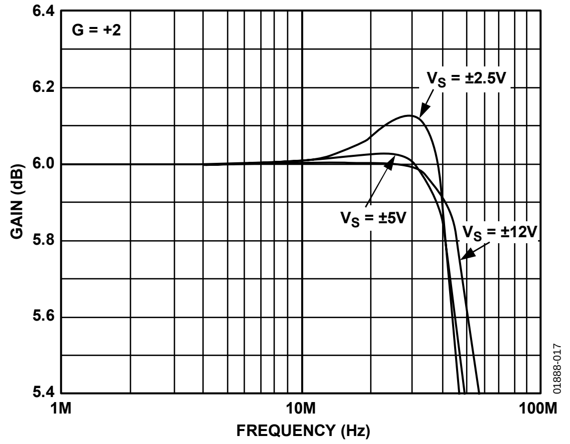


Figure 17. 0.1 dB Flatness vs. Frequency and Supply, V_{OUT} = 1 V p-p, R_L = 150 Ω, Noninverting (See Figure 49)

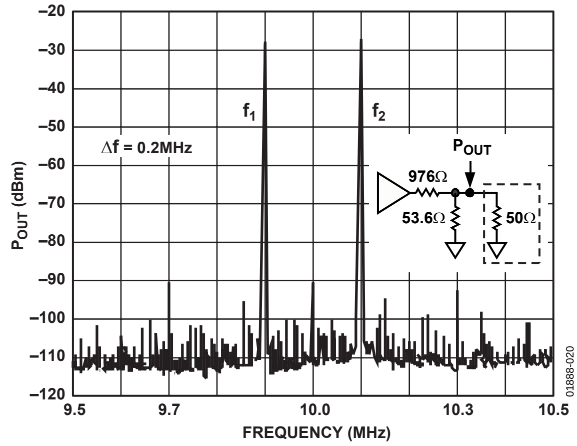


Figure 20. Intermodulation Distortion vs. Frequency

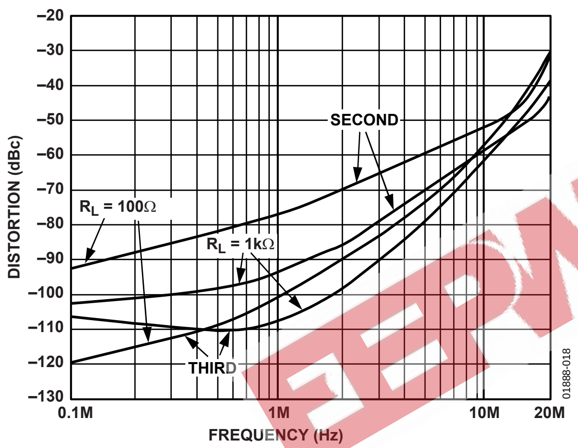


Figure 18. Second and Third Harmonic Distortion vs. Frequency and R_L

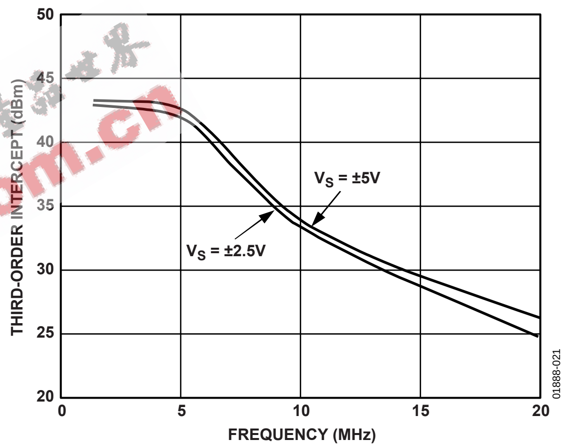


Figure 21. Third-Order Intercept vs. Frequency and Supply Voltage

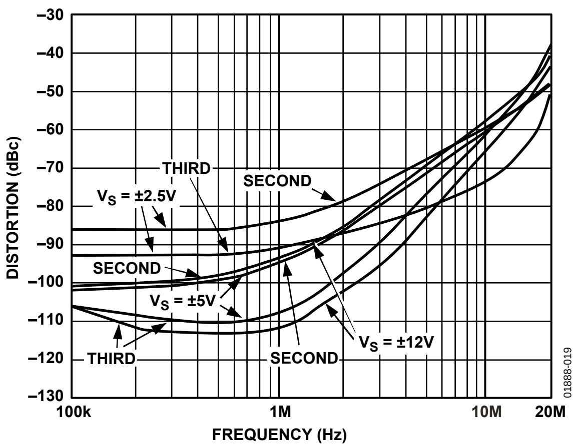


Figure 19. Second and Third Harmonic Distortion vs. Frequency and V_S

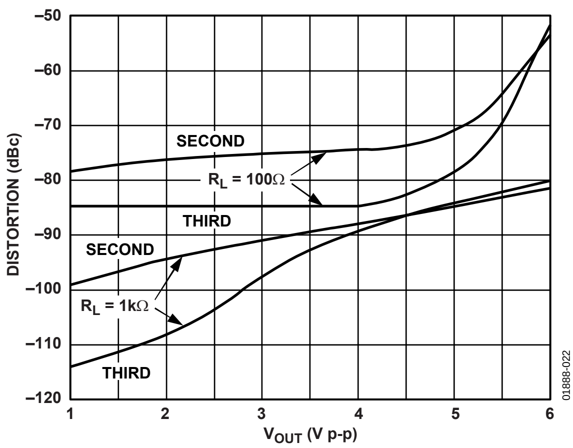


Figure 22. Second and Third Harmonic Distortion vs. V_{OUT} and R_L

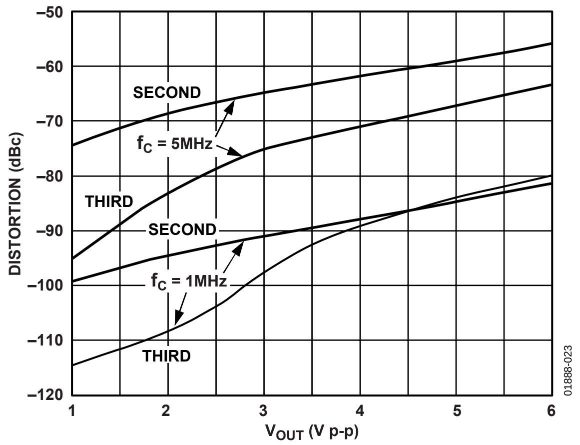


Figure 23. Second and Third Harmonic Distortion vs. V_{OUT} and Fundamental Frequency (f_C), G = +2

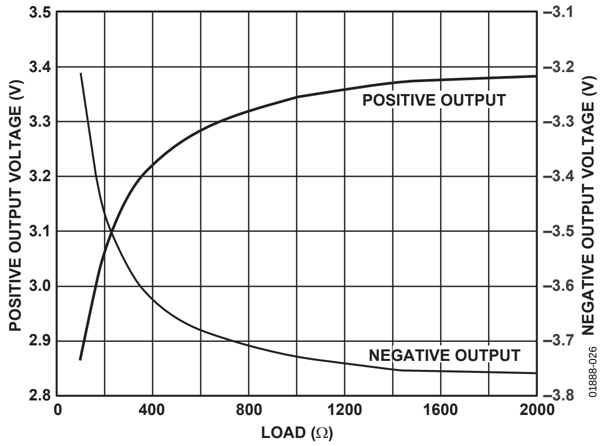


Figure 26. DC Output Voltages vs. Load (See Figure 48)

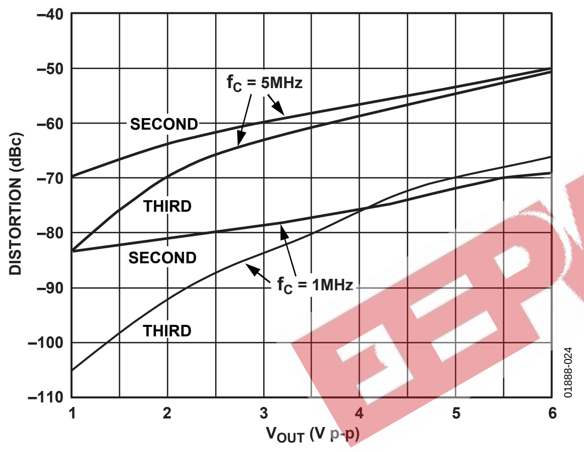


Figure 24. Second and Third Harmonic Distortion vs. V_{OUT} and Fundamental Frequency (f_C), G = +10

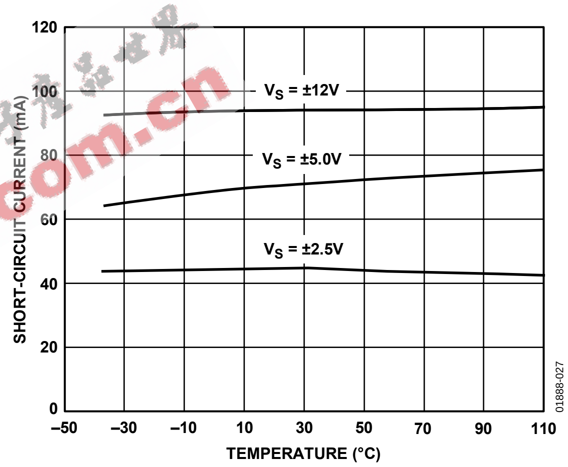


Figure 27. Short-Circuit Current to Ground vs. Temperature

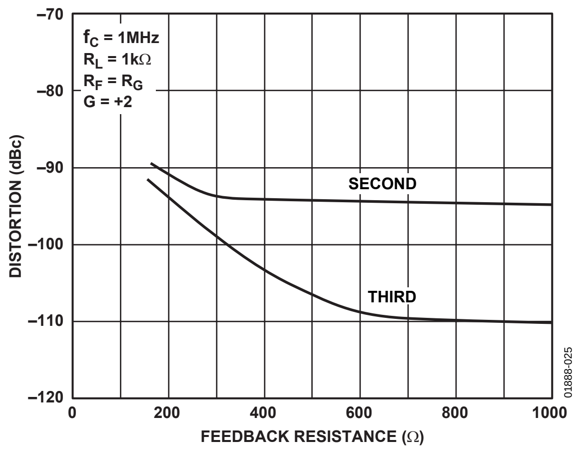


Figure 25. Second and Third Harmonic Distortion vs. Feedback Resistor (R_F)

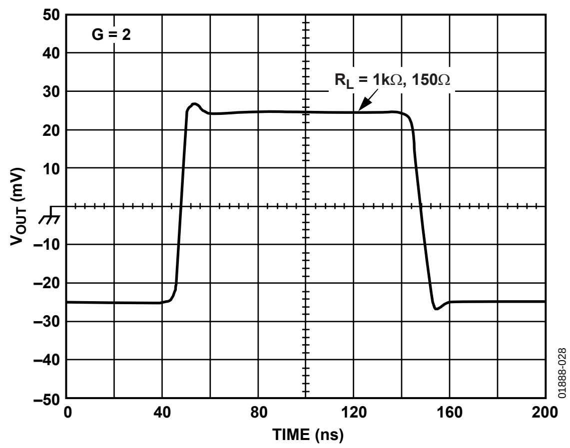


Figure 28. Small Signal Transient Response vs. R_L, V_O = 50 mV p-p, Noninverting (See Figure 49)

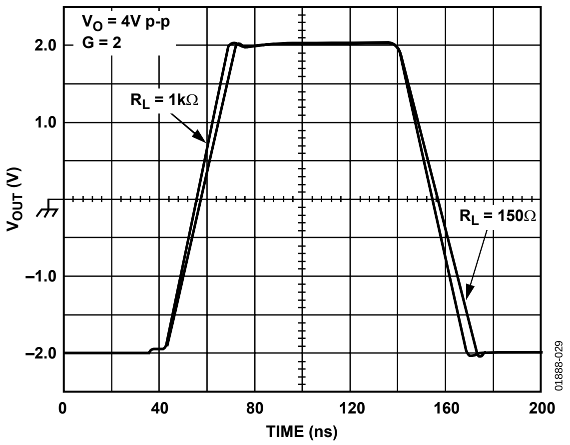


Figure 29. Large Signal Transient Response vs. R_L, Noninverting (See Figure 49)

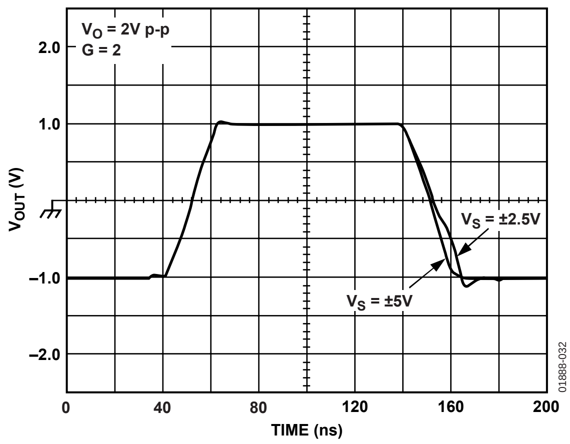


Figure 32. Large Signal Transient Response vs. V_S (See Figure 48)

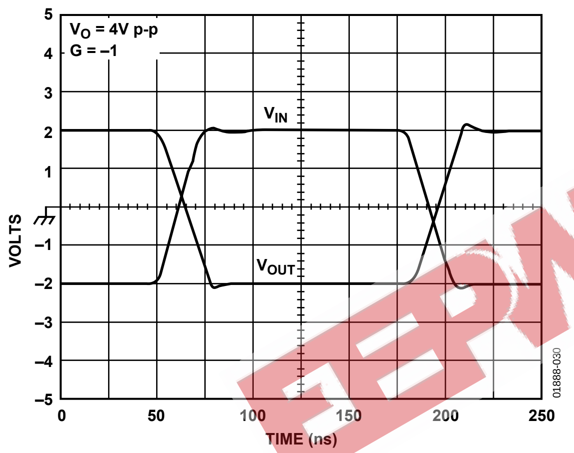


Figure 30. Large Signal Transient Response, Inverting (See Figure 50)

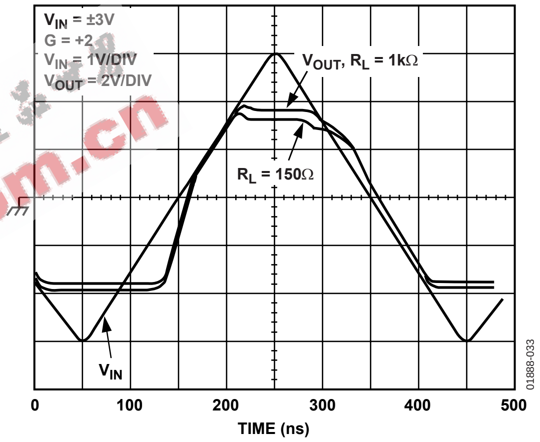


Figure 33. Overdrive Recovery vs. R_L (See Figure 49)

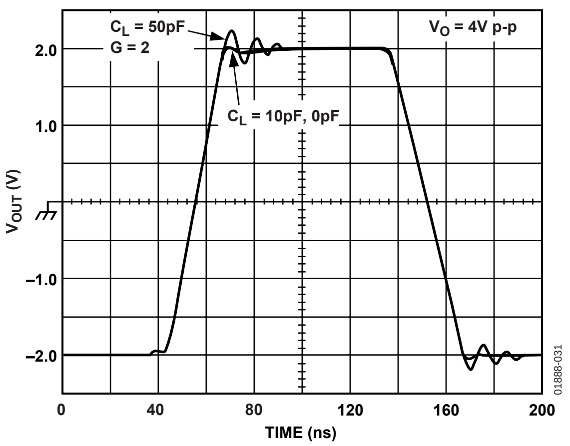


Figure 31. Large Signal Transient Response vs. C_L (See Figure 48)

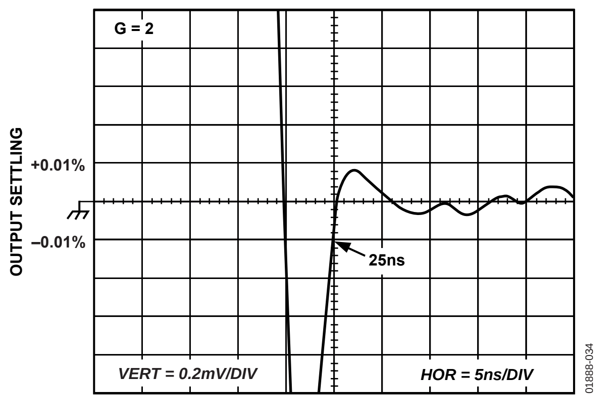


Figure 34. 0.01% Settling Time, 2 V Step

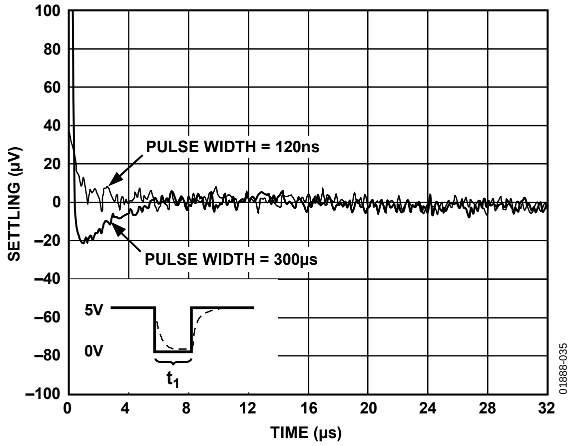


Figure 35. Long-Term Settling, 0 V to 5 V, V_S = ±12 V, G = +13

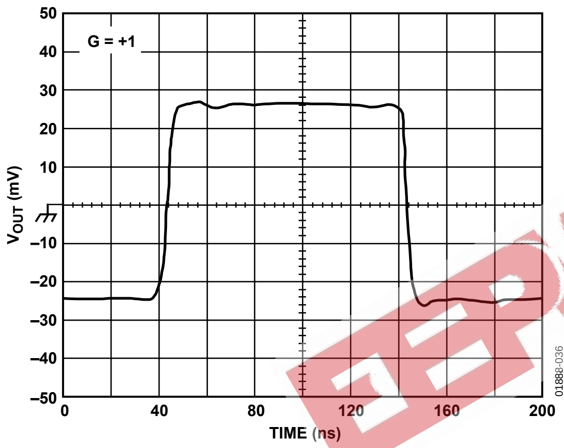


Figure 36. Small Signal Transient Response, V_O = 50 mV p-p, G = +1 (See Figure 48)

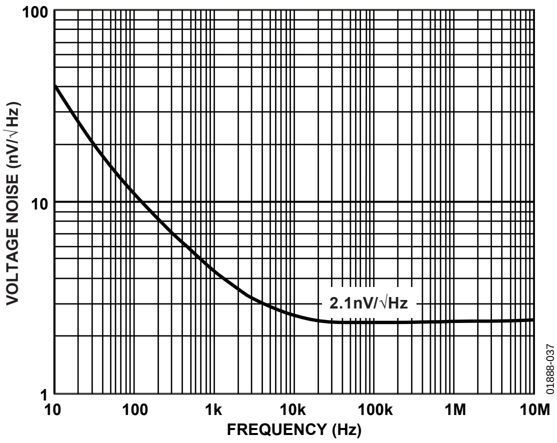


Figure 37. Input Voltage Noise vs. Frequency

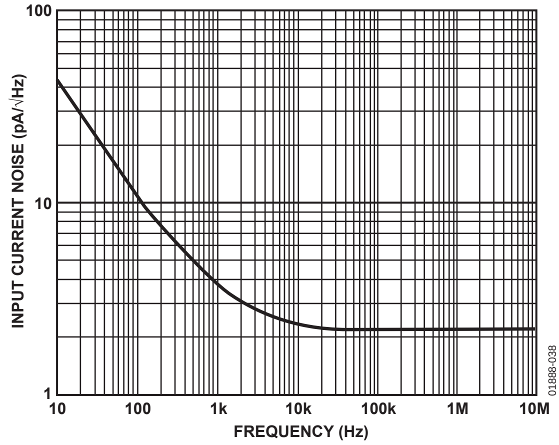


Figure 38. Input Current Noise vs. Frequency

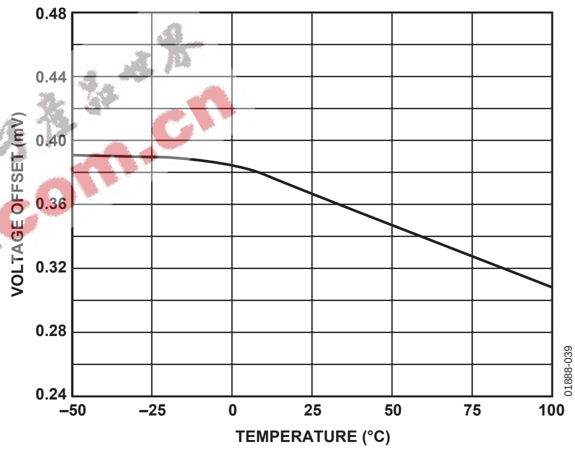


Figure 39. V_{OS} vs. Temperature

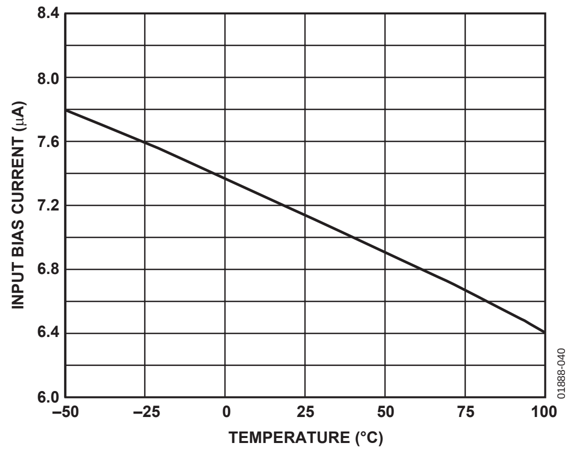


Figure 40. Input Bias Current vs. Temperature

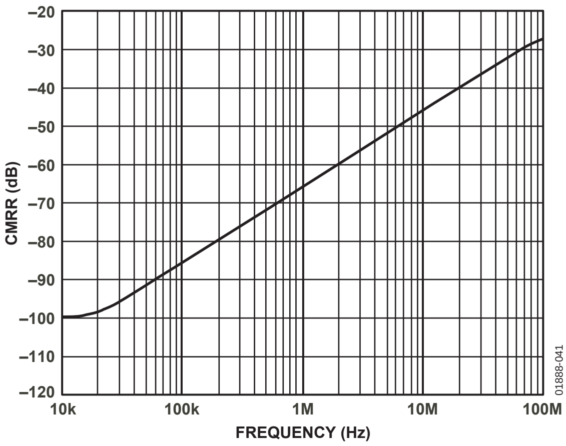


Figure 41. CMRR vs. Frequency (See Figure 51)

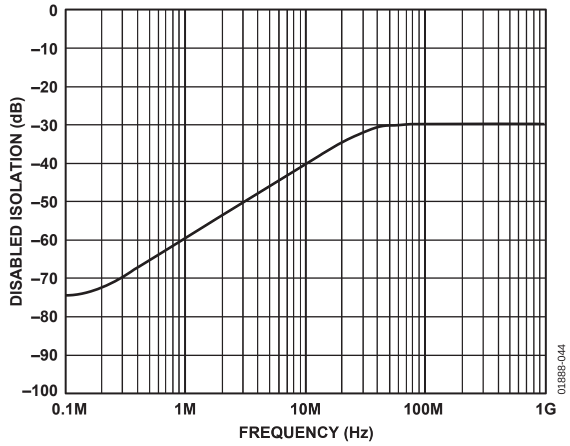


Figure 44. Input-to-Output Isolation, Chip Disabled (See Figure 54)

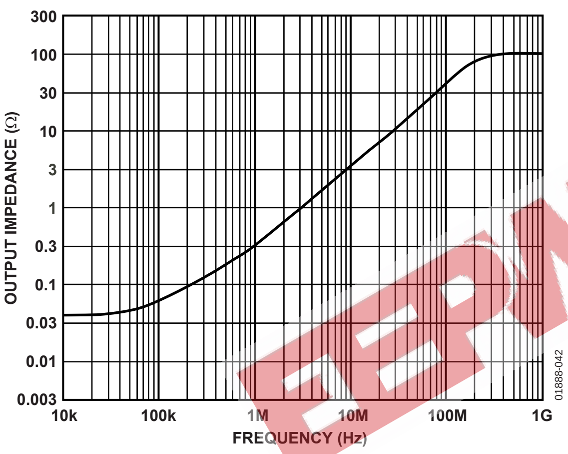


Figure 42. Output Impedance vs. Frequency, Chip Enabled (See Figure 52)

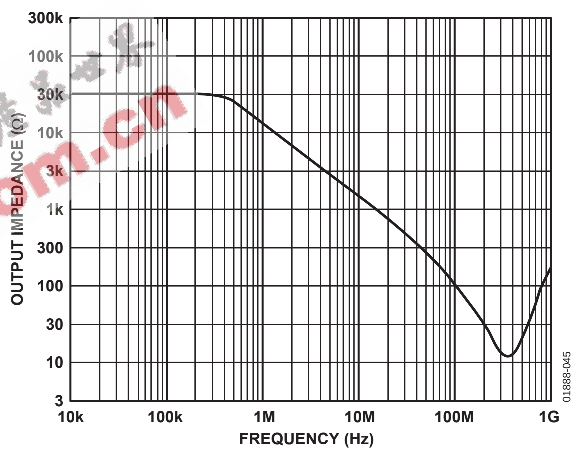


Figure 45. Output Impedance vs. Frequency, Chip Disabled (See Figure 55)

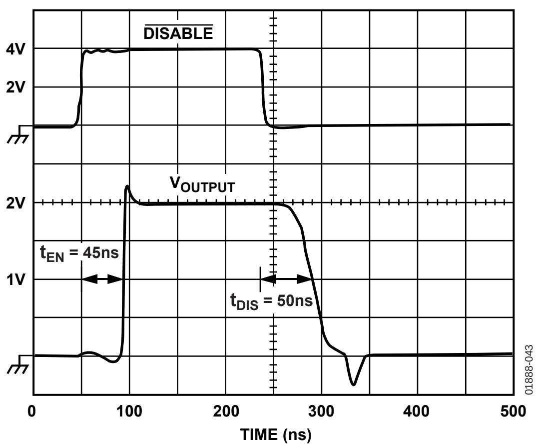


Figure 43. Enable (t_{EN})/Disable (t_{DIS}) Time vs. V_{OUT} (See Figure 53)

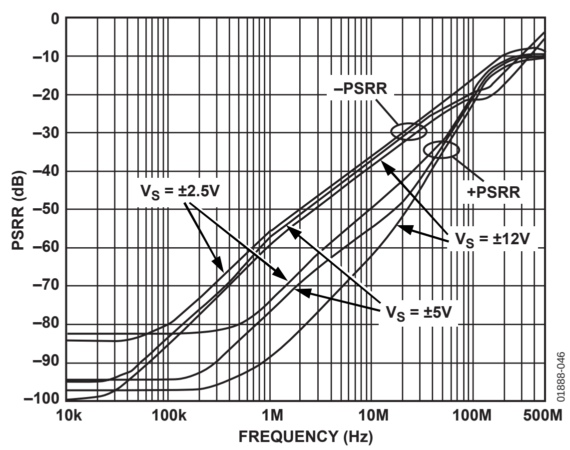


Figure 46. PSRR vs. Frequency and Supply Voltage (See Figure 56 and Figure 57)

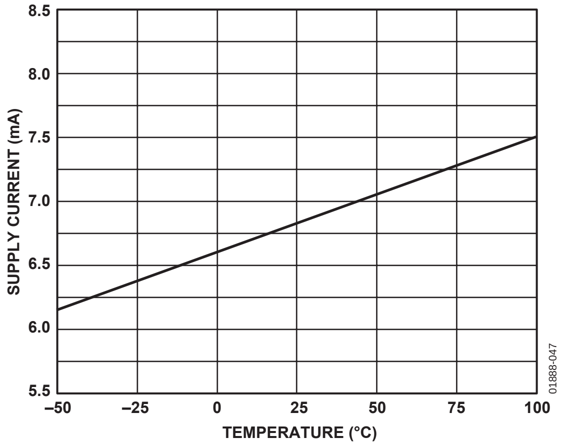


Figure 47. Quiescent Supply Current vs. Temperature

TEST CIRCUITS

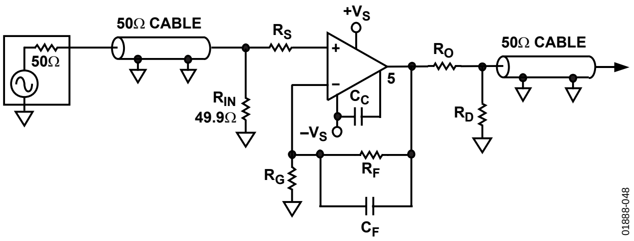


Figure 48. Noninverting Gain

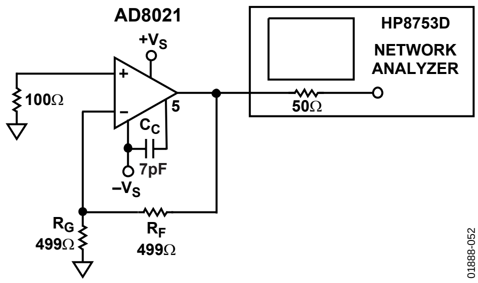


Figure 52. Output Impedance, Chip Enabled

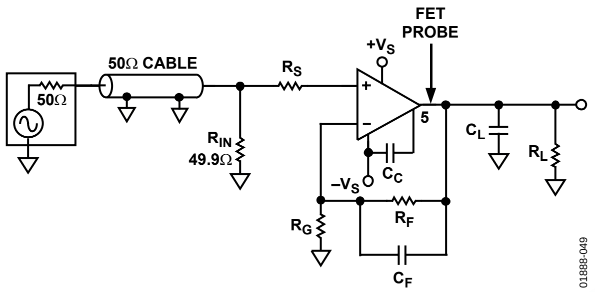


Figure 49. Noninverting Gain and FET Probe

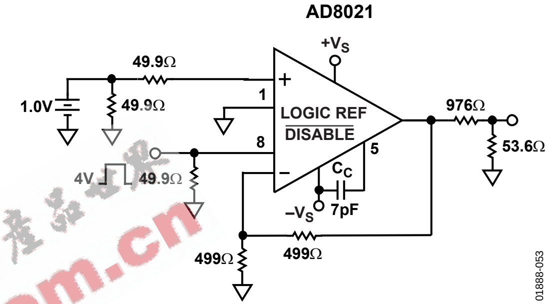


Figure 53. Enable/Disable

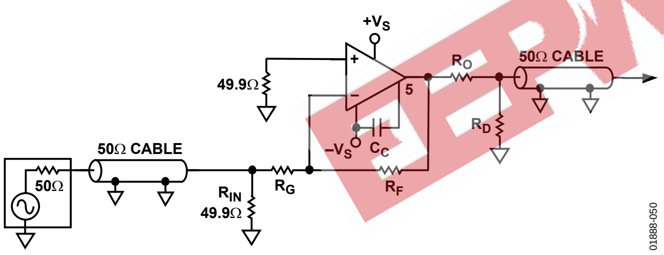


Figure 50. Inverting Gain

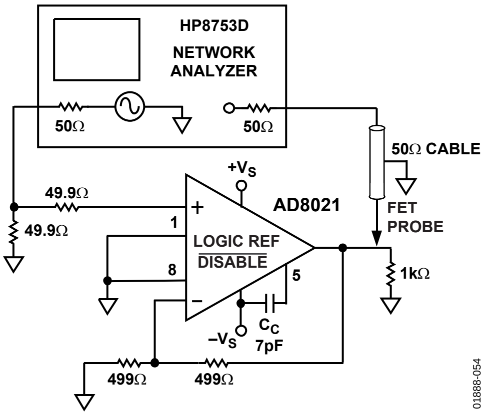


Figure 54. Input-to-Output Isolation, Chip Disabled

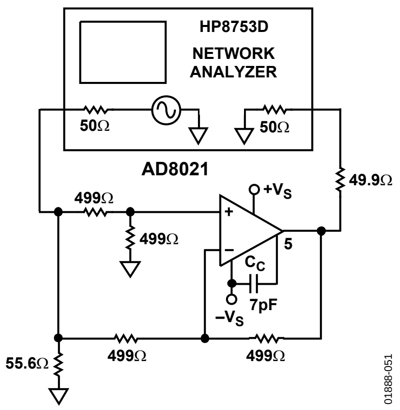


Figure 51. CMRR

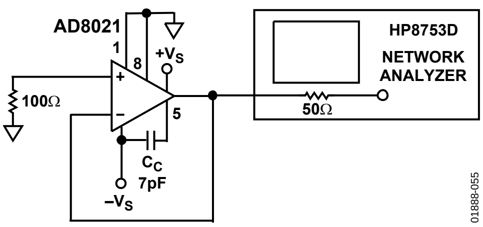


Figure 55. Output Impedance, Chip Disabled

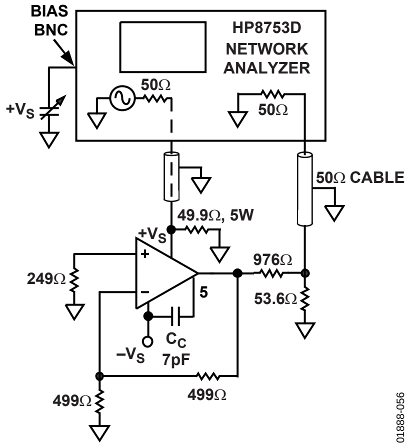


Figure 56. Positive PSRR

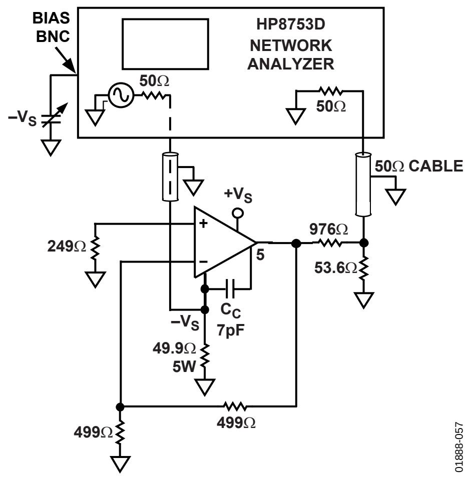


Figure 57. Negative PSRR

APPLICATIONS

The typical voltage feedback op amp is frequency stabilized with a fixed internal capacitor, $C_{INTERNAL}$, using dominant pole compensation. To a first-order approximation, voltage feedback op amps have a fixed gain bandwidth product. For example, if its −3 dB bandwidth is 200 MHz for a gain of G = +1; at a gain of G = +10, its bandwidth is only about 20 MHz. The AD8021 is a voltage feedback op amp with a minimal $C_{INTERNAL}$ of about 1.5 pF. By adding an external compensation capacitor, C_C, the user can circumvent the fixed gain bandwidth limitation of other voltage feedback op amps.

Unlike the typical op amp with fixed compensation, the AD8021 allows the user to:

- Maximize the amplifier bandwidth for closed-loop gains between 1 and 10, avoiding the usual loss of bandwidth and slew rate.
- Optimize the trade-off between bandwidth and phase margin for a particular application.
- Match bandwidth in gain blocks with different noise gains, such as when designing differential amplifiers (as shown in Figure 65).

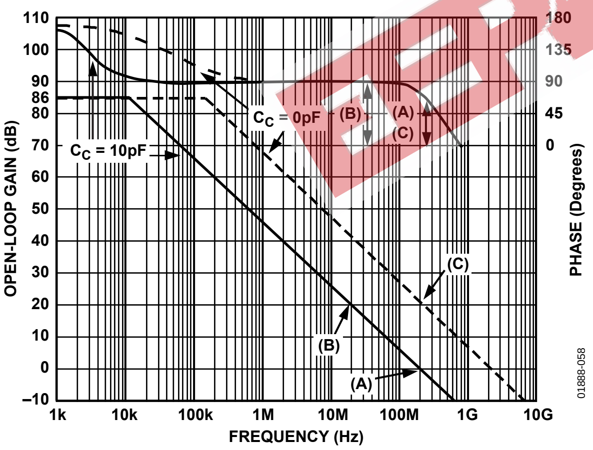


Figure 58. Simplified Diagram of Open-Loop Gain and Phase Response

Figure 58 is the AD8021 gain and phase plot that has been simplified for instructional purposes. Arrow A in Figure 58 shows a bandwidth of about 200 MHz and a phase margin at about 60° when the desired closed-loop gain is G = +1 and the value chosen for the external compensation capacitor is C_C = 10 pF. If the gain is changed to G = +10 and C_C is fixed at 10 pF, then (as expected for a typical op amp) the bandwidth is degraded to about 20 MHz and the phase margin increases to 90° (Arrow B). However, by reducing C_C to 0 pF, the bandwidth and phase margin return to about 200 MHz and 60° (Arrow C), respectively. In addition, the slew rate is dramatically increased, as it roughly varies with the inverse of C_C.

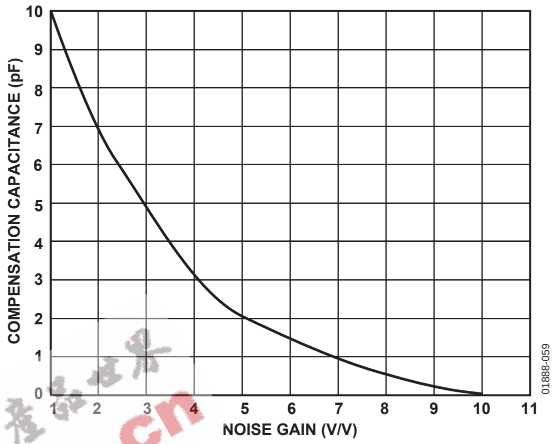


Figure 59. Suggested Compensation Capacitance vs. Gain for Maintaining 1 dB Peaking

Table 6 and Figure 59 provide recommended values of compensation capacitance at various gains and the corresponding slew rate, bandwidth, and noise. Note that the value of the compensation capacitor depends on the circuit noise gain, not the voltage gain. As shown in Figure 60, the noise gain, G_N, of an op amp gain block is equal to its noninverting voltage gain, regardless of whether it is actually used for inverting or noninverting gain. Thus,

Noninverting $G_N = R_F/R_G + 1$

Inverting $G_N = R_F/R_G + 1$

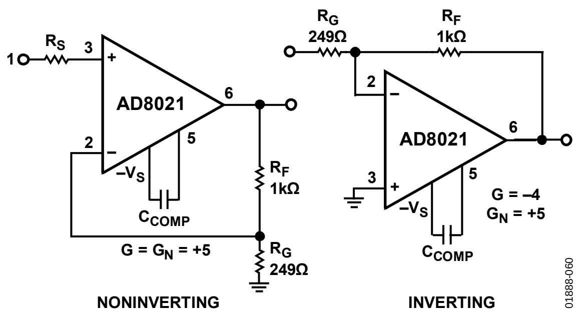


Figure 60. The Noise Gain of Both is 5

$C_F = C_L = 0$, $R_L = 1\ k\Omega$, $R_{IN} = 49.9\ \Omega$ (see Figure 49).

Table 6. Recommended Component Values

Noise Gain (Noninverting Gain)	R_S (Ω)	R_F (Ω)	R_G (Ω)	C_{COMP} (pF)	Slew Rate (V/μs)	−3 dB SS BW (MHz)	Output Noise (AD8021 Only) (nV/√Hz)	Output Noise (AD8021 with Resistors) (nV/√Hz)
1	75	75	NA	10	120	490	2.1	2.8
2	49.9	499	499	7	150	205	4.3	8.2
5	49.9	1 k	249	2	300	185	10.7	15.5
10	49.9	1 k	110	0	420	150	21.2	27.9
20	49.9	1 k	52.3	0	200	42	42.2	52.7
100	49.9	1 k	10	0	34	6	211.1	264.1

With the AD8021, a variety of trade-offs can be made to fine-tune its dynamic performance. Sometimes more bandwidth or slew rate is needed at a particular gain. Reducing the compensation capacitance, as illustrated in Figure 7, increases the bandwidth and peaking due to a decrease in phase margin. On the other hand, if more stability is needed, increasing the compensation capacitor decreases the bandwidth while increasing the phase margin.

As with all high speed amplifiers, parasitic capacitance and inductance around the amplifier can affect its dynamic response. Often, the input capacitance (due to the op amp itself, as well as the PC board) has a significant effect. The feedback resistance, together with the input capacitance, can contribute to a loss of phase margin, thereby affecting the high frequency response, as shown in Figure 14. A capacitor (C_F) in parallel with the feedback resistor can compensate for this phase loss.

Additionally, any resistance in series with the source creates a pole with the input capacitance (as well as dampen high frequency resonance due to package and board inductance and capacitance), the effect of which is shown in Figure 15.

It must also be noted that increasing resistor values increases the overall noise of the amplifier and that reducing the feedback resistor value increases the load on the output stage, thus increasing distortion (see Figure 22).

USING THE DISABLE FEATURE

When Pin 8 ($\overline{\text{DISABLE}}$) is higher than Pin 1 (LOGIC REFERENCE) by approximately 2 V or more, the part is enabled. When Pin 8 is brought down to within about 1.5 V of Pin 1, the part is disabled. See Table 1 for exact disable and enable voltage levels. If the disable feature is not used, Pin 8 can be tied to V_S or a logic high source, and Pin 1 can be tied to ground or logic low. Alternatively, if Pin 1 and Pin 8 are not connected, the part is in an enabled state.

THEORY OF OPERATION

The AD8021 is fabricated on the second generation of Analog Devices proprietary High Voltage eXtra-Fast Complementary Bipolar (XFCB) process, which enables the construction of PNP and NPN transistors with similar f_Ts in the 3 GHz region. The transistors are dielectrically isolated from the substrate (and each other), eliminating the parasitic and latch-up problems caused by junction isolation. It also reduces nonlinear capacitance (a source of distortion) and allows a higher transistor, f_T, for a given quiescent current. The supply current is trimmed, which results in less part-to-part variation of bandwidth, slew rate, distortion, and settling time.

As shown in Figure 61, the AD8021 input stage consists of an NPN differential pair in which each transistor operates at a 0.8 mA collector current. This allows the input devices a high transconductance; thus, the AD8021 has a low input noise of 2.1 nV/√Hz @ 50 kHz. The input stage drives a folded cascode that consists of a pair of PNP transistors. The folded cascode and current mirror provide a differential-to-single-ended conversion of signal current. This current then drives the high impedance node (Pin 5), where the C_C external capacitor is connected. The output stage preserves this high impedance with a current gain of 5000, so that the AD8021 can maintain a high open-loop gain even when driving heavy loads.

Two internal diode clamps across the inputs (Pin 2 and Pin 3) protect the input transistors from large voltages that could otherwise cause emitter-base breakdown, which would result in degradation of offset voltage and input bias current.

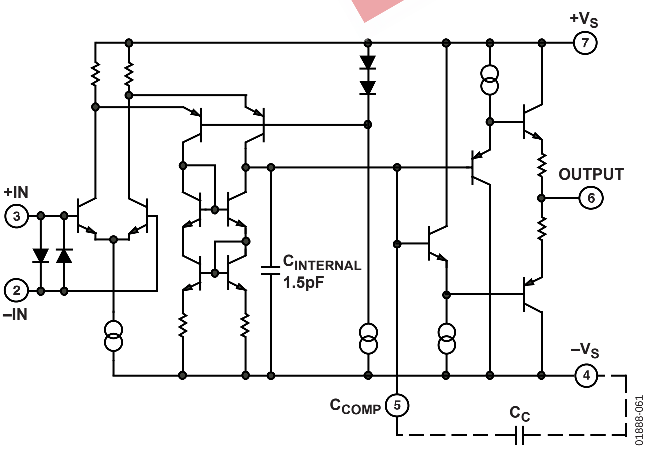


Figure 61. Simplified Schematic

PCB LAYOUT CONSIDERATIONS

As with all high speed op amps, achieving optimum performance from the AD8021 requires careful attention to PC board layout. Particular care must be exercised to minimize lead lengths between the ground leads of the bypass capacitors and between the compensation capacitor and the negative supply. Otherwise, lead inductance can influence the frequency response and even cause high frequency oscillations. Use of a multilayer printed circuit board, with an internal ground plane, reduces ground noise and enables a compact component arrangement.

Due to the relatively high impedance of Pin 5 and low values of the compensation capacitor, a guard ring is recommended. The guard ring is simply a PC trace that encircles Pin 5 and is connected to the output, Pin 6, which is at the same potential as Pin 5. This serves two functions. It shields Pin 5 from any local circuit noise generated by surrounding circuitry. It also minimizes stray capacitance, which would tend to otherwise reduce the bandwidth. An example of a guard ring layout is shown in Figure 62.

Also shown in Figure 62, the compensation capacitor is located immediately adjacent to the edge of the AD8021 package, spanning Pin 4 and Pin 5. This capacitor must be a high quality surface-mount COG or NPO ceramic. The use of leaded capacitors is not recommended. The high frequency bypass capacitor(s) should be located immediately adjacent to the supplies, Pin 4 and Pin 7.

To achieve the shortest possible lead length at the inverting input, the feedback resistor R_F is located beneath the board and spans the distance from the output, Pin 6, to inverting input Pin 2. The return node of Resistor R_G should be situated as close as possible to the return node of the negative supply bypass capacitor connected to Pin 4.

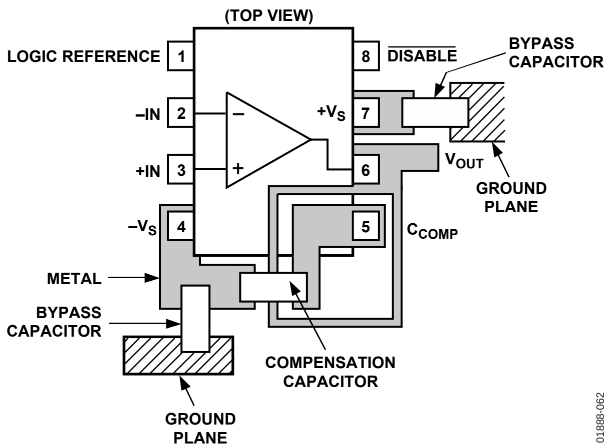


Figure 62. Recommended Location of Critical Components and Guard Ring

DRIVING 16-BIT ADCs

Low noise and adjustable compensation make the AD8021 especially suitable as a buffer/driver for high resolution ADCs.

As seen in Figure 19, the harmonic distortion is better than 90 dBc at frequencies between 100 kHz and 1 MHz. This is an advantage for complex waveforms that contain high frequency information, because the phase and gain integrity of the sampled waveform can be preserved throughout the conversion process. The increase in loop gain results in improved output regulation and lower noise when the converter input changes state during a sample. This advantage is particularly apparent when using 16-bit high resolution ADCs with high sampling rates.

Figure 63 shows a typical ADC driver configuration. The AD8021 is in an inverting gain of −7.5, f_C is 65 kHz, and its output voltage is 10 V p-p. The results are listed in Table 7.

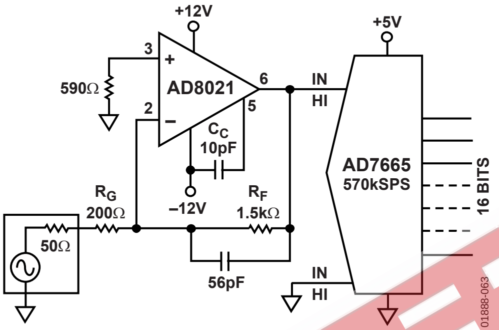


Figure 63. Inverting ADC Driver, Gain = −7.5, f_C = 65 kHz

Table 7. Summary of ADC Driver Performance (f_C = 65 kHz, V_{OUT} = 10 V p-p)

Parameter	Measurement	Unit
Second Harmonic Distortion	−101.3	dBc
Third Harmonic Distortion	−109.5	dBc
THD	−100.0	dBc
SFDR	+100.3	dBc

Figure 64 shows another ADC driver connection. The circuit was tested with a noninverting gain of 10.1 and an output voltage of approximately 20 V p-p for optimum resolution and noise performance. No filtering was used. An FFT was performed using Analog Devices evaluation software for the AD7665 16-bit converter. The results are listed in Table 8.

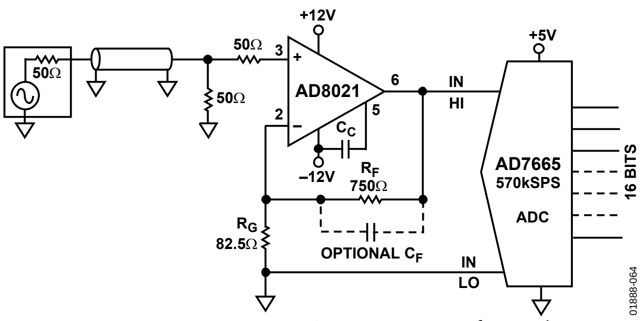


Figure 64. Noninverting ADC Driver, Gain = 10, f_C = 100 kHz

Table 8. Summary of ADC Driver Performance (f_C = 100 kHz, V_{OUT} = 20 V p-p)

Parameter	Measurement	Unit
Second Harmonic Distortion	−92.6	dBc
Third Harmonic Distortion	−86.4	dBc
THD	−84.4	dBc
SFDR	+5.4	dBc

DIFFERENTIAL DRIVER

The AD8021 is uniquely suited as a low noise differential driver for many ADCs, balanced lines, and other applications requiring differential drive. If pairs of internally compensated op amps are configured as inverter and follower, the noise gain of the inverter is higher than that of the follower section, resulting in an imbalance in the frequency response (see Figure 66).

A better solution takes advantage of the external compensation feature of the AD8021. By reducing the C_{COMP} value of the inverter, its bandwidth can be increased to match that of the follower, avoiding compromises in gain bandwidth and phase delay. The inverting and noninverting bandwidths can be closely matched using the compensation feature, thus minimizing distortion.

Figure 65 illustrates an inverter-follower driver circuit operating at a gain of 2, using individually compensated AD8021s. The values of feedback and load resistors were selected to provide a total load of less than 1 kΩ, and the equivalent resistances seen at each op amp's inputs were matched to minimize offset voltage and drift. Figure 67 is a plot of the resulting ac responses of driver halves.

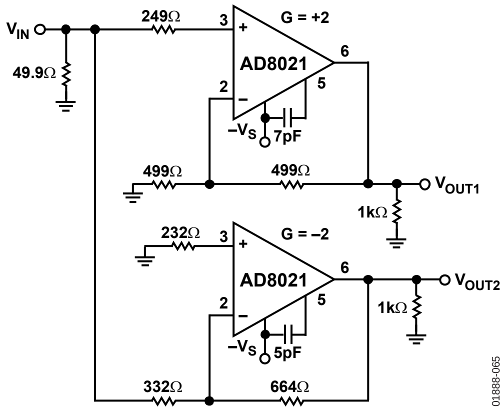


Figure 65. Differential Amplifier

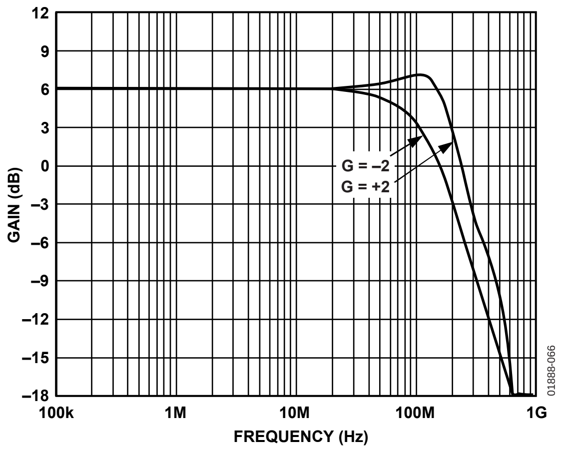


Figure 66. AC Response of Two Identically Compensated High Speed Op Amps Configured for a Gain of +2 and a Gain of −2

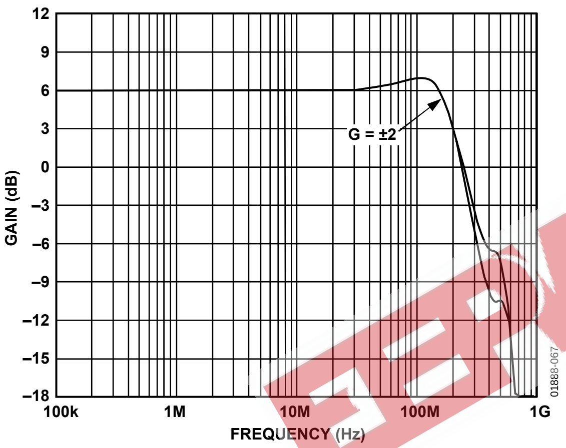


Figure 67. AC Response of Two Dissimilarly Compensated AD8021 Op Amps (Figure 66) Configured for a Gain of +2 and a Gain of −2, (Note the Close Gain Match)

USING THE AD8021 IN ACTIVE FILTERS

The low noise and high gain bandwidth of the AD8021 make it an excellent choice in active filter circuits. Most active filter literature provides resistor and capacitor values for various filters but neglects the effect of the op amp's finite bandwidth on filter performance; ideal filter response with infinite loop gain is implied. Unfortunately, real filters do not behave in this manner. Instead, they exhibit finite limits of attenuation, depending on the gain bandwidth of the active device. Good low-pass filter performance requires an op amp with high gain bandwidth for attenuation at high frequencies, and low noise and high dc gain for low frequency, pass-band performance.

Figure 68 shows the schematic of a 2-pole, low-pass active filter and lists typical component values for filters having a Bessel-type response with a gain of 2 and a gain of 5. Figure 69 is a network analyzer plot of this filter's performance.

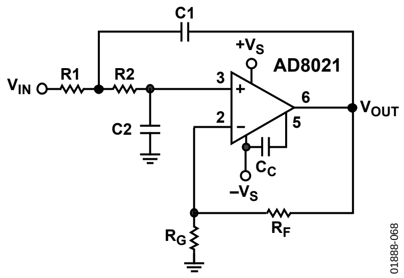


Figure 68. Schematic of a Second-Order, Low-Pass Active Filter

Table 9. Typical Component Values for Second-Order, Low-Pass Active Filter of Figure 68

Gain	R1 (Ω)	R2 (Ω)	R_F (Ω)	R_G (Ω)	C1 (nF)	C2 (nF)	C_C (pF)
2	71.5	215	499	499	10	10	7
5	44.2	365	365	90.9	10	10	2

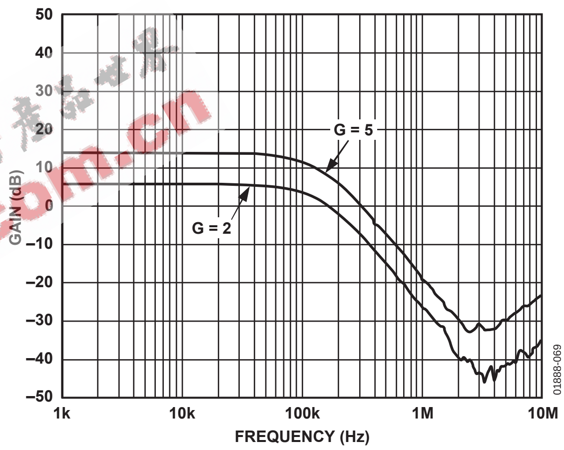


Figure 69. Frequency Response of the Filter Circuit of Figure 68 for Two Different Gains

DRIVING CAPACITIVE LOADS

When the AD8021 drives a capacitive load, the high frequency response can show excessive peaking before it rolls off. Two techniques can be used to improve stability at high frequency and reduce peaking. The first technique is to increase the compensation capacitor, C_C, which reduces the peaking while maintaining gain flatness at low frequencies. The second technique is to add a resistor, R_{SNUB}, in series between the output pin of the AD8021 and the capacitive load, C_L. Figure 70 shows the response of the AD8021 when both C_C and R_{SNUB} are used to reduce peaking. For a given C_L, Figure 71 can be used to determine the value of R_{SNUB} that maintains 2 dB of peaking in the frequency response. Note, however, that using R_{SNUB} attenuates the low frequency output by a factor of $R_{LOAD}/(R_{SNUB} + R_{LOAD})$.

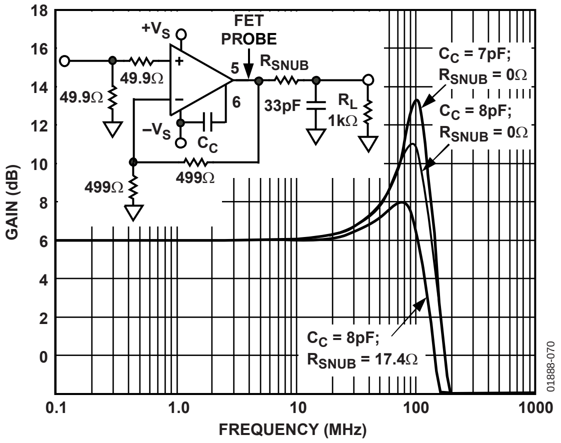


Figure 70. Peaking vs. R_{SNUB} and C_C for C_L = 33 pF

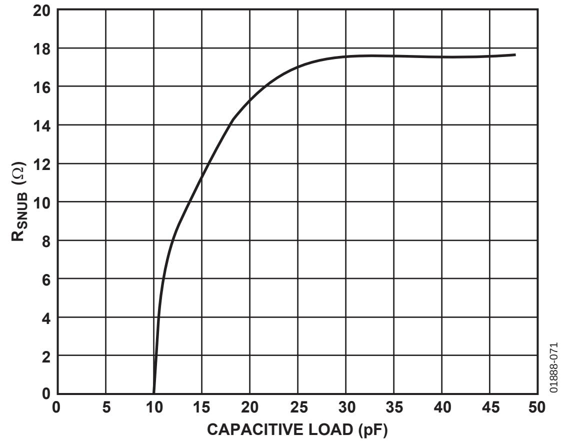
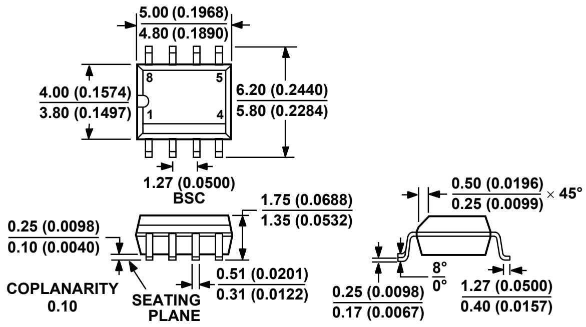


Figure 71. Relationship of R_{SNUB} vs. C_L for 2 dB Peaking at a Gain of +2

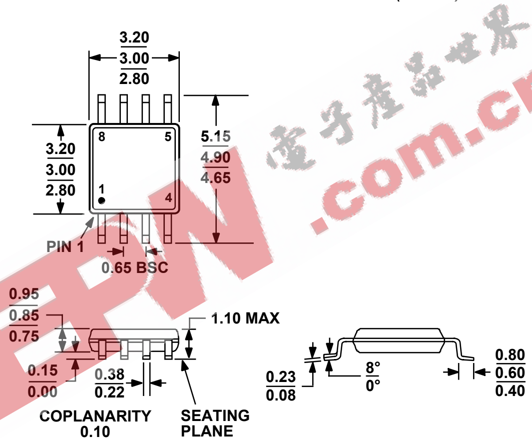
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 72. 8-Lead Standard Small Outline Package [SOIC]
Narrow Body (R-8)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 73. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
AD8021AR	−40°C to +85°C	8-Lead SOIC	R-8	
AD8021AR-REEL	−40°C to +85°C	8-Lead SOIC	R-8	
AD8021AR-REEL7	−40°C to +85°C	8-Lead SOIC	R-8	
AD8021ARZ[1]	−40°C to +85°C	8-Lead SOIC	R-8	
AD8021ARZ-REEL[1]	−40°C to +85°C	8-Lead SOIC	R-8	
AD8021ARZ-REEL7[1]	−40°C to +85°C	8-Lead SOIC	R-8	
AD8021ARM	−40°C to +85°C	8-Lead MSOP	RM-8	HNA
AD8021ARM-REEL	−40°C to +85°C	8-Lead MSOP	RM-8	HNA
AD8021ARM-REEL7	−40°C to +85°C	8-Lead MSOP	RM-8	HNA
AD8021ARMZ[1]	−40°C to +85°C	8-Lead MSOP	RM-8	HNA#
AD8021ARMZ-REEL[1]	−40°C to +85°C	8-Lead MSOP	RM-8	HNA#
AD8021ARMZ-REEL7[1]	−40°C to +85°C	8-Lead MSOP	RM-8	HNA#

[1]Z = Pb-free part, # denotes lead-free product may be top or bottom marked.

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C01888-0-5/06(F)