# Low Noise, 90 MHz Variable-Gain Amplifier

# AD603*

**FEATURES**
**"Linear in dB" Gain Control**
**Pin Programmable Gain Ranges**
**–11 dB to +31 dB with 90 MHz Bandwidth**
**+9 dB to +51 dB with 9 MHz Bandwidth**
**Any Intermediate Range, e.g., –1 dB to +41 dB with 30 MHz Bandwidth**
**Bandwidth Independent of Variable Gain**
**1.3 nV/√Hz Input Noise Spectral Density**
**±0.5 dB Typical Gain Accuracy**
**MIL-STD-883 Compliant and DESC Versions Available**

**APPLICATIONS**
**RF/IF AGC Amplifier**
**Video Gain Control**
**A/D Range Extension**
**Signal Measurement**

## PRODUCT DESCRIPTION

The AD603 is a low noise, voltage-controlled amplifier for use in RF and IF AGC systems. It provides accurate, pin selectable gains of –11 dB to +31 dB with a bandwidth of 90 MHz or +9 dB to +51 dB with a bandwidth of 9 MHz. Any intermediate gain range may be arranged using one external resistor. The input referred noise spectral density is only 1.3 nV/√Hz and power consumption is 125 mW at the recommended ±5 V supplies.

The decibel gain is "linear in dB," accurately calibrated, and stable over temperature and supply. The gain is controlled at a high impedance (50 MΩ), low bias (200 nA) differential input; the scaling is 25 mV/dB, requiring a gain-control voltage of only 1 V to span the central 40 dB of the gain range. An over- and under-range of 1 dB is provided whatever the selected range. The gain-control response time is less than 1 µs for a 40 dB change.

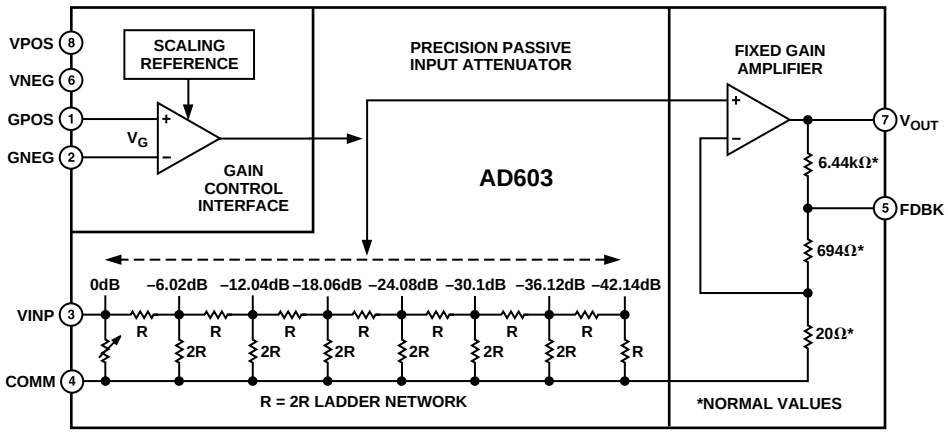
The differential gain-control interface allows the use of either differential or single-ended positive or negative control voltages. Several of these amplifiers may be cascaded and their gain-control gains offset to optimize the system S/N ratio.

The AD603 can drive a load impedance as low as 100 Ω with low distortion. For a 500 Ω load in shunt with 5 pF, the total harmonic distortion for a ±1 V sinusoidal output at 10 MHz is typically –60 dBc. The peak specified output is ±2.5 V minimum into a 500 Ω load, or ±1 V into a 100 Ω load.

The AD603 uses a proprietary circuit topology—the X-AMP™. The X-AMP comprises a variable attenuator of 0 dB to –42.14 dB followed by a fixed-gain amplifier. Because of the attenuator, the amplifier never has to cope with large inputs and can use negative feedback to define its (fixed) gain and dynamic performance. The attenuator has an input resistance of 100 Ω, laser trimmed to ±3%, and comprises a seven-stage R-2R ladder network, resulting in an attenuation between tap points of 6.021 dB. A proprietary interpolation technique provides a continuous gain-control function which is linear in dB.

The AD603A is specified for operation from –40°C to +85°C and is available in both 8-lead SOIC (R) and 8-lead ceramic DIP (Q). The AD603S is specified for operation from –55°C to +125°C and is available in an 8-lead ceramic DIP (Q). The AD603 is also available under DESC SMD 5962-94572.

## FUNCTIONAL BLOCK DIAGRAM




*Patented.
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REV. C



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# AD603—SPECIFICATIONS (@ $T_A$ = +25°C, $V_S$ = ±5 V, –500 mV ≤ $V_G$ ≤ +500 mV, GNEG = 0 V, –10 dB to +30 dB Gain Range, $R_L$ = 500 Ω, and $C_L$ = 5 pF, unless otherwise noted.)

| Model / Parameter | Conditions | AD603 Min | AD603 Typ | AD603 Max | Unit |
|---|---|---|---|---|---|
| INPUT CHARACTERISTICS | | | | | |
| Input Resistance | Pins 3 to 4 | 97 | 100 | **103** | Ω |
| Input Capacitance | | | 2 | | pF |
| Input Noise Spectral Density[1] | Input Short Circuited | | 1.3 | | nV/√Hz |
| Noise Figure | f = 10 MHz, Gain = max, $R_S$ = 10 Ω | | 8.8 | | dB |
| 1 dB Compression Point | f = 10 MHz, Gain = max, $R_S$ = 10 Ω | | –11 | | dBm |
| Peak Input Voltage | | | ±1.4 | ±2 | V |
| OUTPUT CHARACTERISTICS | | | | | |
| –3 dB Bandwidth | $V_{OUT}$ = 100 mV rms | | 90 | | MHz |
| Slew Rate | $R_L$ ≥ 500 Ω | | 275 | | V/µs |
| Peak Output[2] | $R_L$ ≥ 500 Ω | ±2.5 | ±3.0 | | V |
| Output Impedance | f ≤ 10 MHz | | 2 | | Ω |
| Output Short-Circuit Current | | | 50 | | mA |
| Group Delay Change vs. Gain | f = 3 MHz; Full Gain Range | | ±2 | | ns |
| Group Delay Change vs. Frequency | $V_G$ = 0 V; f = 1 MHz to 10 MHz | | ±2 | | ns |
| Differential Gain | | | 0.2 | | % |
| Differential Phase | | | 0.2 | | Degree |
| Total Harmonic Distortion | f = 10 MHz, $V_{OUT}$ = 1 V rms | | –60 | | dBc |
| 3rd Order Intercept | f = 40 MHz, Gain = max, $R_S$ = 50 Ω | | 15 | | dBm |
| ACCURACY | | | | | |
| Gain Accuracy | –500 mV ≤ $V_G$ ≤ +500 mV | | ±0.5 | **±1** | dB |
| $T_{MIN}$ to $T_{MAX}$ | | | | ±1.5 | dB |
| Output Offset Voltage[3] | $V_G$ = 0 V | | | **20** | mV |
| $T_{MIN}$ to $T_{MAX}$ | | | | 30 | mV |
| Output Offset Variation vs. $V_G$ | –500 mV ≤ $V_G$ ≤ +500 mV | | | **20** | mV |
| $T_{MIN}$ to $T_{MAX}$ | | | | 30 | mV |
| GAIN CONTROL INTERFACE | | | | | |
| Gain Scaling Factor | | **39.4** | 40 | **40.6** | dB/V |
| $T_{MIN}$ to $T_{MAX}$ | | 38 | | 42 | dB/V |
| GNEG, GPOS Voltage Range[4] | | –1.2 | | **+2.0** | V |
| Input Bias Current | | | 200 | | nA |
| Input Offset Current | | | 10 | | nA |
| Differential Input Resistance | Pins 1 to 2 | | 50 | | MΩ |
| Response Rate | Full 40 dB Gain Change | | 40 | | dB/µs |
| POWER SUPPLY | | | | | |
| Specified Operating Range | | ±4.75 | | ±6.3 | V |
| Quiescent Current | | | 12.5 | **17** | mA |
| $T_{MIN}$ to $T_{MAX}$ | | | | 20 | mA |

NOTES

[1]Typical open or short-circuited input; noise is lower when system is set to maximum gain and input is short-circuited. This figure includes the effects of both voltage and current noise sources.

[2]Using resistive loads of 500 Ω or greater, or with the addition of a 1 kΩ pull-down resistor when driving lower loads.

[3]The dc gain of the main amplifier in the AD603 is ×35.7; thus, an input offset of 100 µV becomes a 3.57 mV output offset.

[4]GNEG and GPOS, gain control, voltage range is guaranteed to be within the range of $-V_S$ + 4.2 V to $+V_S$ – 3.4 V over the full temperature range of –40°C to +85°C.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

Specifications subject to change without notice.

## ABSOLUTE MAXIMUM RATINGS[1]

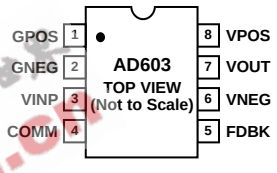
Supply Voltage $\pm V_S$ . . . . . ±7.5 V
Internal Voltage VINP (Pin 3) . . . . . ±2 V Continuous
. . . . . $\pm V_S$ for 10 ms
GPOS, GNEG (Pins 1, 2) . . . . . $\pm V_S$
Internal Power Dissipation[2] . . . . . 400 mW
Operating Temperature Range
AD603A . . . . . –40°C to +85°C
AD603S . . . . . –55°C to +125°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature Range (Soldering 60 sec) . . . . . +300°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Thermal Characteristics:
8-Lead SOIC Package: $\theta_{JA}$ = 155°C/W, $\theta_{JC}$ = 33°C/W
8-Lead Ceramic Package: $\theta_{JA}$ = 140°C/W, $\theta_{JC}$ = 15°C/W

## PIN FUNCTION DESCRIPTIONS

| Pin | Mnemonic | Description |
|---|---|---|
| Pin 1 | GPOS | Gain-Control Input "HI" (Positive Voltage Increases Gain) |
| Pin 2 | GNEG | Gain-Control Input "LO" (Negative Voltage Increases Gain) |
| Pin 3 | VINP | Amplifier Input |
| Pin 4 | COMM | Amplifier Ground |
| Pin 5 | FDBK | Connection to Feedback Network |
| Pin 6 | VNEG | Negative Supply Input |
| Pin 7 | VOUT | Amplifier Output |
| Pin 8 | VPOS | Positive Supply Input |

## CONNECTION DIAGRAMS
### 8-Lead Plastic SOIC (R) Package
### 8-Lead Ceramic DIP (Q) Package




## ORDERING GUIDE

| Part Number | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| AD603AR | –40°C to +85°C | 8-Lead SOIC | SO-8 |
| AD603AQ | –40°C to +85°C | 8-Lead Ceramic DIP | Q-8 |
| AD603SQ/883B* | –55°C to +125°C | 8-Lead Ceramic DIP | Q-8 |
| AD603-EB | | Evaluation Board | |
| AD603ACHIPS | –40°C to +85°C | Die | |
| AD603AR-REEL | –40°C to +85°C | 13" Reel | SO-8 |
| AD603AR-REEL7 | –40°C to +85°C | 7" Reel | SO-8 |

*Refer to AD603 Military data sheet. Also available as 5962-9457203MPA.



## CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD603 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

## THEORY OF OPERATION

The AD603 comprises a fixed-gain amplifier, preceded by a broadband passive attenuator of 0 dB to 42.14 dB, having a gain-control scaling factor of 40 dB per volt. The fixed gain is laser-trimmed in two ranges, to either 31.07 dB (×35.8) or 50 dB (×358), or may be set to any range in between using one external resistor between Pins 5 and 7. Somewhat higher gain can be obtained by connecting the resistor from Pin 5 to common, but the increase in output offset voltage limits the maximum gain to about 60 dB. For any given range, the bandwidth is independent of the voltage-controlled gain. This system provides an under- and overrange of 1.07 dB in all cases; for example, the overall gain is –11.07 dB to 31.07 dB in the maximum-bandwidth mode (Pin 5 and Pin 7 strapped).

This *X-AMP* structure has many advantages over former methods of gain-control based on nonlinear elements. Most importantly, the fixed-gain amplifier can use negative feedback to increase its accuracy. Since large inputs are first attenuated, the amplifier input is always small. For example, to deliver a ±1 V output in the –1 dB/+41 dB mode (that is, using a fixed amplifier gain of 41.07 dB) its input is only 8.84 mV; thus the distortion can be very low. Equally important, the small-signal gain and phase response, and thus the pulse response, are essentially independent of gain.

Figure 1 is a simplified schematic. The input attenuator is a seven-section R-2R ladder network, using untrimmed resistors of nominally R = 62.5 Ω, which results in a characteristic resistance of 125 Ω ± 20%. A shunt resistor is included at the input and laser trimmed to establish a more exact input resistance of 100 Ω ± 3%, which ensures accurate operation (gain and HP corner frequency) when used in conjunction with external resistors or capacitors.

The nominal maximum signal at input VINP is 1 V rms (±1.4 V peak) when using the recommended ±5 V supplies, although operation to ±2 V peak is permissible with some increase in HF distortion and feedthrough. *Pin 4 (SIGNAL COMMON) must be connected directly to the input ground; significant impedance in this connection will reduce the gain accuracy.*

The signal applied at the input of the ladder network is attenuated by 6.02 dB by each section; thus, the attenuation to each of the taps is progressively 0 dB, 6.02 dB, 12.04 dB, 18.06 dB, 24.08 dB, 30.1 dB, 36.12 dB and 42.14 dB. A unique circuit technique is employed to interpolate between these tap-points, indicated by the "slider" in Figure 1, thus providing continuous attenuation from 0 dB to 42.14 dB. It will help, in understanding the AD603, to think in terms of a mechanical means for moving this slider from left to right; in fact, its "position" is controlled by the voltage between Pins 1 and 2. The details of the gain-control interface are discussed later.

The gain is at all times very exactly determined, and a linear-in-dB relationship is automatically guaranteed by the exponential nature of the attenuation in the ladder network (the X-AMP principle). In practice, the gain deviates slightly from the ideal law, by about ±0.2 dB peak (see, for example, Figure 16).

### Noise Performance

An important advantage of the X-AMP is its superior noise performance. The nominal resistance seen at inner tap points is 41.7 Ω (one third of 125 Ω), which exhibits a Johnson noise-spectral density (NSD) of 0.83 nV/√Hz (that is, $\sqrt{4kTR}$) at 27°C, which is a large fraction of the total input noise. The first stage of the amplifier contributes a further 1 nV/√Hz, for a total input noise of 1.3 nV/√Hz. It will be apparent that it is essential to use a low resistance in the ladder network to achieve the very low specified noise level. The signal's source impedance forms a voltage divider with the AD603's 100 Ω input resistance. In some applications, the resulting attenuation may be unacceptable, requiring the use of an external buffer or preamplifier to match a high impedance source to the low impedance AD603.

The noise at maximum gain (that is, at the 0 dB tap) depends on whether the input is short-circuited or open-circuited: when shorted, the minimum NSD of slightly over 1 nV/√Hz is achieved; when open, the resistance of 100 Ω looking into the first tap generates 1.29 nV/√Hz, so the noise increases to a total of 1.63 nV/√Hz. (This last calculation would be important if the AD603 were preceded by, for example, a 900 Ω resistor to allow operation from inputs up to 10 V rms.) As the selected tap moves away from the input, the dependence of the noise on source impedance quickly diminishes.

Apart from the small variations just discussed, the signal-to-noise (S/N) ratio at the output is essentially independent of the attenuator setting. For example, on the –11 dB/+31 dB range the fixed gain of ×35.8 raises the output NSD to 46.5 nV/√Hz. Thus, for the maximum undistorted output of 1 V rms and a 1 MHz bandwidth, the output S/N ratio would be 86.6 dB, that is, 20 log (1 V/46.5 μV).

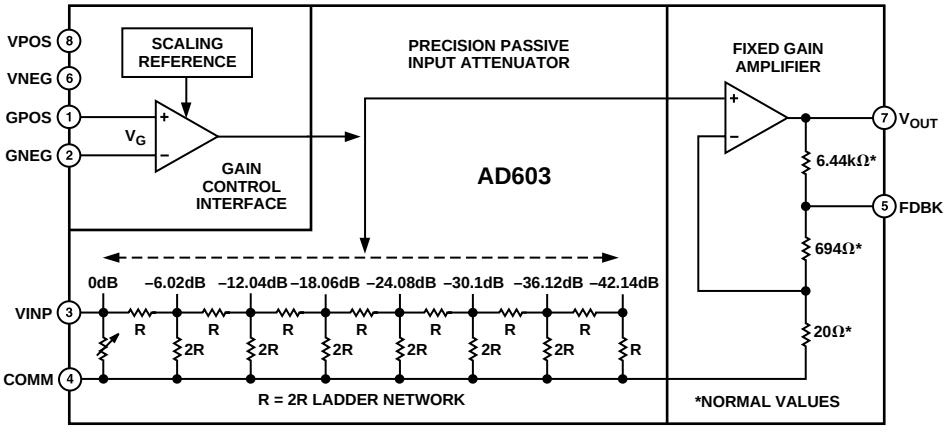



*Figure 1. Simplified Block Diagram of the AD603*

**The Gain-Control Interface**

The attenuation is controlled through a differential, high-impedance (50 MΩ) input, with a scaling factor which is laser-trimmed to 40 dB per volt, that is, 25 mV/dB. An internal bandgap reference ensures stability of the scaling with respect to supply and temperature variations.

When the differential input voltage $V_G$ = 0 V, the attenuator "slider" is centered, providing an attenuation of 21.07 dB. For the maximum bandwidth range, this results in an overall gain of 10 dB (= –21.07 dB + 31.07 dB). When the control input is –500 mV, the gain is lowered by 20 dB (= 0.500 V × 40 dB/V), to –10 dB; when set to +500 mV, the gain is increased by 20 dB, to 30 dB. When this interface is overdriven in either direction, the gain approaches either –11.07 dB (= –42.14 dB + 31.07 dB) or 31.07 dB (= 0 + 31.07 dB), respectively. The only constraint on the gain-control voltage is that it be kept within the common-mode range (–1.2 V to +2.0 V assuming +5 V supplies) of the gain control interface.

The basic gain of the AD603 can thus be calculated using the following simple expression:

$$Gain\ (dB) = 40\ V_G + 10 \quad (1)$$

where $V_G$ is in volts. When Pins 5 and 7 are strapped (see next section) the gain becomes

$$Gain\ (dB) = 40\ V_G + 20\ for\ 0\ to\ +40\ dB$$

and

$$Gain\ (dB) = 40\ V_G + 30\ for\ +10\ to\ +50\ dB \quad (2)$$

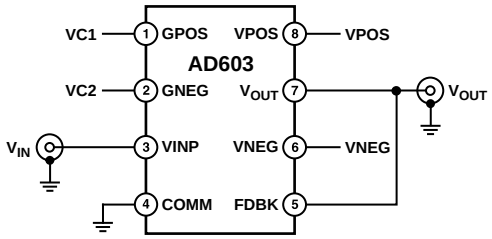
The high impedance gain-control input ensures minimal loading when driving many amplifiers in multiple channel or cascaded applications. The differential capability provides flexibility in choosing the appropriate signal levels and polarities for various control schemes.

For example, if the gain is to be controlled by a DAC providing a positive only ground-referenced output, the "Gain Control LO" (GNEG) pin should be biased to a fixed offset of +500 mV, to set the gain to –10 dB when "Gain Control HI" (GPOS) is at zero, and to 30 dB when at +1.00 V.

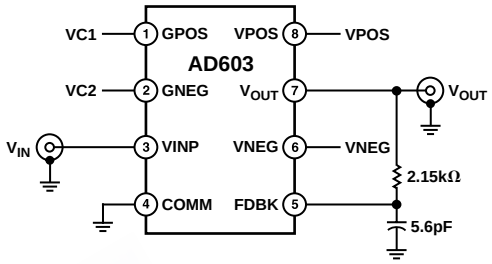
It is a simple matter to include a voltage divider to achieve other scaling factors. When using an 8-bit DAC having an FS output of +2.55 V (10 mV/bit), a divider ratio of 2 (generating 5 mV/bit) would result in a gain-setting resolution of 0.2 dB/bit. The use of such offsets is valuable when two AD603s are cascaded, when various options exist for optimizing the S/N profile, as will be shown later.

**Programming the Fixed-Gain Amplifier Using Pin Strapping**

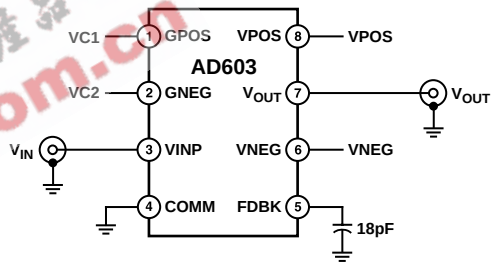
Access to the feedback network is provided at Pin 5 (FDBK). The user may program the gain of the AD603's output amplifier using this pin, as shown in Figure 2. There are three modes: in the default mode, FDBK is unconnected, providing the range +9 dB/+51 dB; when $V_{OUT}$ and FDBK are shorted, the gain is lowered to –11 dB/+31 dB; when an external resistor is placed between $V_{OUT}$ and FDBK any intermediate gain can be achieved, for example, –1 dB/+41 dB. Figure 3 shows the nominal maximum gain versus external resistor for this mode.




*a. –10 dB to +30 dB; 90 MHz Bandwidth*




*b. 0 dB to +40 dB; 30 MHz Bandwidth*




*c. +10 dB to +50 dB; 9 MHz Bandwidth*

*Figure 2. Pin Strapping to Set Gain*

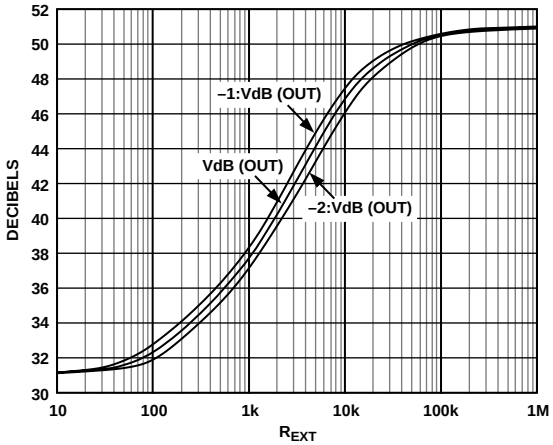



*Figure 3. Gain vs. $R_{EXT}$, Showing Worst-Case Limits Assuming Internal Resistors Have a Maximum Tolerance of 20%*

Optionally, when a resistor is placed from FDBK to COMM, higher gains can be achieved. This fourth mode is of limited value because of the low bandwidth and the elevated output offsets; it is thus not included in Figure 2.

The gain of this amplifier in the first two modes is set by the ratio of on-chip laser-trimmed resistors. While the ratio of these resistors is very accurate, the absolute value of these resistors can vary by as much as ±20%. Thus, when an external resistor is connected in parallel with the nominal 6.44 kΩ ± 20% internal resistor, the overall gain accuracy is somewhat poorer. The worst-case error occurs at about 2 kΩ (see Figure 4).

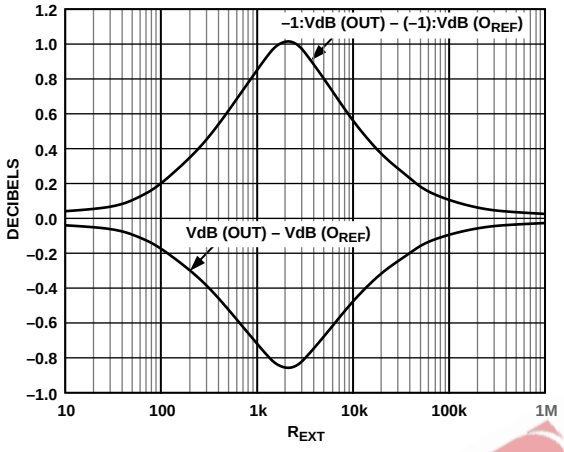



*Figure 4. Worst-Case Gain Error, Assuming Internal Resistors Have a Maximum Tolerance of –20% (Top Curve) or +20% (Bottom Curve)*

While the gain-bandwidth product of the fixed-gain amplifier is about 4 GHz, the actual bandwidth is not exactly related to the maximum gain. This is because there is a slight enhancing of the ac response magnitude on the maximum bandwidth range, due to higher order poles in the open-loop gain function; this mild peaking is not present on the higher gain ranges. Figure 2 shows how optional capacitors may be added to extend the frequency response in high gain modes.

## CASCADING TWO AD603S

Two or more AD603s can be connected in series to achieve higher gain. Invariably, ac coupling must be used to prevent the dc offset voltage at the output of each amplifier from overloading the following amplifier at maximum gain. The required high pass coupling network will usually be just a capacitor, chosen to set the desired corner frequency in conjunction with the well-defined 100 Ω input resistance of the following amplifier.

For two AD603s, the total gain-control range becomes 84 dB (two times 42.14 dB); the overall –3 dB bandwidth of cascaded stages will be somewhat reduced. Depending on the pin-strapping, the gain and bandwidth for two cascaded amplifiers can range from –22 dB to +62 dB (with a bandwidth of about 70 MHz) to +22 dB to +102 dB (with a bandwidth of about 6 MHz).

There are several ways of connecting the gain-control inputs in cascaded operation. The choice depends on whether it is important to achieve the highest possible Instantaneous Signal-to-Noise Ratio (ISNR), or, alternatively, to minimize the ripple in the gain error. The following examples feature the AD603 programmed for maximum bandwidth; the explanations apply to other gain/bandwidth combinations with appropriate changes to the arrangements for setting the maximum gain.

### Sequential Mode (Optimal S/N Ratio)

In the sequential mode of operation, the ISNR is maintained at its highest level for as much of the gain control range possible. Figure 5 shows the SNR over a gain range of –22 dB to +62 dB, assuming an output of 1 V rms and a 1 MHz bandwidth; Figure 6 shows the general connections to accomplish this. Here, both the positive gain-control inputs (GPOS) are driven in parallel by a positive-only, ground-referenced source with a range of 0 V to +2 V, while the negative gain-control inputs (GNEG) arc biased by stable voltages to provide the needed gain-offsets. These voltages may be provided by resistive dividers operating from a common voltage reference.

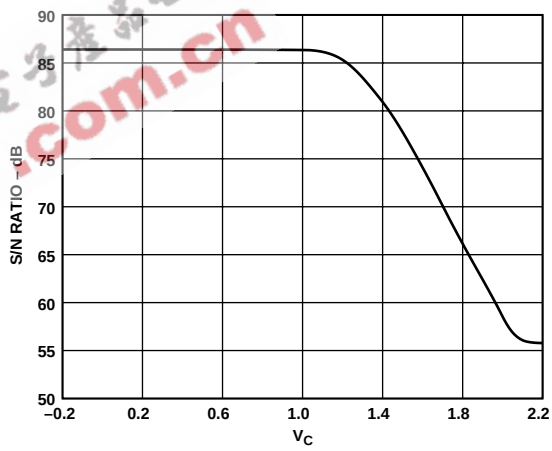



*Figure 5. SNR vs. Control Voltage—Sequential Control (1 MHz Bandwidth)*

The gains are offset (Figure 7) such that A2's gain is increased only after A1's gain has reached its maximum value. Note that for a differential input of –600 mV or less, the gain of a single amplifier (A1 or A2) will be at its minimum value of –11.07 dB; for a differential input of +600 mV or more, the gain will be at its maximum value of 31.07 dB. Control inputs beyond these limits will not affect the gain and can be tolerated without damage or foldover in the response. This is an important aspect of the AD603's gain-control response. (See the Specifications section of this data sheet for more details on the allowable voltage range) The gain is now

$$Gain\ (dB) = 40\ V_G + G_O \qquad (3)$$

where $V_G$ is the applied control voltage and $G_O$ is determined by the gain range chosen. In the explanatory notes that follow, we assume the maximum-bandwidth connections are used, for which $G_O$ is –20 dB.

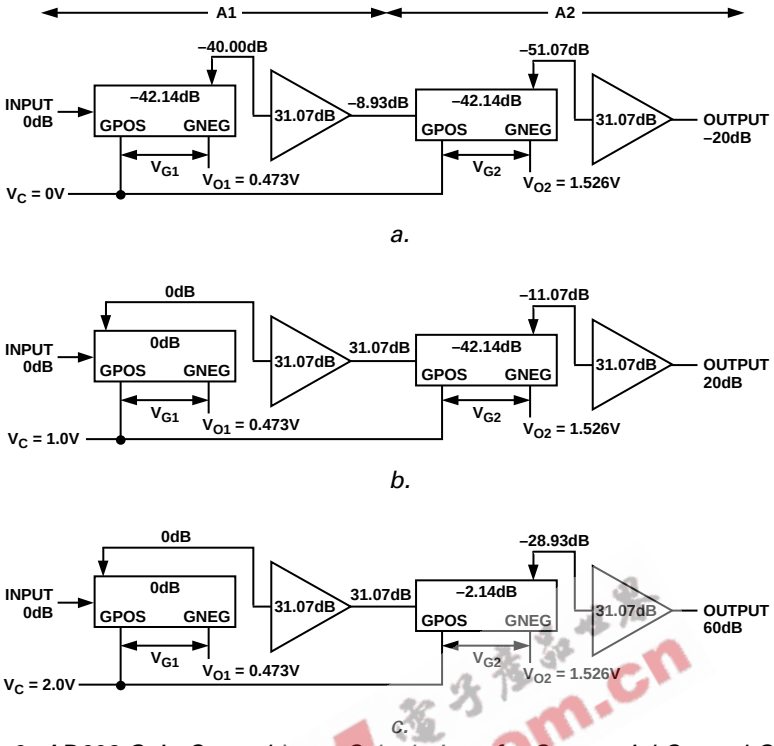



*Figure 6. AD603 Gain Control Input Calculations for Sequential Control Operation*

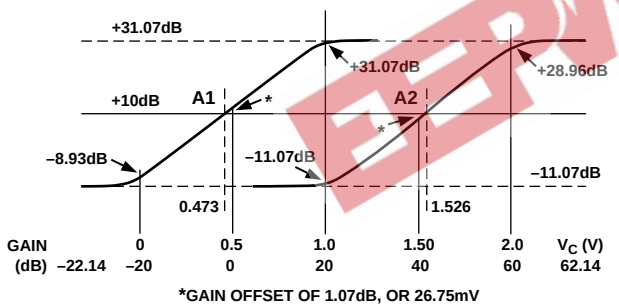



*Figure 7. Explanation of Offset Calibration for Sequential Control*

With reference to Figure 6, note that $V_{G1}$ refers to the differential gain-control input to A1 and $V_{G2}$ refers to the differential gain-control input to A2. When $V_G$ is zero, $V_{G1}$ = –473 mV and thus the gain of A1 is –8.93 dB (recall that the gain of each individual amplifier in the maximum-bandwidth mode is –10 dB for $V_G$ = –500 mV and 10 dB for $V_G$ = 0 V); meanwhile, $V_{G2}$ = –1.908 V so the gain of A2 is "pinned" at –11.07 dB. The overall gain is thus –20 dB. This situation is shown in Figure 6a.

When $V_G$ = +1.00 V, $V_{G1}$ = 1.00 V – 0.473 V = +0.526 V, which sets the gain of A1 to at nearly its maximum value of 31.07 dB, while $V_{G2}$ = 1.00 V – 1.526 V = 0.526 V, which sets A2's gain at nearly its minimum value –11.07 dB. Close analysis shows that the degree to which neither AD603 is completely pushed to its maximum or minimum gain exactly cancels in the overall gain, which is now +20 dB. This is depicted in Figure 6b.

When $V_G$ = +2.0 V, the gain of A1 is pinned at 31.07 dB and that of A2 is near its maximum value of 28.93 dB, resulting in an overall gain of 60 dB (see Figure 6c). This mode of operation is further clarified by Figure 8, which is a plot of the separate gains of A1 and A2 and the overall gain versus the control voltage. Figure 9 is a plot of the gain error of the cascaded amplifiers versus the control voltage. Figure 10 is a plot of the gain error of the cascaded stages versus the control voltages.

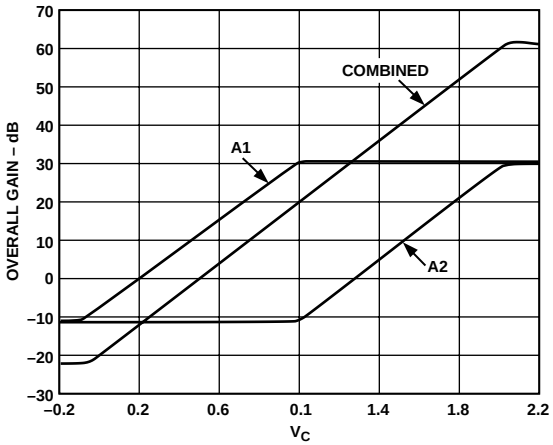



*Figure 8. Plot of Separate and Overall Gains in Sequential Control*

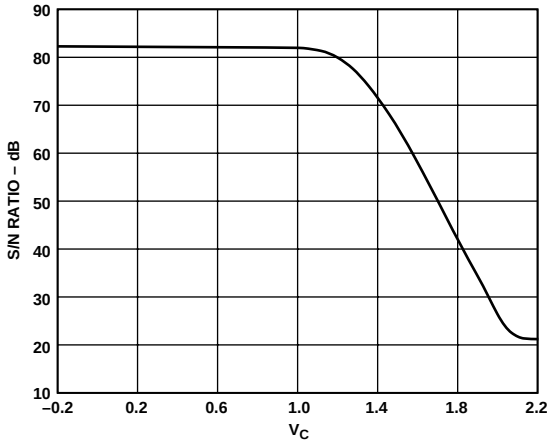



*Figure 9. SNR for Cascaded Stages—Sequential Control*

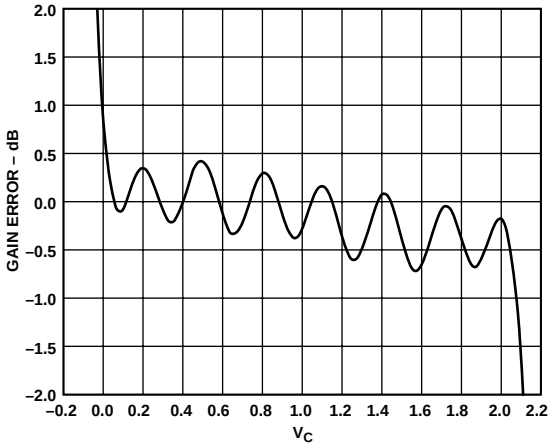



*Figure 11. Gain Error for Cascaded Stages–Parallel Control*

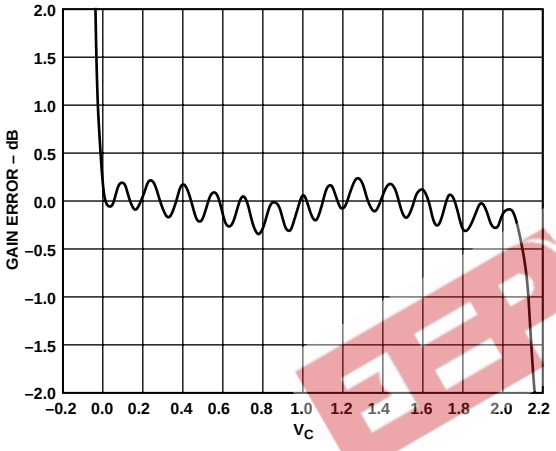



*Figure 10. Gain Error for Cascaded Stages—Sequential Control*

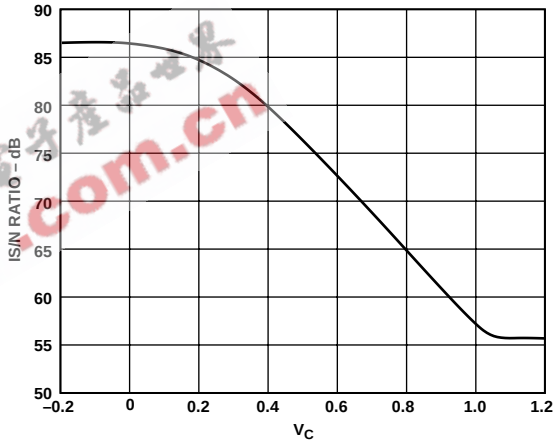



*Figure 12. ISNR for Cascaded Stages–Parallel Control*

**Parallel Mode (Simplest Gain-Control Interface)**

In this mode, the gain-control of voltage is applied to both inputs in parallel—the GPOS pins of both A1 and A2 are connected to the control voltage and the GNEW inputs are grounded. The gain scaling is then doubled to 80 dB/V, requiring only a 1.00 V change for an 80 dB change of gain:

$$Gain\ (dB) = 80\ V_G + G_O \qquad (4)$$

where, as before $G_O$ depends on the range selected; for example, in the maximum-bandwidth mode, $G_O$ is +20 dB. Alternatively, the GNEG pins may be connected to an offset voltage of +0.500 V, in which case, $G_O$ is –20 dB.

The amplitude of the gain ripple in this case is also doubled, as shown in Figure 11, while the instantaneous signal-to-noise ratio at the output of A2 now decreases linearly as the gain increased (Figure 12).

**Low Gain Ripple Mode (Minimum Gain Error)**

As can be seen from Figures 9 and 10, the error in the gain is periodic, that is, it shows a small ripple. (Note that there is also a variation in the *output offset voltage*, which is due to the gain interpolation, but this is not exact in amplitude.) By offsetting the gains of A1 and A2 by half the period of the ripple, that is, by 3 dB, the residual gain errors of the two amplifiers can be made to cancel. Figure 13 shows that much lower gain ripple when configured in this manner. Figure 14 plots the ISNR as a function of gain; it is very similar to that in the "Parallel Mode."

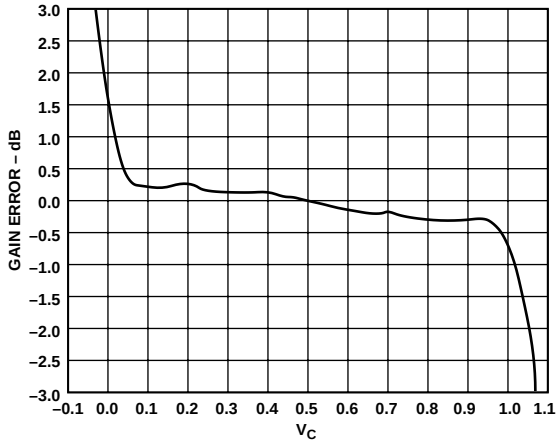



*Figure 13. Gain Error for Cascaded Stages–Low Ripple Mode*

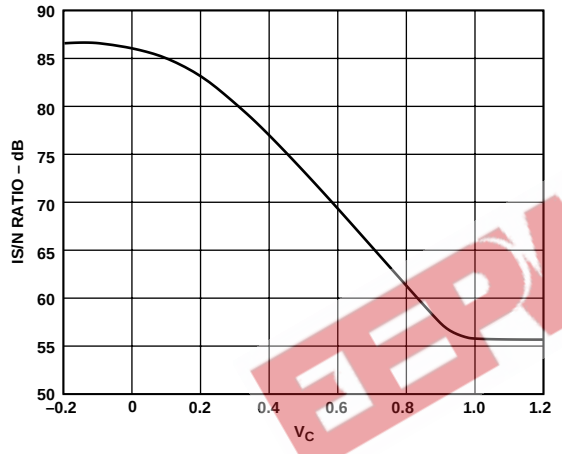



*Figure 14. ISNR vs. Control Voltage–Low Ripple Mode*

## THEORY OF THE AD603

### A Low Noise AGC Amplifier

Figure 15 shows the ease with which the AD603 can be connected as an AGC amplifier. The circuit illustrates many of the points previously discussed: It uses few parts, has linear-in-dB gain, operates from a single supply, uses two cascaded amplifiers in sequential gain mode for maximum S/N ratio, and an external resistor programs each amplifier's gain. It also uses a simple temperature-compensated detector.

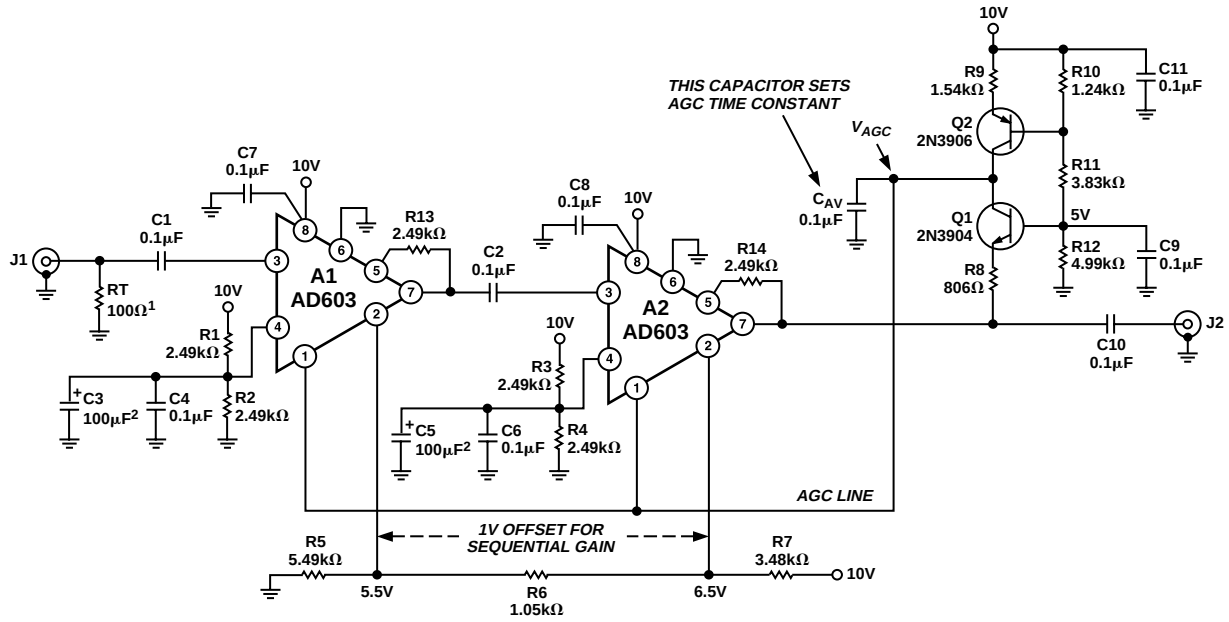
The circuit operates from a single 10 V supply. Resistors R1, R2, R3, and R4 bias the common pins of A1 and A2 at 5 V. This pin is a low impedance point and must have a low impedance path to ground, here provided by the 100 µF tantalum capacitors and the 0.1 µF ceramic capacitors.

The cascaded amplifiers operate in sequential gain. Here, the offset voltage between the pins 2 (GNEG) of A1 and A2 is 1.05 V (42.14 dB × 25 mV/dB), provided by a voltage divider consisting of resistors R5, R6, and R7. Using standard values, the offset is not exact, but it is not critical for this application.

The gain of both A1 and A2 is programmed by resistors R13 and R14, respectively, to be about 42 dB; thus the maximum gain of the circuit is twice that, or 84 dB. The gain-control range can be shifted up by as much as 20 dB by appropriate choices of R13 and R14.

The circuit operates as follows. A1 and A2 are cascaded. Capacitor C1 and the 100 Ω of resistance at the input of A1 form a time-constant of 10 µs. C2 blocks the small dc offset voltage at the output of A1 (which might otherwise saturate A2 at its maximum gain) and introduces a high-pass corner at about 16 kHz, eliminating low frequency noise.

A half-wave detector is used, based on Q1 and R8. The current into capacitor $C_{AV}$ is just the difference between the collector current of Q2 (biased to be 300 µA at 300 K, 27°C) and the collector current of Q1, which increases with the amplitude of the




NOTES
[1]$R_T$ PROVIDES A 50Ω INPUT IMPEDANCE
[2]C3 AND C5 ARE TANTALUM

*Figure 15. A Low Noise AGC Amplifier*

output signal. The automatic gain control voltage, $V_{AGC}$, is the time-integral of this *error* current. In order for $V_{AGC}$ (and thus the gain) to remain insensitive to short-term amplitude fluctuations in the output signal, the rectified current in Q1 must, on average, exactly balance the current in Q2. If the output of A2 is too small to do this, $V_{AGC}$ will increase, causing the gain to increase, until Q1 conducts sufficiently.

Consider the case where R8 is zero and the output voltage $V_{OUT}$ is a square wave at, say, 455 kHz, which is well above the corner frequency of the control loop.

During the time $V_{OUT}$ is negative with respect to the base voltage of Q1, Q1 conducts; when $V_{OUT}$ is positive, it is cut off. Since the average collector current of Q1 is forced to be 300 μA, and the square wave has a duty-cycle of 1:1, Q1's collector current when conducting must be 600 μA. With R8 omitted, the peak amplitude of $V_{OUT}$ is forced to be just the $V_{BE}$ of Q1 at 600 μA, typically about 700 mV, or 2 $V_{BE}$ peak-to-peak. This voltage, hence the amplitude at which the output stabilizes, has a strong negative temperature coefficient (TC), typically –1.7 mV/°C. Although this may not be troublesome in some applications, the correct value of R8 will render the output stable with temperature.

To understand this, first note that the current in Q2 is made to be proportional to absolute temperature (PTAT). For the moment, continue to assume that the signal is a square wave.

When Q1 is conducting, $V_{OUT}$ is now the sum of $V_{BE}$ and a voltage that is PTAT and which can be chosen to have an equal but opposite TC to that of the $V_{BE}$. This is actually nothing more than an application of the "bandgap voltage reference" principle. When R8 is chosen such that the sum of the voltage across it and the $V_{BE}$ of Q1 is close to the bandgap voltage of about 1.2 V, $V_{OUT}$ will be stable over a wide range of temperatures, provided, of course, that Q1 and Q2 share the same thermal environment.

Since the average emitter current is 600 μA during each half-cycle of the square wave a resistor of 833 Ω would add a PTAT voltage of 500 mV at 300 K, increasing by 1.66 mV/°C. In practice, the optimum value will depend on the type of transistor used and, to a lesser extent, on the waveform for which the temperature stability is to be optimized; for the inexpensive 2N3904/2N306 pair and sine wave signals, the recommended value is 806 Ω.

This resistor also serves to lower the peak current in Q1 when more typical signals (usually, sinusoidal) are involved, and the 1.8 kHz LP filter it forms with $C_{AV}$ helps to minimize distortion due to ripple in $V_{AGC}$. Note that the output amplitude under sine wave conditions will be higher than for a square wave, since the average value of the current *for an ideal rectifier* would be 0.637 times as large, causing the output amplitude to be 1.88 (=1.2/0.637) V, or 1.33 V rms. In practice, the somewhat nonideal rectifier results in the sine wave output being regulated to about 1.4 V rms, or 3.6 V p-p.

The bandwidth of the circuit exceeds 40 MHz. At 10.7 MHz, the AGC threshold is 100 μV (–67 dBm) and its maximum gain is 83 dB (20 log 1.4 V/100 μV). The circuit holds its output at 1.4 V rms for inputs as low as –67 dBm to +15 dBm (82 dB), where the input signal exceeds the AD603's maximum input rating. For a 30 dBm input at 10.7 MHz, the second harmonic is 34 dB down from the fundamental and the third harmonic is 35 dB down.

**CAUTION**

Careful component selection, circuit layout, power-supply decoupling, and shielding are needed to minimize the AD603's susceptibility to interference from radio and TV stations, etc. In bench evaluation, we recommend placing all of the components in a shielded box and using feedthrough decoupling networks for the supply voltage. Circuit layout and construction are also critical, since stray capacitances and lead inductances can form resonant circuits and are a potential source of circuit peaking, oscillation, or both.

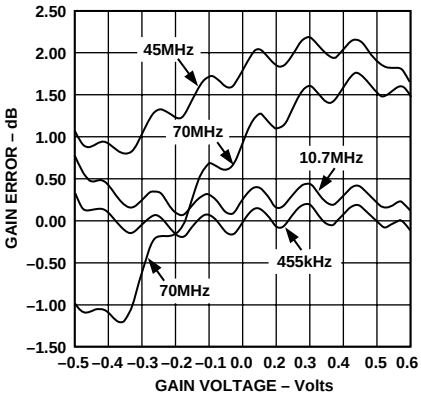



Figure 16. Gain Error vs. Gain Control Voltage at 455 kHz, 10.7 MHz, 45 MHz, 70 MHz

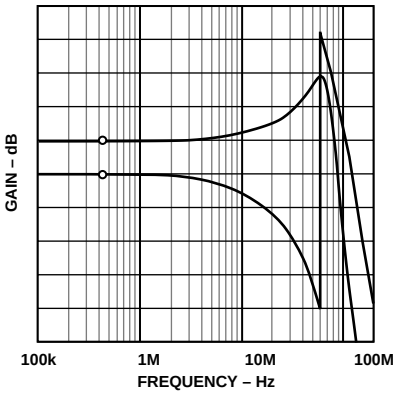



Figure 17. Frequency and Phase Response vs. Gain (Gain = –10 dB, $P_{IN}$ = –30 dBm, Pin 5 Connected to Pin 7)

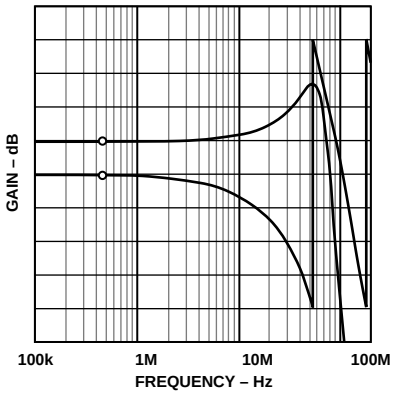



Figure 18. Frequency and Phase Response vs. Gain (Gain = +10 dB, $P_{IN}$ = –30 dBm, Pin 5 Connected to Pin 7)

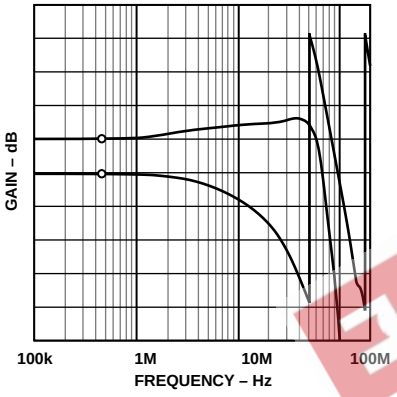



Figure 19. Frequency and Phase Response vs. Gain (Gain = +30 dB, $P_{IN}$ = –30 dBm, Pin 5 Connected to Pin 7)

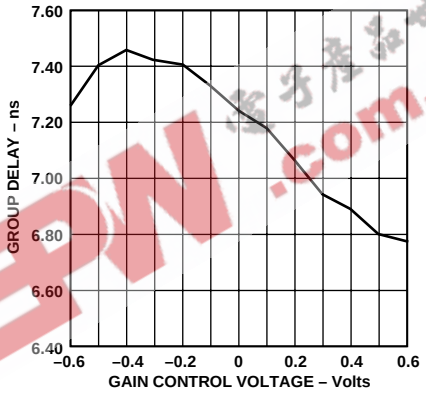



Figure 20. Group Delay vs. Gain Control Voltage

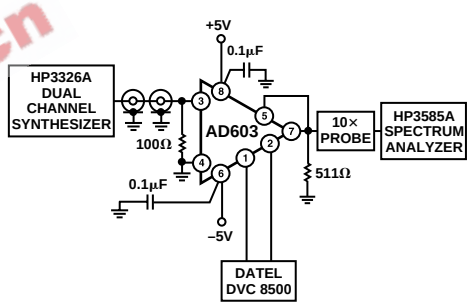



Figure 21. Third Order Intermodulation Distortion Test Setup

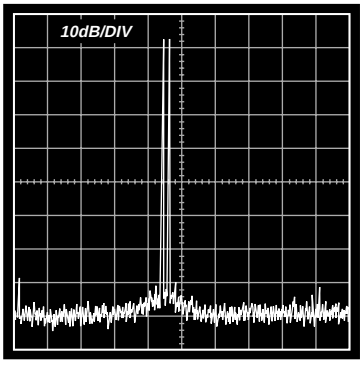



Figure 22. Third Order Intermodulation Distortion at 455 kHz (10× Probe Used to HP3585A Spectrum Analyzer, Gain = 0 dB, $P_{IN}$ = 0 dBm, Pin 5 Connected to Pin 7)

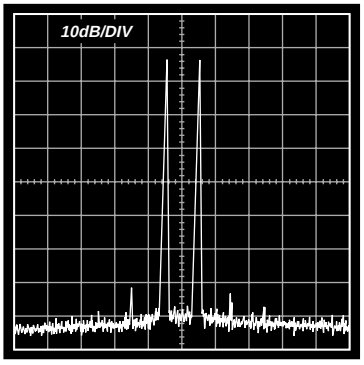



Figure 23. Third Order Intermodulation Distortion at 10.7 MHz (10× Probe Used to HP3585A Spectrum Analyzer, Gain = 0 dB, $P_{IN}$ = 0 dBm, Pin 5 Connected to Pin 7)

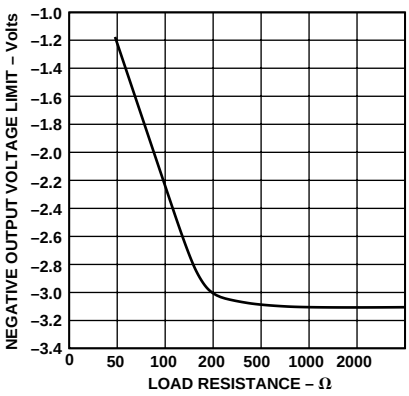



Figure 24. Typical Output Voltage Swing vs. Load Resistance (Negative Output Swing Limits First)

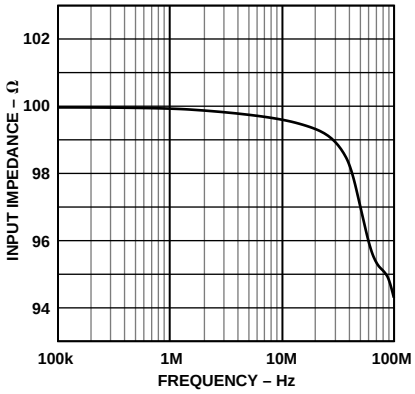



*Figure 25. Input Impedance vs. Frequency (Gain = –10 dB)*

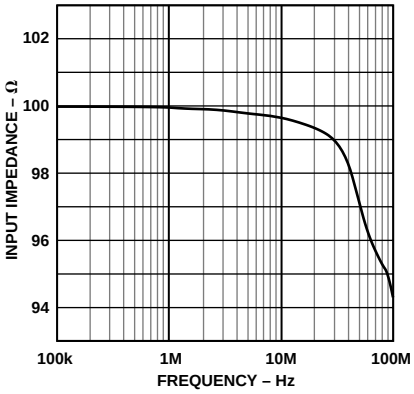



*Figure 26. Input Impedance vs. Frequency (Gain = +10 dB)*

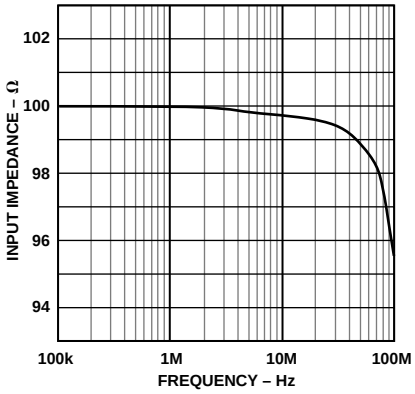



*Figure 27. Input Impedance vs. Frequency (Gain = +30 dB)*

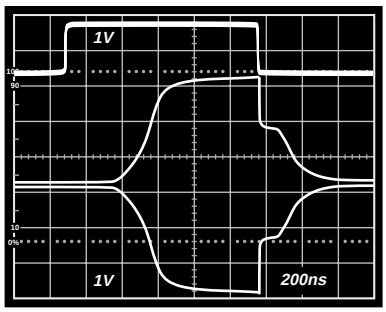



*Figure 28. Gain-Control Channel Response Time*

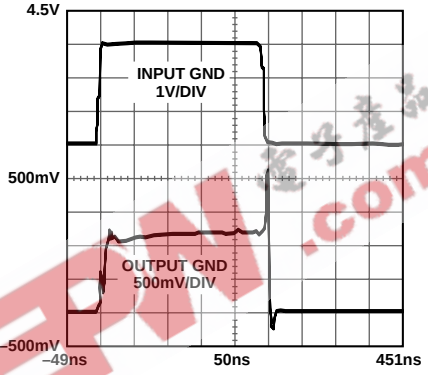



*Figure 29. Input Stage Overload Recovery Time, Pin 5 Connected to Pin 7 (Input Is 500 ns Period, 50% Duty-Cycle Square Wave, Output Is Captured Using Tektronix 11402 Digitizing Oscilloscope)*

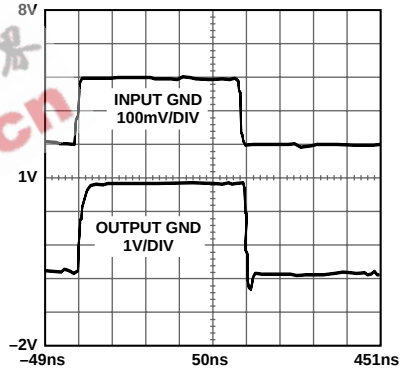



*Figure 30. Output Stage Overload Recovery Time, Pin 5 Connected to Pin 7 (Input Is 500 ns Period, 50% Duty-Cycle Square Wave, Output Is Captured Using Tektronix 11402 Digitizing Oscilloscope)*

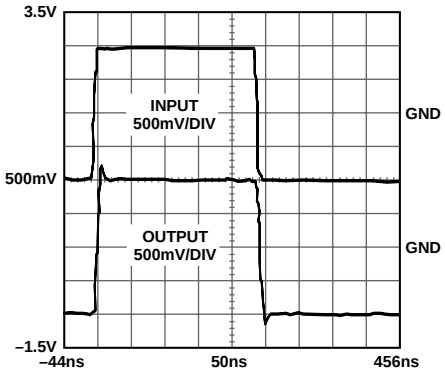



*Figure 31. Transient Response, G = 0 dB, Pin 5 Connected to Pin 7 (Input is 500 ns Period, 50% Duty-Cycle Square Wave, Output Is Captured Using Tektronix 11402 Digitizing Oscilloscope)*

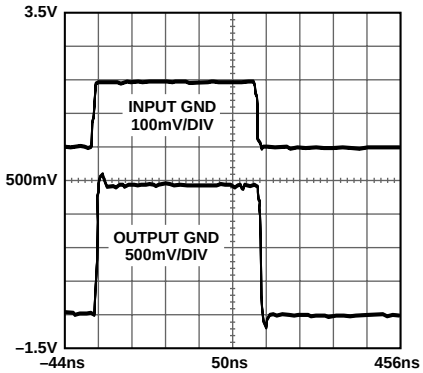



*Figure 32. Transient Response, G = +20 dB, Pin 5 Connected to Pin 7 (Input is 500 ns Period, 50% Duty-Cycle Square Wave, Output Is Captured Using Tektronix 11402 Digitizing Oscilloscope)*

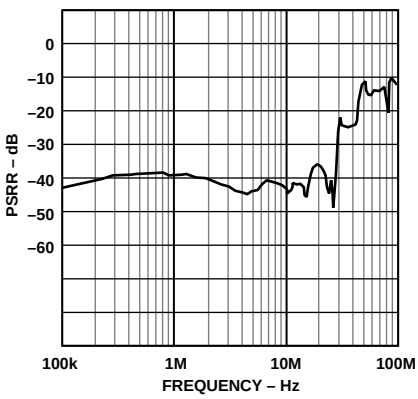



*Figure 33. PSRR vs. Frequency (Worst Case Is Negative Supply PSRR, Shown Here)*

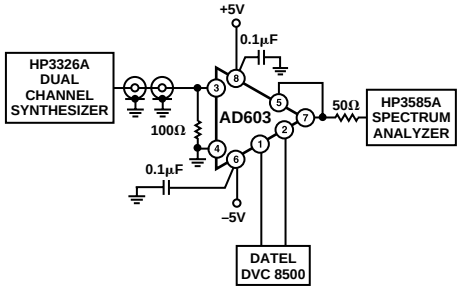



*Figure 34. Test Setup Used for: Noise Figure, 3rd Order Intercept and 1 dB Compression Point Measurements*

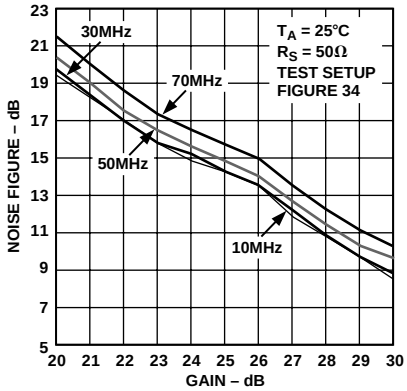



*Figure 35. Noise Figure in –10 dB/ +30 dB Mode*

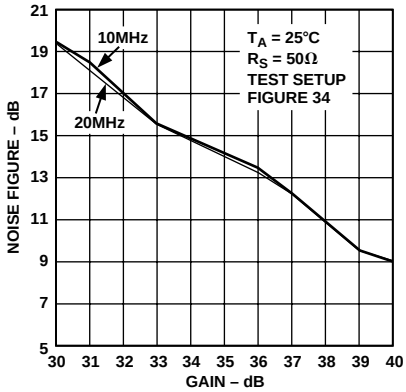



*Figure 36. Noise Figure in 0 dB/+40 dB Mode*

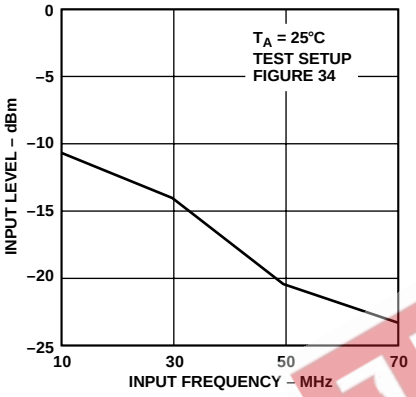



*Figure 37. 1 dB Compression Point, –10 dB/+30 dB Mode, Gain = 30 dB*

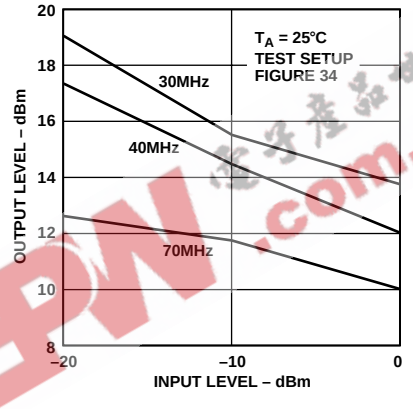



*Figure 38. 3rd Order Intercept –10 dB/ +30 dB Mode, Gain = 10 dB*

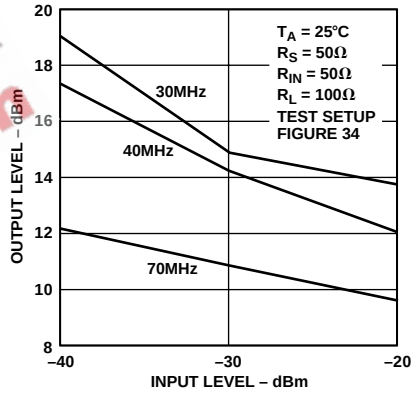
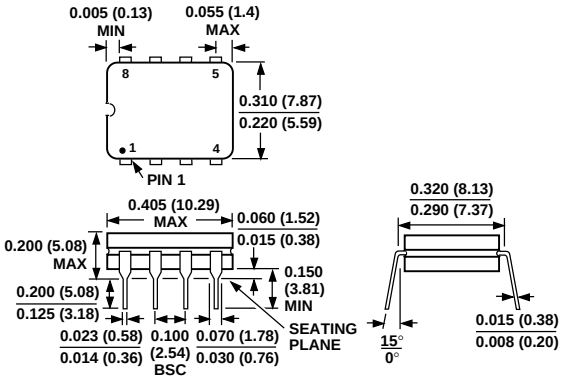



*Figure 39. 3rd Order Intercept, –10 dB/ +30 dB Mode, Gain = 30 dB*

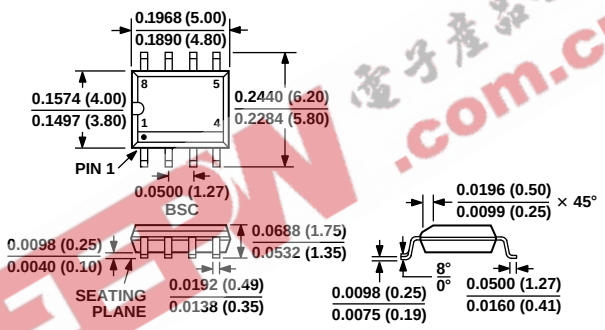
## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

### 8-Lead Cerdip (Q-8)




### 8-Lead SOIC (SO-8)



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