Nonvolatile Memory, 1024-Position Digital Potentiometers

AD5231*

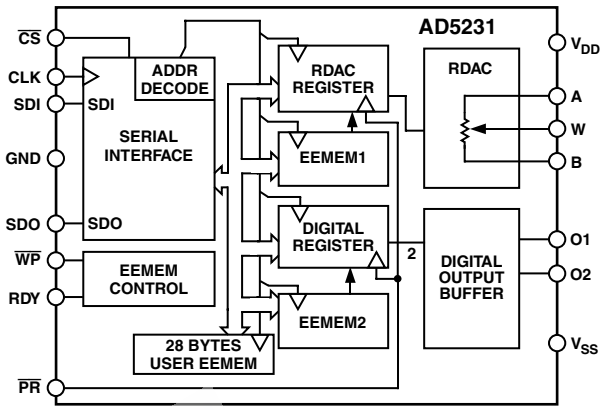
FEATURES

Nonvolatile Memory[1] Preset Maintains Wiper Settings
1024-Position Resolution
Full Monotonic Operation
10 kΩ, 50 kΩ, and 100 kΩ Terminal Resistance
Permanent Memory Write-Protection
Wiper Settings Read Back
Linear Increment/Decrement
Log Taper Increment/Decrement
Push Button Increment/Decrement Compatible
SPI Compatible Serial Interface with Readback Function
3 V to 5 V Single Supply or ±2.5 V Dual Supply
28 Bytes User Nonvolatile Memory for Constant Storage
100 Year Typical Data Retention T_A = 55°C

APPLICATIONS

Mechanical Potentiometer Replacement
Instrumentation: Gain, Offset Adjustment
Programmable Voltage to Current Conversion
Programmable Filters, Delays, Time Constants
Line Impedance Matching
Power Supply Adjustment
Low Resolution DAC Replacement

FUNCTIONAL BLOCK DIAGRAM



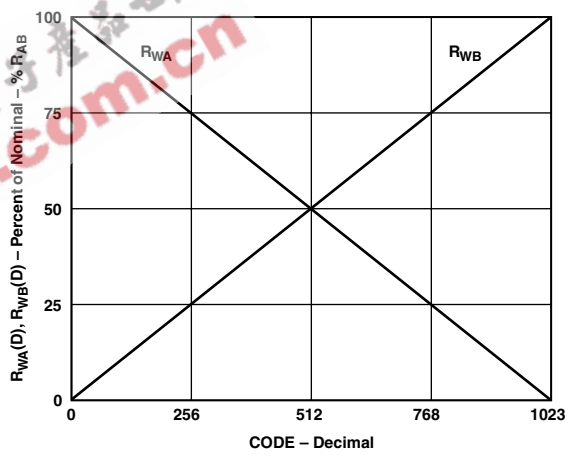


Figure 1. $R_{WA}(D)$ and $R_{WB}(D)$ vs. Decimal Code

GENERAL DESCRIPTION

The AD5231 provides nonvolatile memory digitally controlled potentiometers[2] with 1024-position resolution. These devices perform the same electronic adjustment function as a mechanical potentiometer. The AD5231's versatile programming via a standard 3-wire serial interface allows 16 modes of operation and adjustment, including scratch pad programming, memory storing and retrieving, increment/decrement, log taper adjustment, wiper setting read back, and extra user-defined EEMEM.

In the scratch pad programming mode, a specific setting can be programmed directly to the RDAC[2] register, which sets the resistance at terminals W-A and W-B. The RDAC register can also be loaded with a value previously stored in the EEMEM[1] register. The value in the EEMEM can be changed or protected. When changes are made to the RDAC register, the value of the new setting can be saved into the EEMEM. Thereafter, such value will be transferred automatically to the RDAC register during system power ON. It is enabled by the internal preset strobe. EEMEM can also be retrieved through direct programming and external preset pin control.

Other operations include linear step increment and decrement commands such that the setting in the RDAC register can be moved UP or DOWN, one step at a time. For logarithmic changes in wiper setting, a left/right bit shift command adjusts the level in ±6 dB steps.

The AD5231 is available in thin TSSOP-16 package. All parts are guaranteed to operate over the extended industrial temperature range of –40°C to +85°C.

NOTES
[1]The terms Nonvolatile Memory and EEMEM are used interchangeably.
[2]The terms Digital Potentiometer and RDAC are used interchangeably.
*Patent pending

REV. 0

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AD5231–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS 10 kΩ, 50 kΩ, 100 kΩ VERSIONS

(V_{DD} = 3 V ± 10% or 5 V ± 10% and V_{SS} = 0 V, V_A = +V_{DD}, V_B = 0 V, –40°C < T_A < +85°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS RHEOSTAT MODE						
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}, V_A = NC, Monotonic	–1	±1/2	+1.8	LSB
Resistor Integral Nonlinearity[2]	R-INL	R_{WB}, V_A = NC	–0.2		+0.2	% FS
Nominal Resistor Tolerance	ΔR_{WB}	D = $3FF_H$	–40		+20	%
Resistance Temperature Coefficient	$\Delta R_{AB}/\Delta T$			600		ppm/°C
Wiper Resistance	R_W	I_W = 100 µA, V_{DD} = 5.5 V, Code = Half-Scale		15	100	Ω
		I_W = 100 µA, V_{DD} = 3 V, Code = Half-Scale		50		Ω
DC CHARACTERISTICS POTENTIOMETER DIVIDER MODE						
Resolution	N		10			Bits
Differential Nonlinearity[3]	DNL	Monotonic, T_A = 25°C	–1	±1/2	+1	LSB
		Monotonic, T_A = –40°C or +85°C	–1		+1.25	LSB
Integral Nonlinearity[3]	INL		–0.4		+0.4	% FS
Voltage Divider Temperature Coefficient	$\Delta V_W/\Delta T$	Code = Half-Scale		15		ppm/°C
Full-Scale Error	V_{WFSE}	Code = Full-Scale	–3		0	% FS
Zero-Scale Error	V_{WZSE}	Code = Zero-Scale	0		+1.5	% FS
RESISTOR TERMINALS						
Terminal Voltage Range[4]	$V_{A, B, W}$		V_{SS}		V_{DD}	V
Capacitance[5] A, B	$C_{A, B}$	f = 1 MHz, Measured to GND, Code = Half-Scale		50		pF
Capacitance[5] W	C_W	f = 1 MHz, Measured to GND, Code = Half-Scale		50		pF
Common-Mode Leakage Current[5, 6]	I_{CM}	V_W = V_{DD}/2		0.01	1	µA
DIGITAL INPUTS and OUTPUTS						
Input Logic High	V_{IH}	With Respect to GND, V_{DD} = 5 V	2.4			V
Input Logic Low	V_{IL}	With Respect to GND, V_{DD} = 5 V			0.8	V
Input Logic High	V_{IH}	With Respect to GND, V_{DD} = 3 V	2.1			V
Input Logic Low	V_{IL}	With Respect to GND, V_{DD} = 3 V			0.6	V
Input Logic High	V_{IH}	With Respect to GND, V_{DD} = +2.5 V, V_{SS} = –2.5 V	2.0			V
Input Logic Low	V_{IL}	With Respect to GND, V_{DD} = +2.5 V, V_{SS} = –2.5 V			0.5	V
Output Logic High (SDO, RDY)	V_{OH}	$R_{PULL-UP}$ = 2.2 kΩ to 5 V	4.9			V
Output Logic Low	V_{OL}	I_{OL} = 1.6 mA, V_{LOGIC} = 5 V			0.4	V
Input Current	I_{IL}	V_{IN} = 0 V or V_{DD}			±2.5	µA
Input Capacitance[5]	C_{IL}			4		pF
Output Current[5]	I_{O1}, I_{O2}	V_{DD} = 5 V, V_{SS} = 0 V, T_A = 25°C		50		mA
		V_{DD} = 2.5 V, V_{SS} = 0 V, T_A = 25°C		7		mA
POWER SUPPLIES						
Single-Supply Power Range	V_{DD}	V_{SS} = 0 V	2.7		5.5	V
Dual-Supply Power Range	V_{DD}/V_{SS}		±2.25		±2.75	V
Positive Supply Current	I_{DD}	V_{IH} = V_{DD} or V_{IL} = GND		2.7	10	µA
Programming Mode Current	$I_{DD(PG)}$	V_{IH} = V_{DD} or V_{IL} = GND		40		mA
Read Mode Current[7]	$I_{DD(XFR)}$	V_{IH} = V_{DD} or V_{IL} = GND	0.3	3	9	mA
Negative Supply Current	I_{SS}	V_{IH} = V_{DD} or V_{IL} = GND, V_{DD} = +2.5 V, V_{SS} = –2.5 V		0.5	10	µA
Power Dissipation[8]	P_{DISS}	V_{IH} = V_{DD} or V_{IL} = GND		0.018	0.05	mW
Power Supply Sensitivity[5] I_O I_{OL}	P_{SS}	ΔV_{DD} = 5 V ± 10%		0.002	0.01	%/%
DYNAMIC CHARACTERISTICS[5, 9]						
Bandwidth	BW	–3 dB, R = 10 kΩ/50 kΩ/100 kΩ		370/85/44		kHz
Total Harmonic Distortion	THD_W	V_A = 1 V_{RMS}, V_B = 0 V, f = 1 kHz, R_{AB} = 10 kΩ		0.022		%
Total Harmonic Distortion	THD_W	V_A = 1 V_{RMS}, V_B = 0 V, f = 1 kHz, R_{AB} = 50 kΩ, 100 kΩ		0.045		%

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
V_W Settling Time	t_S	$V_A = V_{DD}$, $V_B = 0$ V, V_W = 0.50% Error Band, Code 000_H to 200_H For R_{AB} = 10 kΩ/50 kΩ/100 kΩ		1.2/3.7/7		µs
Resistor Noise Voltage	e_{N_WB}	R_{WB} = 5 kΩ, f = 1 kHz		9		nV/√Hz

NOTES
[1]Typicals represent average readings at 25°C and V_{DD} = 5 V.
[2]Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. I_W ~ 50 µA @ V_{DD} = +2.7 V and I_W ~ 400 µA @ V_{DD} = +5 V for the R_{AB} = 10 kΩ version, I_W ~ 50 µA for the R_{AB} = 50 kΩ and I_W ~ 25 µA for the R_{AB} = 100 kΩ version. See test circuit Figure 12.
[3]INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter. $V_A = V_{DD}$ and $V_B = V_{SS}$. DNL specification limits of –1 LSB minimum are Guaranteed Monotonic operating conditions. See test circuit Figure 13.
[4]Resistor terminals A, B, and W have no limitations on polarity with respect to each other. Dual Supply Operation enables ground-referenced bipolar signal adjustment.
[5]Guaranteed by design and not subject to production test.
[6]Common-mode leakage current is a measure of the dc leakage from any terminal B and W to a common-mode bias level of $V_{DD}/2$.
[7]Transfer (XFR) Mode current is not continuous. Current consumed while EEMEM locations are read and transferred to the RDAC register. See TPC 19.
[8]P_{DISS} is calculated from $(I_{DD} \times V_{DD}) + (I_{SS} \times V_{SS})$.
[9]All dynamic characteristics use V_{DD} = +2.5 V and V_{SS} = –2.5 V.

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS 10 kΩ, 50 kΩ, 100 kΩ VERSIONS

(V_{DD} = 3 V to 5.5 V and –40°C < T_A < +85°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
INTERFACE TIMING CHARACTERISTICS[2, 3]						
Clock Cycle Time (t_{CYC})	t_1		20			ns
$\overline{CS}$ Setup Time	t_2		10			ns
CLK Shutdown Time to $\overline{CS}$ Rise	t_3		1			t_{CYC}
Input Clock Pulsewidth	t_4, t_5	Clock Level High or Low	10			ns
Data Setup Time	t_6	From Positive CLK Transition	5			ns
Data Hold Time	t_7	From Positive CLK Transition	5			ns
$\overline{CS}$ to SDO-SPI Line Acquire	t_8				40	ns
$\overline{CS}$ to SDO-SPI Line Release	t_9				50	ns
CLK to SDO Propagation Delay[4]	t_{10}	R_P = 2.2 kΩ, C_L < 20 pF			50	ns
CLK to SDO Data Hold Time	t_{11}	R_P = 2.2 kΩ, C_L < 20 pF	0			ns
$\overline{CS}$ High Pulsewidth[5]	t_{12}		10			ns
$\overline{CS}$ High to $\overline{CS}$ High[5]	t_{13}		4			t_{CYC}
$\overline{RDY}$ Rise to $\overline{CS}$ Fall	t_{14}		0			ns
$\overline{CS}$ Rise to $\overline{RDY}$ Fall Time	t_{15}			0.1	0.15	ms
Read/Store to Nonvolatile EEMEM[6]	t_{16}	Applies to Command 2_H, 3_H, 9_H			25	ms
$\overline{CS}$ Rise to Clock Rise/Fall Setup	t_{17}		10			ms
Preset Pulsewidth (Asynchronous)	t_{PRW}	Not Shown in Timing Diagram	50			ms
Preset Response Time to RDY High	t_{PRESP}	$\overline{PR}$ Pulsed Low to Refreshed Wiper Positions		70		µs
FLASH/EE MEMORY RELIABILITY						
Endurance[7]			100			K Cycles
Data Retention[8]				100		Years

NOTES
[1]Typicals represent average readings at 25°C and V_{DD} = 5 V.
[2]Guaranteed by design and not subject to production test.
[3]See timing diagram for location of measured values. All input control voltages are specified with $t_R = t_F$ = 2.5 ns (10% to 90% of 3 V) and timed from a voltage level of 1.5 V. Switching characteristics are measured using both V_{DD} = 3 V and 5 V.
[4]Propagation delay depends on value of V_{DD}, R_{PULL_UP}, and C_L. See applications text.
[5]Valid for commands that do not activate the RDY pin.
[6]RDY pin low only for commands 2, 3, 8, 9, 10, and the PR hardware pulse: CMD_8 ~ 1 µs; CMD_9,10 ~0.12 µs; CMD_2,3 ~20 µs. Device operation at T_A = –40°C and V_{DD} < +3 V extends the save time to 35 µs.
[7]Endurance is qualified to 100,000 cycles as per JEDEC Std. 22 method A117 and measured at –40°C, +25°C, and +85°C; typical endurance at 25°C is 700,000 cycles.
[8]Retention lifetime equivalent at junction temperature (T_J) = 55°C as per JEDEC Std. 22, Method A117. Retention lifetime based on an activation energy of 0.6 eV will derate with junction temperature as shown in Figure 20 in the Flash/EE Memory Description section of this data sheet. The AD5231 contains 9,646 transistors. Die size: 69 mil × 115 mil, 7,993 sq. mil.

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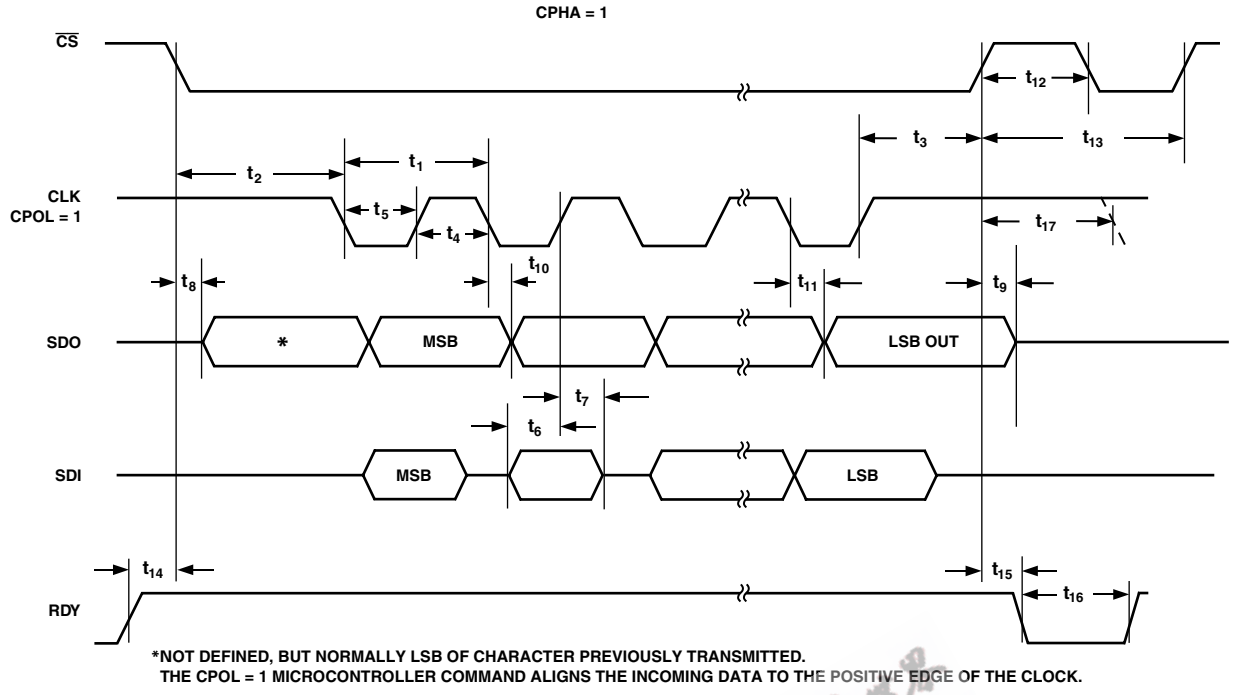


Figure 2a. CPHA = 1 Timing Diagram

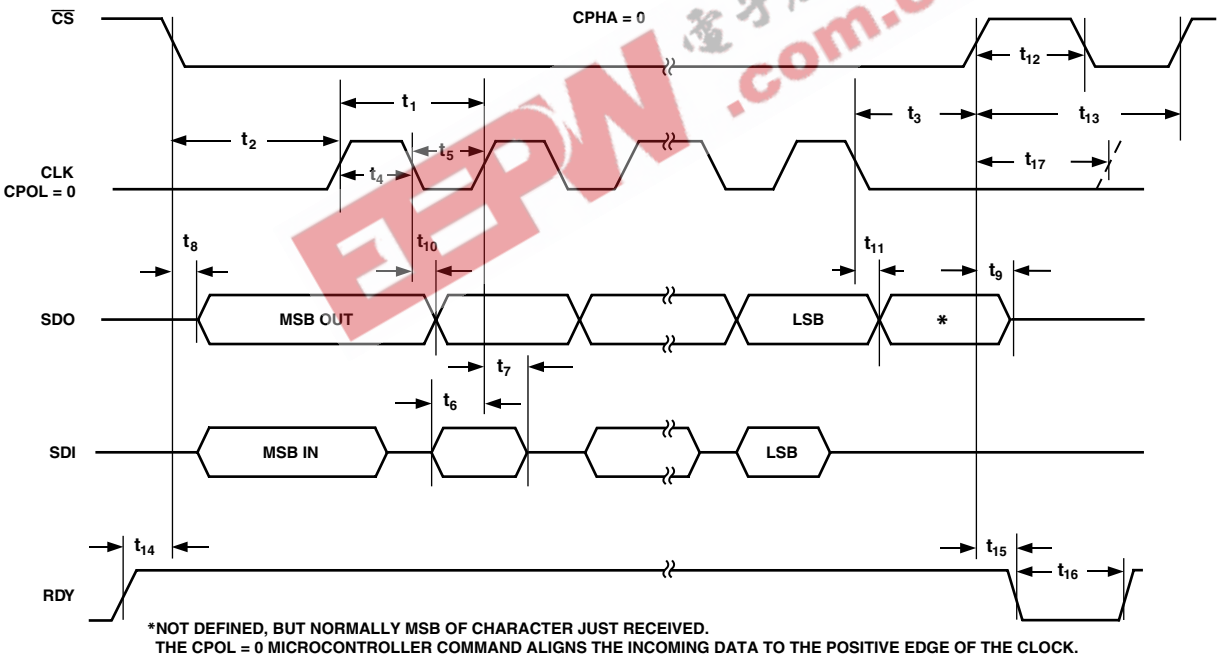


Figure 2b. CPHA = 0 Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = 25°C, unless otherwise noted)

V_{DD} to GND ..... –0.3 V, +7 V
V_{SS} to GND ..... +0.3 V, –7 V
V_{DD} to V_{SS} ..... 7 V
V_A, V_B, V_W to GND ..... V_{SS} – 0.3 V, V_{DD} + 0.3 V
A–B, A–W, B–W
  Intermittent[2] ..... ±20 mA
  Continuous ..... ±2 mA
Digital Inputs and Output Voltage to GND
  ..... –0.3 V, V_{DD} + 0.3 V
Operating Temperature Range[3] ..... –40°C to +85°C
Maximum Junction Temperature (T_J Max) ..... 150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature, Soldering
  Vapor Phase (60 sec) ..... 215°C
  Infrared (15 sec) ..... 220°C

Thermal Resistance Junction-to-Ambient θ_{JA},
  TSSOP-16 ..... 150°C/W
Thermal Resistance Junction-to-Case θ_{JC},
  TSSOP-16 ..... 28°C/W
Package Power Dissipation = (T_J Max – T_A)/θ_{JA}

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.

[3]Includes programming of nonvolatile memory

ORDERING GUIDE

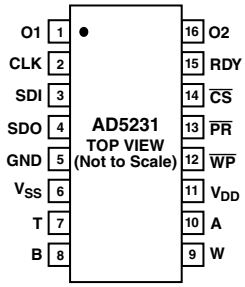
Model	R_{AB} (kΩ)	Temperature Range (°C)	Package Description	Package Option	Ordering Quantity	Top Mark*
AD5231BRU10	10	–40 to +85	TSSOP-16	RU-16	96	5231B10
AD5231BRU10-REEL7	10	–40 to +85	TSSOP-16	RU-16	1,000	5231B10
AD5231BRU50	50	–40 to +85	TSSOP-16	RU-16	96	5231B50
AD5231BRU50-REEL7	50	–40 to +85	TSSOP-16	RU-16	1,000	5231B50
AD5231BRU100	100	–40 to +85	TSSOP-16	RU-16	96	5231BC
AD5231BRU100-REEL7	100	–40 to +85	TSSOP-16	RU-16	1,000	5231BC

*Line 1 contains ADI logo symbol and the date code YYWW; line 2 contains detail model number listed in this column.

CAUTION

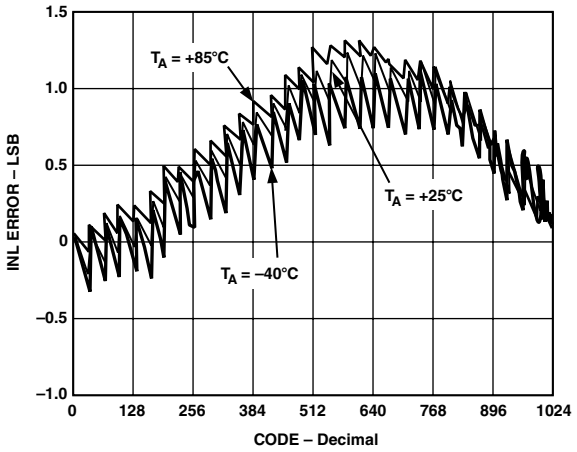
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5231 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION

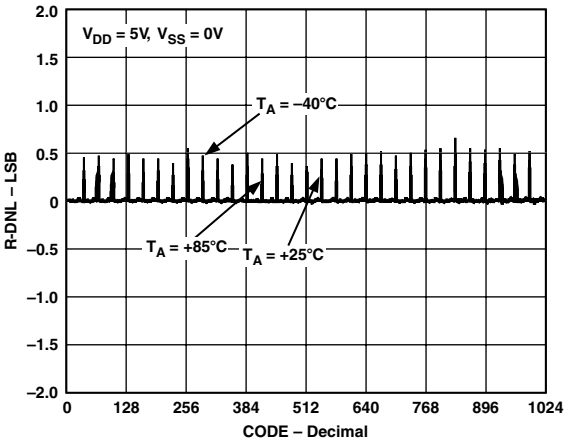


PIN FUNCTION DESCRIPTIONS

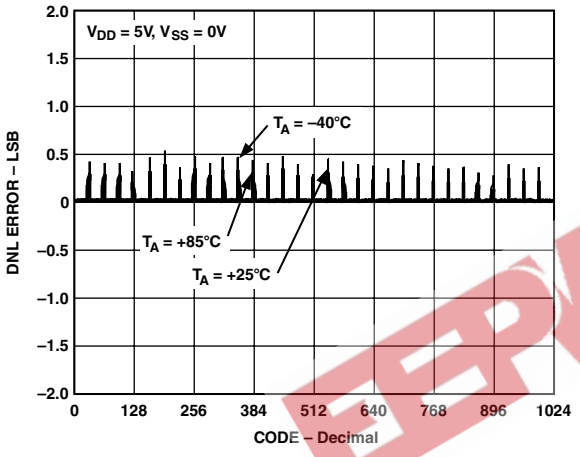
Pin No.	Mnemonic	Description
1	O1	Nonvolatile Digital Output #1. ADDR(O1) = 1_H, data bit position D0
2	CLK	Serial Input Register Clock Pin. Shifts in one bit at a time on positive clock edges.
3	SDI	Serial Data Input Pin. Shifts in one bit at a time on positive clock CLK edges. MSB loaded first.
4	SDO	Serial Data Output Pin. Open Drain Output requires external pull-up resistor. Commands 9 and 10 activate the SDO output. (See Instruction operation Truth Table, Table III.) Other commands shift out the previously loaded SDI bit pattern delayed by 24 clock pulses. This allows daisy-chain operation of multiple packages.
5	GND	Ground Pin, Logic Ground Reference
6	V_{SS}	Negative Supply. Connect to zero volts for single supply applications.
7	T	Used as digital input during factory test mode. Connect to V_{DD} or V_{SS}.
8	B	B Terminal of RDAC
9	W	Wiper Terminal of RDAC. ADDR(RDAC1) = 0_H.
10	A	A Terminal of RDAC1
11	V_{DD}	Positive Power Supply Pin
12	$\overline{WP}$	Write Protect Pin. When active low, $\overline{WP}$ prevents any changes to the present contents except $\overline{PR}$ and cmd 1 and 8 will refresh the RDAC register from EEMEM. Execute on NOP instruction before returning to $\overline{WP}$ high.
13	$\overline{PR}$	Hardware Override Preset Pin. Refreshes the scratch pad register with current contents of the EEMEM register. Factory default loads midscale 512_{10} until EEMEM loaded with a new value by the user ($\overline{PR}$ is activated at the logic high transition).
14	$\overline{CS}$	Serial Register Chip Select Active Low. Serial register operation takes place when $\overline{CS}$ returns to logic high.
15	RDY	Ready. Active-high open drain output. Identifies completion of commands 2, 3, 8, 9, 10, and $\overline{PR}$.
16	O2	Nonvolatile Digital Output #2. ADDR(O2) = 1_H, data bit position D1.



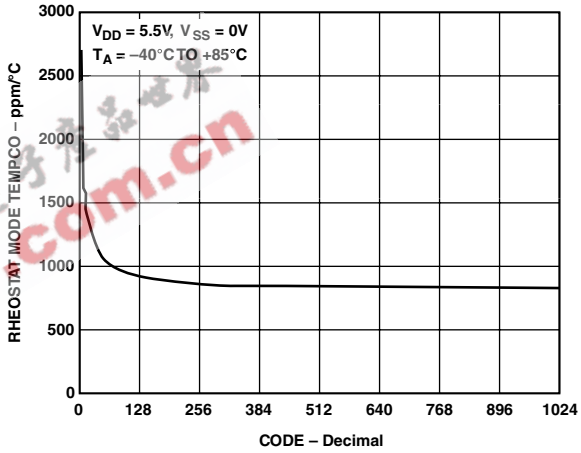
TPC 1. INL vs. Code, T_A = –40°C, +25°C, +85°C Overlay, R_{AB} = 10 kΩ



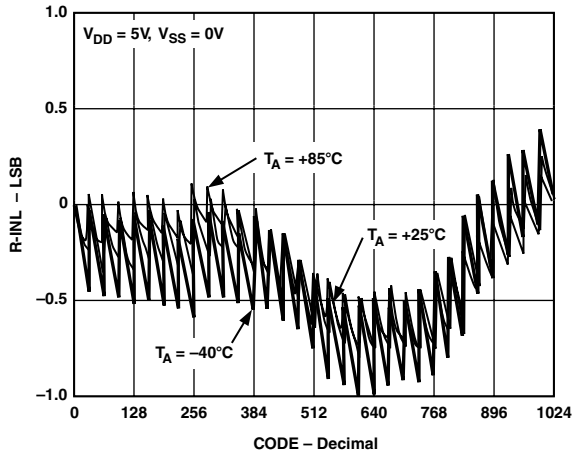
TPC 4. R-DNL vs. Code, T_A = –40°C, +25°C, +85°C Overlay, R_{AB} = 10 kΩ



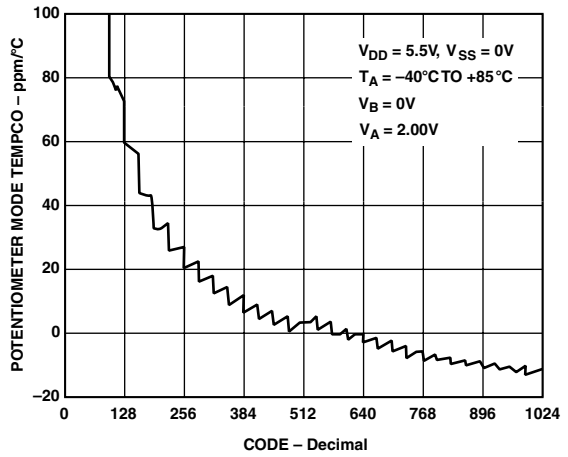
TPC 2. DNL vs. Code, T_A = –40°C, +25°C, +85°C Overlay, R_{AB} = 10 kΩ



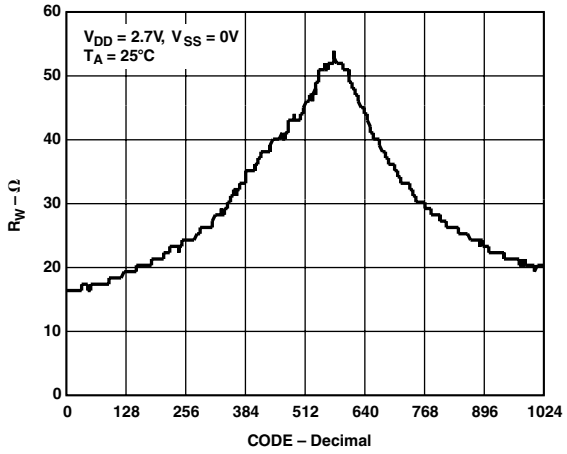
TPC 5. $\Delta R_{WB}/\Delta T$ vs. Code, R_{AB} = 10 kΩ



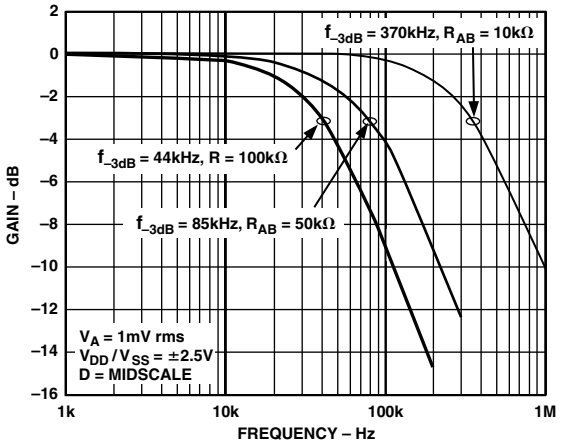
TPC 3. R-INL vs. Code, T_A = –40°C, +25°C, +85°C Overlay, R_{AB} = 10 kΩ



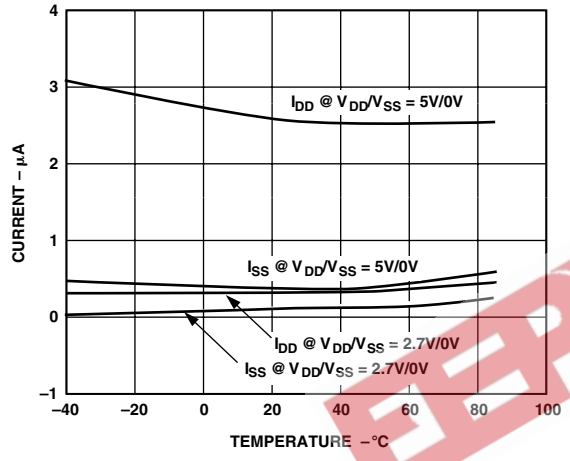
TPC 6. $\Delta R_{WB}/\Delta T$ vs. Code, R_{AB} = 10 kΩ



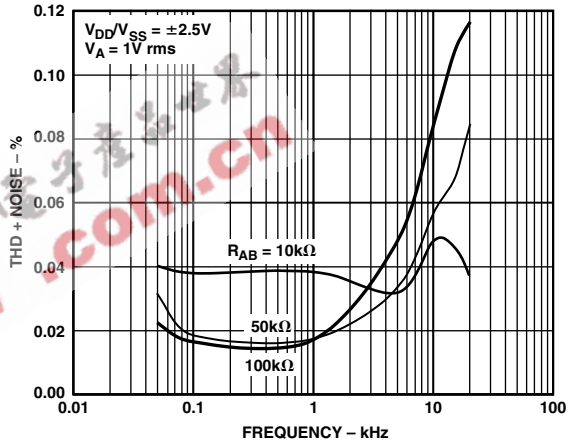
TPC 7. Wiper-On Resistance vs. Code



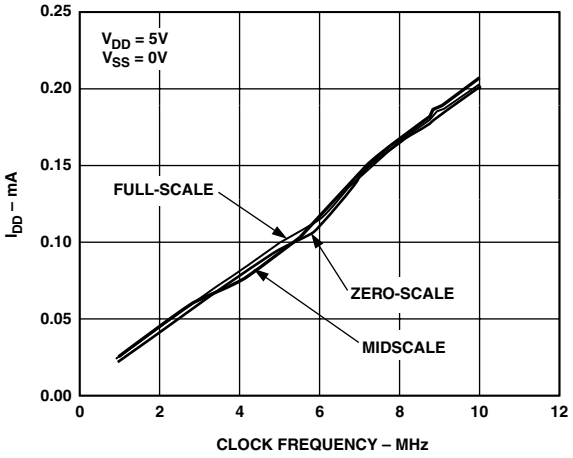
TPC 10. –3 Bandwidth vs. Resistance. Test Circuit in Figure 16.



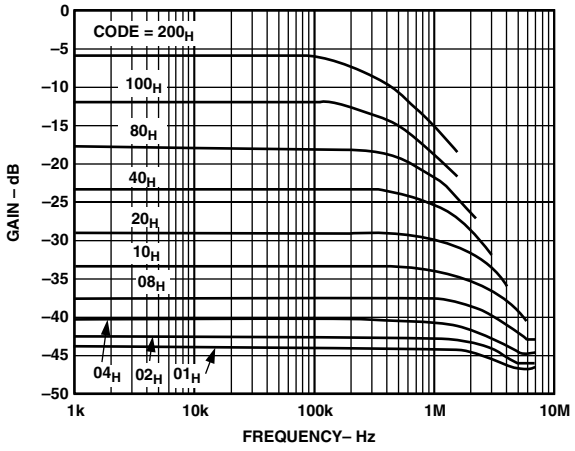
TPC 8. I_{DD} vs. Temperature, R_{AB} = 10 kΩ



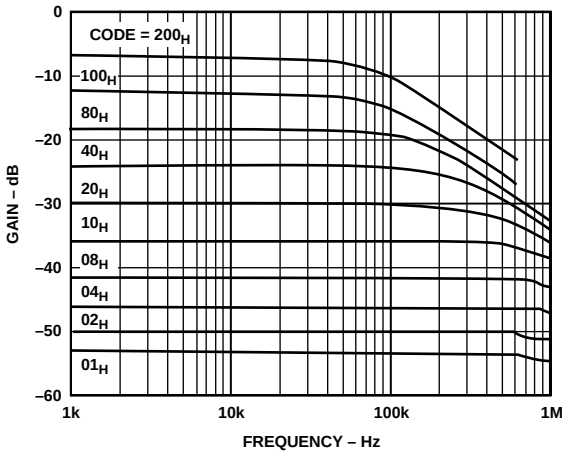
TPC 11. Total Harmonic Distortion vs. Frequency



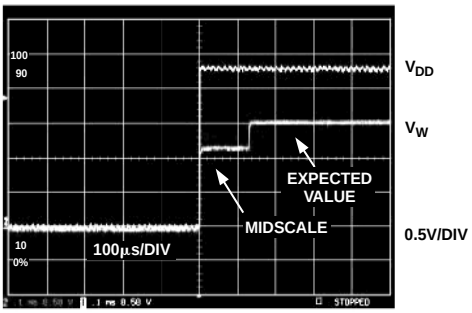
TPC 9. I_{DD} vs. Clock Frequency, R_{AB} = 10 kΩ



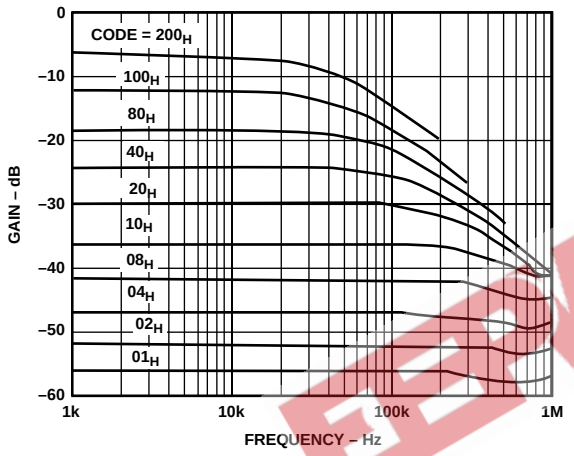
TPC 12. Gain vs. Frequency vs. Code, R_{AB} = 10 kΩ. Test Circuit in Figure 18



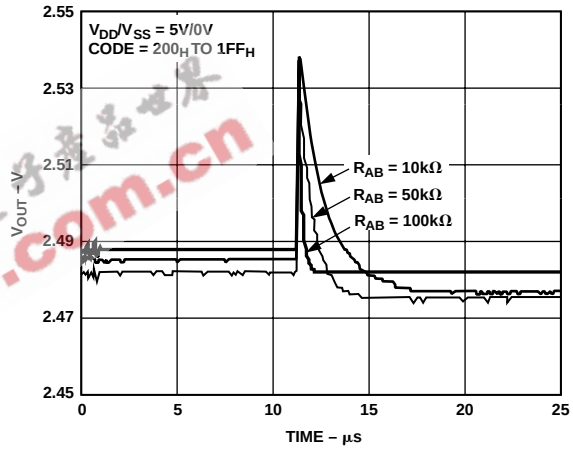
TPC 13. Gain vs. Frequency vs. Code, R_{AB} = 50 kΩ. Test Circuit in Figure 18



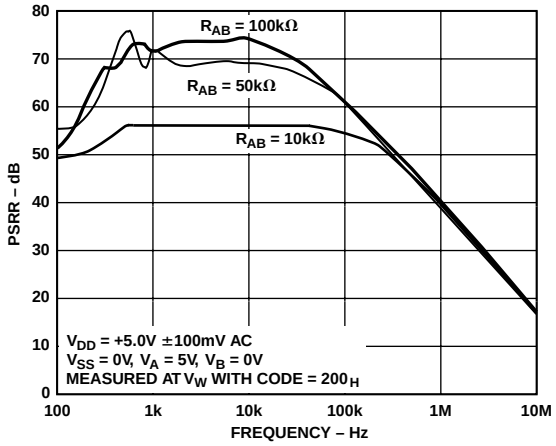
TPC 16. Power-On Reset, V_{DD} = 2.25 V, Code = 1010101010_B



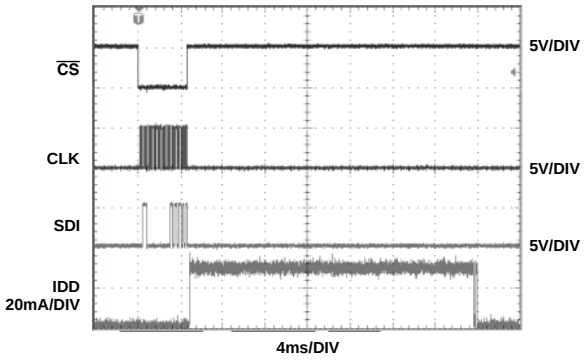
TPC 14. Gain vs. Frequency vs. Code, R_{AB} = 100 kΩ. Test Circuit in Figure 18



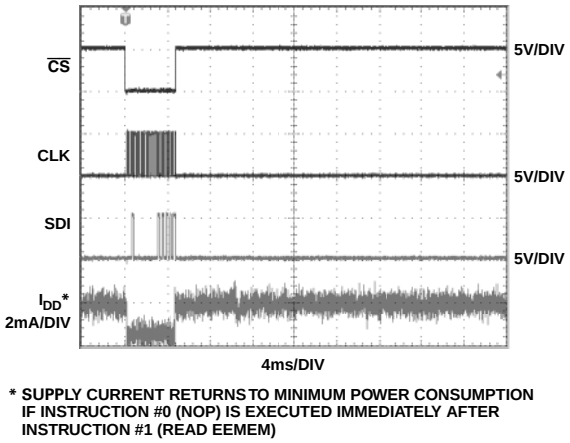
TPC 17. Midscale Glitch Energy, Code 200_H to $1FF_H$



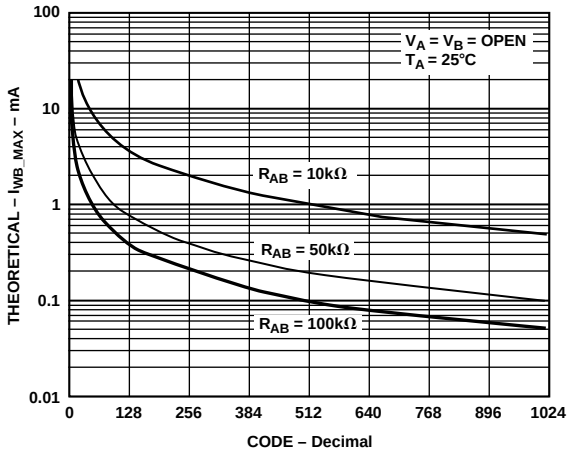
TPC 15. PSRR vs. Frequency



TPC 18. I_{DD} vs. Time (Save) Program Mode



TPC 19. I_{DD} vs. Time (Read) Program Mode



TPC 20. I_{WB_MAX} vs. Code

OPERATIONAL OVERVIEW

The AD5231 digital potentiometer is designed to operate as a true variable resistor replacement device for analog signals that remain within the terminal voltage range of $V_{SS} < V_{TERM} < V_{DD}$. The basic voltage range is limited to a $|V_{DD} - V_{SS}| < 5.5$ V. The digital potentiometer wiper position is determined by the RDAC register contents. The RDAC register acts as a scratch pad register allowing as many value changes as necessary to place the potentiometer wiper in the correct position. The scratch pad register can be programmed with any position value using the standard SPI serial interface mode by loading the complete representative data word. Once a desirable position is found this value can be saved into an EEMEM register. Thereafter the wiper position will always be set at that position for any future ON-OFF-ON power supply sequence. The EEMEM save process takes approximately 25 ms, during this time the shift register is locked preventing any changes from taking place. The RDY pin indicates the completion of this EEMEM save.

There are 16 instructions that facilitate users' programming needs. Refer to Table III. The instructions are:

1. Do Nothing
2. Restore EEMEM Setting to RDAC
3. Save RDAC Setting to EEMEM
4. Save RDAC Setting or User Data to EEMEM
5. Decrement 6 dB
6. Decrement 6 dB
7. Decrement One Step
8. Decrement One Step
9. Reset EEMEM setting to RDAC
10. Read EEMEM to SDO
11. Read Wiper Setting to SDO
12. Write Data to RDAC
13. Increment 6 dB
14. Increment 6 dB
15. Increment One Step
16. Increment One Step

Scratch Pad and EEMEM Programming

The scratch pad register (RDAC register) directly controls the position of the digital potentiometer wiper. When the scratch pad register is loaded with all zeros, the wiper will be connected to the B-Terminal of the variable resistor. When the scratch pad register is loaded with midscale code (1/2 of full-scale position), the wiper will be connected to the middle of the variable resistor. And when the scratch pad is loaded with full-scale code, all ones, the wiper will connect to the A-Terminal. Since the scratch pad register is a standard logic register, there is no restriction on the number of changes allowed. The EEMEM registers have a program erase/write cycle limitation described in the Flash/EEMEM Reliability section.

Basic Operation

The basic mode of setting the variable resistor wiper position (programming the scratch pad register) is accomplished by loading the serial data input register with the command instruction #11, which includes the desired wiper position data. When the desired wiper position is found, the user would load the serial data input register with the command instruction #2, which makes a copy of the desired wiper position data into the nonvolatile EEMEM register. After 25 ms the wiper position will be permanently stored in the nonvolatile EEMEM location. Table I provides an application-programming example listing the sequence of serial data input (SDI) words and the serial data output appearing at the SDO Pin in hexadecimal format.

Table I. Set and Save RDAC Data to EEMEM Register

SDI	SDO	Action
$B00100_H$	$XXXXXX_H$	Loads data 100_H into RDAC register, Wiper W moves to 1/4 full-scale position.
$20XXXX_H$	$B00100_H$	Saves copy of RDAC register contents into EEMEM register.

At system power ON, the scratch pad register is automatically refreshed with the value last saved in the EEMEM register. The factory preset EEMEM value is midscale but thereafter, the EEMEM value can be changed by user.

During operation, the scratch pad (wiper) register can also be refreshed with the current content of the nonvolatile EEMEM register under hardware control by pulsing the $\overline{PR}$ Pin without activating instruction 1 or 8. Beware that the $\overline{PR}$ pulse first sets the wiper at midscale when brought to logic zero, and then on the positive transition to logic high, it reloads the RDAC wiper register with the contents of EEMEM. Many additional advanced programming commands are available to simplify the variable resistor adjustment process, See Table III. For example, the wiper position can be changed one step at a time by using the Increment/Decrement instruction or by 6 dB at a time with the Shift Left/Right instruction command. Once an Increment, Decrement, or Shift command has been loaded into the shift register, subsequent $\overline{CS}$ strobes will repeat this command. This is useful for push button control applications. See the advanced control modes section following the Instruction Operation Truth Table. A serial data output SDO Pin is available for daisy-chaining and for readout of the internal register contents. The serial input data register uses a 24-bit [instruction/address/data] WORD format.

EEMEM Protection

Write protect ($\overline{WP}$) disables any changes of the scratch pad register contents regardless of the software commands, except that the EEMEM setting can be refreshed and overwritten $\overline{WP}$ by using commands 1, 8, and $\overline{PR}$ pulse. Therefore, the write-protect ($\overline{WP}$) Pin provides a hardware EEMEM protection feature. To disable $\overline{WP}$, it is recommended to execute a NOP command before returning $\overline{WP}$ to logic high.

Digital Input/Output Configuration

All digital inputs are ESD-protected high-input impedance that can be driven directly from most digital sources. Active at logic low, $\overline{PR}$ and $\overline{WP}$ must be biased to V_{DD} if they are not used. No internal pull-up resistors are present on any digital input pins. The SDO and RDY Pins are open-drain digital outputs where pull-up resistors are needed only if using these functions. A resistor value in the range of 1 kΩ to 10 kΩ is a proper choice which balances the power and switching speed trade off.

The equivalent serial data input and output logic is shown in Figure 3. The open drain output SDO is disabled whenever chip select $\overline{CS}$ is logic high. ESD protection of the digital inputs is shown in Figures 4a and 4b.

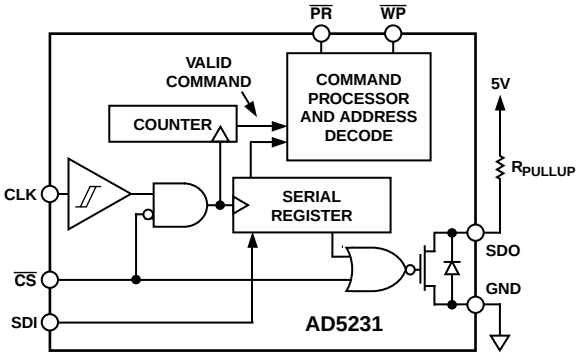


Figure 3. Equivalent Digital Input-Output Logic

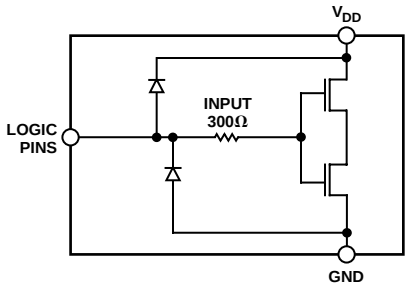


Figure 4a. Equivalent ESD Digital Input Protection

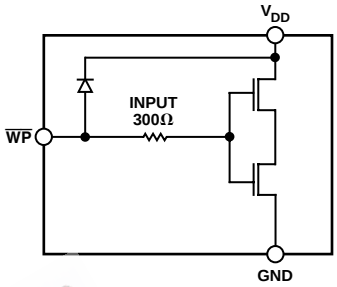


Figure 4b. Equivalent $\overline{WP}$ Input Protection

Serial Data Interface

The AD5231 contains a four-wire SPI compatible digital interface (SDI, SDO, $\overline{CS}$, and CLK). The AD5231 uses a 24-bit serial data word loaded MSB first. The format of the SPI compatible word is shown in Table II. The chip select $\overline{CS}$ Pin needs to be held low until the complete data word is loaded into the SDI Pin. When $\overline{CS}$ returns high the serial data word is decoded according to the instructions in Table III. The Command Bits (Cx) control the operation of the digital potentiometer. The Address Bits (Ax) determine which register is activated. The Data Bits (Dx) are the values that are loaded into the decoded register. Table V provides an address map of the EEMEM locations. The last instruction executed prior to a period of no programming activity should be the No Operation (NOP) instruction. This will place the internal logic circuitry in a minimum power dissipation state.

The SPI interface can be used in two slave modes CPHA = 1, CPOL = 1 and CPHA = 0, CPOL = 0. CPHA and CPOL refer to the control bits, that dictate SPI timing in these MicroConverters® and microprocessors: ADuC812/ADuC824, M68HC11, and MC68HC16R1/916R1.

Daisy-Chain Operation

The Serial Data Output Pin (SDO) serves two purposes. It can be used to readout the contents of the wiper setting and EEMEM values using instructions 10 and 9, respectively. The remaining instructions (#0–#8, #11–#15) are valid for daisy-chaining multiple devices in simultaneous operations. Daisy-chaining minimizes the number of port pins required from the controlling IC (see Figure 5). The SDO Pin contains an open drain N-Ch FET that requires a pull-up resistor, if this function is used. As shown in Figure 5, users need to tie the SDO Pin of one package to the

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SDI Pin of the next package. Users may need to increase the clock period because the pull-up resistor and the capacitive loading at the SDO-SDI interface may require additional time delay between subsequent packages. When two AD5231s are daisy-chained, 48 bits of data are required. The first 24 bits go to U2 and the second 24 bits go to U1. The 24 bits are formatted to contain the 4-bit instruction, followed by the 4-bit address, 6-bit don't care, then the 10 bits of data. (The don't care can be used to store user information. See section Using Additional Internal Nonvolatile EEMEM). The $\overline{CS}$ should be kept low until all 48 bits are clocked into their respective serial registers. The $\overline{CS}$ is then pulled high to complete the operation.

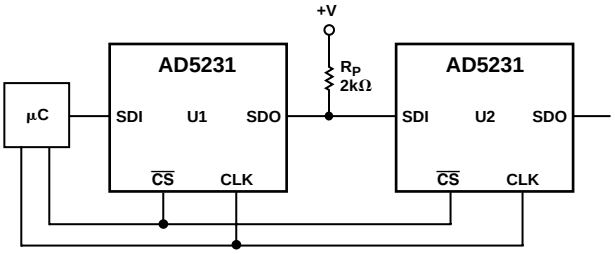


Figure 5. Daisy Chain Configuration using SDO

Terminal Voltage Operation Range

The AD5231 positive V_{DD} and negative V_{SS} power supply defines the boundary conditions for proper 3 terminal digital potentiometer operation. Supply signals present on terminals A, B, and W that exceed V_{DD} or V_{SS} will be clamped by the internal forward biased diodes (see Figure 6).

The ground pin of the AD5231 device is primarily used as a digital ground reference, which needs to be tied to the PCB's common ground. The digital input control signals to the AD5231 must be referenced to the device ground pin (GND), and satisfy the logic level defined in the specification table of this data sheet. An internal level-shift circuit ensures that the common-mode voltage range of the three terminals extends from V_{SS} to V_{DD}, regardless of the digital input level.

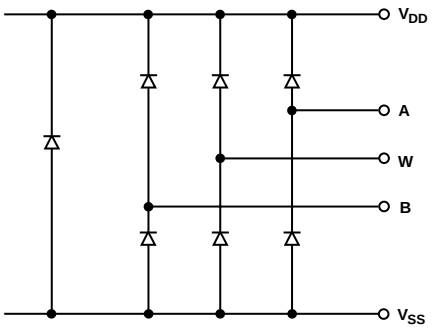


Figure 6. Maximum Terminal Voltages Set by V_{DD} and V_{SS}

Power-Up Sequence

Since there are diodes to limit the voltage compliance at terminals A, B, and W (see Figure 6), it is important to power V_{DD}/V_{SS} first before applying any voltage to terminals A, B, and W. Otherwise, the diode will be forward-biased such that V_{DD}/V_{SS} will be powered unintentionally and may affect the rest of the user's circuit. The ideal power-up sequence is in the following order: GND, V_{DD}, V_{SS}, Digital Inputs, and V A/B/W. The order of powering V_A, V_B, V_W, and digital inputs are not important as long as they are powered after V_{DD}/V_{SS}.

Regardless of the power-up sequence and the ramp rates of the power supplies, once V_{DD}/V_{SS} are powered, the power-on reset remains effective, which retrieves EEMEM saved value to RDAC register.

Latched Digital Outputs

A pair of digital outputs, O1 and O2, is available on the AD5231 that provide a nonvolatile logic 0 or logic 1 setting. O1 and O2 are standard CMOS logic outputs (shown in Figure 7). These outputs are ideal to replace functions often provided by DIP switches. In addition, they can be used to drive other standard CMOS logic controlled parts that need an occasional setting change.

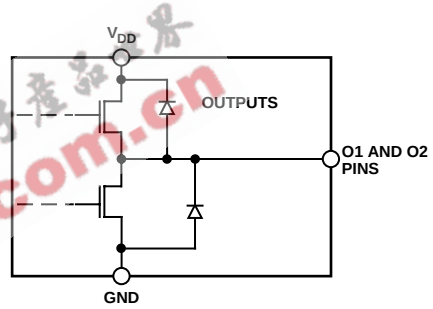


Figure 7. Logic Outputs O1 and O2

Table II. AD5231 24-Bit Serial Data Word

MSB Instruction Byte 0									Data Byte 1								Data Byte 0							LSB
RDAC	C3	C2	C1	C0	0	0	0	A0	X	X	X	X	X	X	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
EEMEM	C3	C2	C1	C0	A3	A2	A1	A0	D 15	D 14	D 13	D 12	D 11	D 10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Command bits are C0 to C3. Address bits are A3 to A0. Data bits D0 to D9 are applicable to RDAC; D0 to D15 are applicable to EEMEM. Command instruction codes are defined in Table III.

Table III. Instruction/Operation Truth Table[1, 2, 3]

Instruction Number	Instruction Byte 0 B23 ••••••••••••••••••••• B16 C3 C2 C1 C0 A3 A2 A1 A0	Data Byte 1 B15 ••••• B8 X ••• D9 D8	Data Byte 0 B7 ••• B0 D7 ••• D0	Operation
0	0 0 0 0 X X X X	X ••• X X	X ••• X	NOP: Do nothing. See Table XI
1	0 0 0 1 0 0 0 A0	X ••• X X	X ••• X	Write content of EEMEM to RDAC Register. This command leaves device in the Read Program power state. To return part to the idle state, perform NOP instruction #0. See Table XI
2	0 0 1 0 0 0 0 A0	X ••• X X	X ••• X	SAVE WIPER SETTING: Write contents of RDAC to EEMEM. See Table X
3[4]	0 0 1 1 A3 A2 A1 A0	D15 ••• D8	D7 ••• D0	Write contents of Serial Register Data Bytes 0 and 1 (total 16-bit) to EEMEM(ADDR). See Table XIII
4[5]	0 1 0 0 0 0 0 A0	X ••• X X	X ••• X	Decrement 6 dB: Right Shift contents of RDAC, stops at all "Zeros."
5[5]	0 1 0 1 X X X X	X ••• X X	X ••• X	Same as instruction 4
6[5]	0 1 1 0 0 0 0 A0	X ••• X X	X ••• X	Decrement content of RDAC Register by "One," stops at all "Zeros."
7[5]	0 1 1 1 X X X X	X ••• X X	X ••• X	Same as instruction 6
8	1 0 0 0 X X X X	X ••• X X	X ••• X	RESET: Load RDAC with its corresponding EEMEM previously saved value.
9	1 0 0 1 A3 A2 A1 A0	X ••• X X	X ••• X	Write content of EEMEM(ADDR) to Serial Register Data Bytes 0 and 1. SDO activated. See Table XIV
10	1 0 1 0 0 0 0 A0	X ••• X X	X ••• X	Write content of RDAC to Serial Register Data Bytes 0 and 1. SDO activated. See Table XV
11	1 0 1 1 0 0 0 A0	X ••• D9, D8	D7 ••• D0	Write content of Serial Register Data Bytes 0 and 1 (total 10-bit) to RDAC Register. See Table IX
12[5]	1 1 0 0 0 0 0 A0	X ••• X X	X ••• X	Increment 6 dB: Left Shift content of RDAC, stops at all "Ones." See Table XII
13[5]	1 1 0 1 X X X X	X ••• X X	X ••• X	Same as instruction 12
14[5]	1 1 1 0 0 0 0 A0	X ••• X X	X ••• X	Increment content of RDAC Register by "One," stops at all "Ones." See Table X.
15[5]	1 1 1 1 X X X X	X ••• X X	X ••• X	Same as instruction 14

NOTES

[1]The SDO output shifts out the last 24 bits of data clocked into the serial register for daisy-chain operation. Exception, any instruction following instruction #9 or #10, the selected internal register data will be present in Data Bytes 0 and 1. The instruction following #9 and #10 must also be a full 24-bit data word to completely clock out the contents of the serial register.

[2]The RDAC register is a volatile scratch pad register that is refreshed at power ON from the corresponding nonvolatile EEMEM register.

[3]Execution of the above operations takes place when the $\overline{CS}$ strobe returns to logic high.

[4]Instruction #3 write two data bytes (16-Bit data) to EEMEM. In the case of 0 addresses, only the last 10 bits are valid for wiper position setting.

[5]The increment, decrement, and shift commands ignore the contents of the shift register Data Bytes 0 and 1.

ADVANCED CONTROL MODES

The AD5231 digital potentiometer contains a set of user programming features to address the wide applications available to these universal adjustment devices. Key programming features include:

- Scratch Pad Programming to any desirable values
- Nonvolatile memory storage of the present scratch pad RDAC register value into the EEMEM register
- Increment and Decrement instructions for RDAC wiper register
- Left and right Bit Shift of RDAC wiper register to achieve 6 dB level changes
- 28 extra bytes of user-addressable nonvolatile memory

Linear Increment and Decrement Commands

The increment and decrement commands (#14, #15, #6, #7) are useful for linear step adjustment applications. These commands simplify microcontroller software coding by allowing the controller to just send an increment or decrement command to the device. For increment command, executing instruction #14 with proper address will automatically move the wiper to the next resistance segment position. Instruction #15 performs the same function except address does not need to be specified.

Logarithmic Taper Mode Adjustment (±6 dB/step)

Four programming instructions produce logarithmic taper increment and decrement wiper. These settings are activated by the 6 dB increment and 6 dB decrement instructions #12, #13, #4, and #5, respectively. For example, starting at zero scale, executing 11 times the increment instruction #12 will move the wiper in +6 dB per step from the 0% to full scale R_{AB}. The +6 dB increment instruction doubles the value of the RDAC register content each time the command is executed. When the wiper position is near the maximum setting, the last +6 dB increment instruction will cause the wiper to go to the full-scale 1023 code position. Further +6 dB per increment instruction will no longer change the wiper position beyond its full scale.

6 dB step increment and decrement are achieved by shifting the bit internally to the left and right, respectively. The following information explains the nonideal ±6 dB step adjustment at certain conditions. Table IV illustrates the operation of the shifting function on the RDAC register data bits. Each line going down the table represents a successive shift operation. Note that the left shift #12 and #13 commands were modified such that if the data in the RDAC register is equal to zero, and the data is left shifted, the RDAC register is then set to code 1. Similarly, if the data in the RDAC register is greater than or equal to midscale, and the data is left shifted, then the data in the RDAC register is automatically set to full-scale. This makes the left shift function as ideal a logarithmic adjustment as possible.

The right shift #4 and #5 commands will be ideal only if the LSB is zero (i.e., ideal logarithmic—no error). If the LSB is a 1, the right shift function generates a linear half LSB error, which translates to a numbers of bits dependent logarithmic error as shown in Figure 8. The plot shows the error of the odd numbers of bits for AD5231.

Table IV. Detail Left and Right Shift Functions for 6 dB Step Increment and Decrement

Left Shift (+6 dB/step) ↓ Right Shift (–6 dB/step) ↓

Left Shift	Right Shift
00 0000 0000	11 1111 1111
00 0000 0001	01 1111 1111
00 0000 0010	00 1111 1111
00 0000 0100	00 0111 1111
00 0000 1000	00 0011 1111
00 0001 0000	00 0001 1111
00 0010 0000	00 0000 1111
00 0100 0000	00 0000 0111
00 1000 0000	00 0000 0011
01 0000 0000	00 0000 0001
10 0000 0000	00 0000 0000
11 1111 1111	00 0000 0000
11 1111 1111	00 0000 0000

Actual conformance to a logarithmic curve between the data contents in the RDAC register and the wiper position for each Right Shift #4 and #5 command execution contains an error only for odd numbers of bits. Even numbers of bits are ideal. The graph in Figure 8 shows plots of Log_Error [i.e., $20 \times \log_{10}$ (error/code)] AD5231. For example, code 3 Log_Error = $20 \times \log_{10}$ (0.5/3) = –15.56 dB, which is the worst case. The plot of Log_Error is more significant at the lower codes.

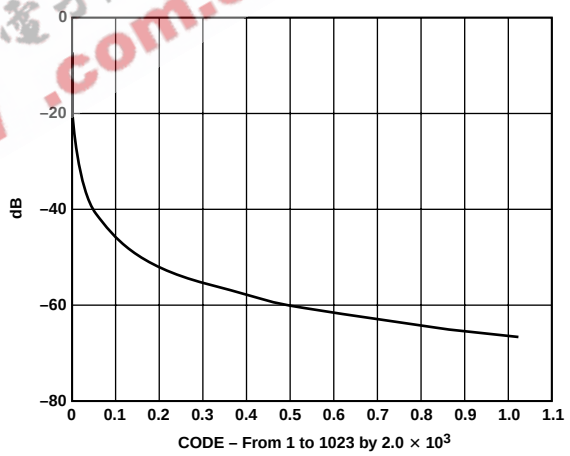


Figure 8. Plot of Log_Error Conformance for Odd Numbers of Bits Only (Even Numbers of Bits are Ideal)

Using Additional Internal Nonvolatile EEMEM

The AD5231 contains additional internal user storage registers (EEMEM) for saving constants and other 16-bit data. Table V provides an address map of the internal storage registers shown in the functional block diagram as EEMEM1, EEMEM2, and 28 bytes (14 addresses × 2 bytes each) of User EEMEM.

Table V. EEMEM Address Map

Address	EEMEM For
0000	RDAC[1, 2]
0001	O1 and O2[3]
0010	USER1[4]
0011	USER2
:	:
1110	USER13
1111	USER14

NOTES
[1]RDAC data stored in EEMEM location is transferred to the RDAC Register at Power ON, or when instructions #1, #8, and $\overline{PR}$ are executed.
[2]Execution of instruction #1 leaves the device in the Read Mode power consumption state. After the last instruction #1 is executed, the user should perform a NOP, instruction #0 to return the device to the low power idling state.
[3]O1 and O2 data stored in EEMEM locations are transferred to their corresponding Digital Register at Power ON, or when instructions #1 and #8 are executed.
[4]USER <data> are internal nonvolatile EEMEM registers available to store and retrieve constants and other 16-bit information using #3 and #9, respectively.

RDAC STRUCTURE

The patent pending RDAC contains multiple strings of equal resistor segments, with an array of analog switches, that act as the wiper connection. The number of positions is the resolution of the device. The AD5231 has 1024 connection points allowing it to provide better than 0.1% set-ability resolution. Figure 9 shows an equivalent structure of the connections between the three terminals of the RDAC. The SW_A and SW_B will always be ON, while one of the switches SW(0) to SW(2^N–1) will be ON one at a time depending on the resistance position decoded from the data bits. Since the switch is not ideal, there is a 15 Ω wiper resistance, R_W. Wiper resistance is a function of supply voltage and temperature. The lower the supply voltage, or the higher the temperature, the higher the resulting wiper resistance. Users should be aware of the wiper resistance dynamics if accurate prediction of the output resistance is needed.

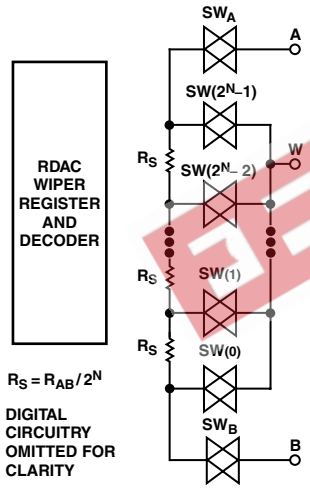


Figure 9. Equivalent RDAC Structure (Patent Pending)

Table VI. Nominal Individual Segment Resistor (R_S)

Device Resolution	10 kΩ Version	50 kΩ Version	100 kΩ Version
10-Bit	9.8 Ω	48.8 Ω	97.6 Ω

PROGRAMMING THE VARIABLE RESISTOR

Rheostat Operation

The nominal resistance of the RDAC between terminals A-and-B, R_{AB} is available with 10 kΩ, 50 kΩ, and 100 kΩ with 1024 positions (10-bit resolution). The final digit(s) of the part number determine the nominal resistance value, e.g., 10 kΩ = 10; 50 kΩ = 50; 100 kΩ = C.

The 10-bit data word in the RDAC latch is decoded to select one of the 1024 possible settings. The following discussion describes the calculation of resistance R_{WB} at different codes of a 10 kΩ part. For V_{DD} = 5 V, the wiper first connection starts at the B terminal for data 000_H. $R_{WB}(0)$ is 15 Ω because of the wiper resistance and it is independent of the nominal resistance. The second connection is the first tap point where $R_{WB}(1)$ becomes 9.7 Ω + 15 Ω = 27.4 Ω for data 001_H. The third connection is the next tap point representing $R_{WB}(2)$ = 19.4 + 15 = 34.4 Ω for data 002_H and so on. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at $R_{WB}(1023)$ = 10005 Ω. See Figure 9 for a simplified diagram of the equivalent RDAC circuit. When R_{WB} is used, the A–terminal can be left floating or tied to the wiper.

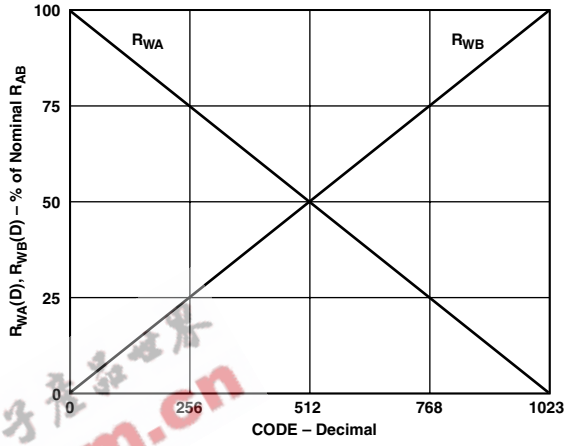


Figure 10. $R_{WA}(D)$ and $R_{WB}(D)$ vs. Decimal Code

The general equation, which determines the programmed output resistance between W and B, is:

$$R_{WB}(D) = \frac{D}{1024} \times R_{AB} + R_W \quad (1)$$

Where D is the decimal equivalent of the data contained in the RDAC register, R_{AB} is the Nominal Resistance between terminals A-and-B, and R_W is the wiper resistance.

For example, the following output resistance values will be set for the following RDAC latch codes with V_{DD} = 5 V (applies to R_{AB} = 10 kΩ Digital Potentiometers):

Table VII. R_{WB} at Selected Codes for R_{AB} = 10 kΩ

D(DEC)	$R_{WB}(D)$ (Ω)	Output State
1023	10,005	Full-Scale
512	50015	MidScale
1	24.7	1 LSB
0	15	Zero-Scale (Wiper Contact Resistor)

Note that in the zero-scale condition a finite wiper resistance of 15 Ω is present. Care should be taken to limit the current flow between W and B in this state to no more than 20 mA to avoid degradation or possible destruction of the internal switches.

Like the mechanical potentiometer the RDAC replaces, the AD5231 parts are totally symmetrical. The resistance between the wiper W and terminal A also produces a digitally controlled complementary resistance R_{WA}. Figure 10 shows the symmetrical programmability of the various terminal connections. When R_{WA} is used, the B-terminal can be let floating or tied to the wiper. Setting the resistance value for R_{WA} starts at a maximum value of resistance and decreases as the data loaded in the latch is increased in value. The general transfer equation for this operation is:

$$R_{WA}(D) = \frac{1024 - D}{1024} \times R_{AB} + R_W \quad (2)$$

For example, the following output resistance values will be set for the following RDAC latch codes with V_{DD} = 5 V (applies to R_{AB} = 10 kΩ Digital Potentiometers):

Table VIII. R_{WA}(D) at Selected Codes for R_{AB} = 10 kΩ

D(DEC)	R_{WA}(D) (Ω)	Output State
1023	24.7	Full-Scale
512	5015	MidScale
1	10005	1 LSB
0	10015	Zero-Scale

The typical distribution of R_{AB} from device-to device matches tightly when they are processed at the same batch. When devices are processed at different time, device-to device matching becomes process lot dependent and exhibits a –40% to +20% variation. The change in R_{AB} with temperature has a 600 ppm/°C temperature coefficient.

PROGRAMMING THE POTENTIOMETER DIVIDER

Voltage Output Operation

The digital potentiometer can be configured to generate an output voltage at the wiper terminal which is proportional to the input voltages applied to terminals A and B. For example connecting A-terminal to 5 V and B-terminal to ground produces an output voltage at the wiper which can be any value starting at 0 V up to 5 V. Each LSB of voltage is equal to the voltage applied across terminal AB divided by the 2^N position resolution of the potentiometer divider.

Since AD5231 can also be supplied by dual supplies, the general equation defining the output voltage at V_W with respect to ground for any given input voltages applied to terminals A and B is:

$$V_W(D) = \frac{D}{1024} \times V_{AB} + V_B \quad (3)$$

Equation 3 assumes V_W is buffered so that the effect of wiper resistance is nulled. Operation of the digital potentiometer in the divider mode results in more accurate operation over temperature. Here the output voltage is dependent on the ratio of the internal resistors and not the absolute value, therefore, the drift improves to 15 ppm/°C. There is no voltage polarity restriction between terminals A, B, and W as long as the terminal voltage (V_{TERM}) stays within $V_{SS} < V_{TERM} < V_{DD}$.

PROGRAMMING EXAMPLES

The following programming examples illustrate typical sequence of events for various features of the AD5231. Users should refer to Table III for the instructions and data word format. The Instruction numbers, addresses, and data appearing at SDI and SDO Pins are based in hexadecimal in the following examples.

Table IX. Scratch Pad Programming

SDI	SDO	Action
$B00100_H$	$XXXXXX_H$	Loads data 100_H into RDAC register, Wiper W moves to 1/4 full-scale position.

Table X. Incrementing RDAC Followed by Storing the Wiper Setting to EEMEM

SDI	SDO	Action
$B00100_H$	$XXXXXX_H$	Loads data 100_H into RDAC register, Wiper W moves to 1/4 full-scale position.
$E0XXXX_H$	$B00100_H$	Increments RDAC register by one to 101_H.
$E0XXXX_H$	$E0XXXX_H$	Increments RDAC register by one to 102_H.
Continue until desired wiper position is reached.		
$20XXXX_H$	$XXXXXX_H$	Saves RDAC register data into EEMEM.
Optionally tie $\overline{WP}$ to GND to protect EEMEM values.		

Table XI. Restoring EEMEM Value to RDAC Register

EEMEM value for RDAC can be restored by Power On, or Strobing $\overline{PR}$ pin, or Programming shown below.

SDI	SDO	Action
$10XXXX_H$	$XXXXXX_H$	Restores EEMEM value to RDAC register.
$00XXXX_H$	$10XXXX_H$	NOP. Recommended step to minimize power consumption.
$8XXXXX_H$	$00XXXX_H$	Reset EEMEM value to RDAC register.

Table XII. Using Left Shift by One to Increment +6 dB Step

SDI	SDO	Action
$C0XXXX_H$	$XXXXXX_H$	Moves wiper to double the present data contained in RDAC register.

Table XIII. Storing Additional User Data in EEMEM

SDI	SDO	Action
$32AAAA_H$	$XXXXXX_H$	Stores data $AAAA_H$ into spare EEMEM location USER1. (Allowable to address in 14 locations with maximum 16 bits of Data.)
335555_H	$32AAAA_H$	Stores data 5555_H into spare EEMEM location USER2. (Allowable to address in 14 locations with maximum 16 bits of Data.)

Table XIV. Reading Back Data From Various Memory Locations

SDI	SDO	Action
$92XXXX_H$	$XXXXXX_H$	Prepares data read from USER1 location.
$00XXXX_H$	$92AAAA_H$	NOP instruction #0 sends 24-bit word out of SDO where the last 16 bits contain the contents of USER1 location. NOP command ensures device returns to idle power dissipation state.

Table XV. Reading Back Wiper Settings

SDI	SDO	Action
$B00200_H$	$XXXXXX_H$	Sets RDAC to midscale.
$C0XXXX_H$	$B00200_H$	Doubles RDAC from midscale to full-scale. (Left shift instructions)
$A0XXXX_H$	$C0XXXX_H$	Prepares reading wiper setting from RDAC register.
$XXXXXX_H$	$A003FF_H$	Readback full-scale value from RDAC register.

TEST CIRCUITS

Figures 11 to 19 define the test conditions used in the product specifications table.

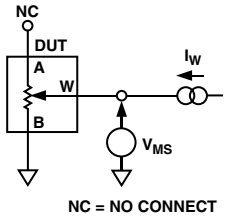


Figure 11. Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)

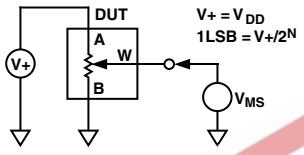


Figure 12. Potentiometer Divider Nonlinearity Error Test Circuit (INL, DNL)

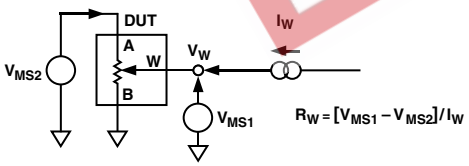


Figure 13. Wiper Resistance Test Circuit

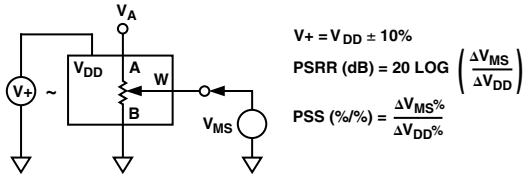


Figure 14. Power Supply Sensitivity Test Circuit (PSS, PSRR)

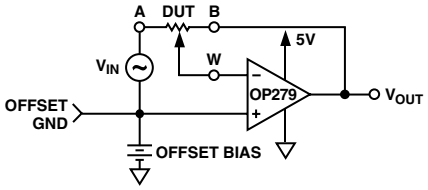


Figure 15. Inverting Gain Test Circuit

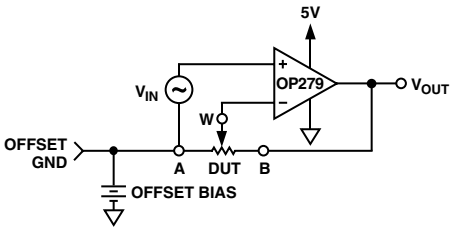


Figure 16. Noninverting Gain Test Circuit

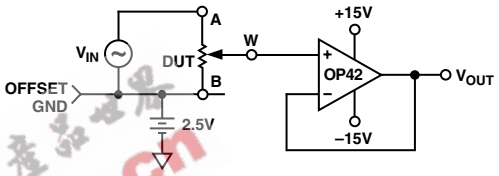


Figure 17. Gain vs. Frequency Test Circuit

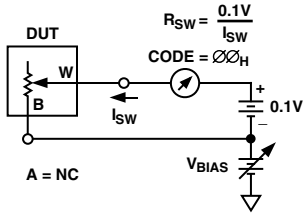


Figure 18. Incremental ON Resistance Test Circuit

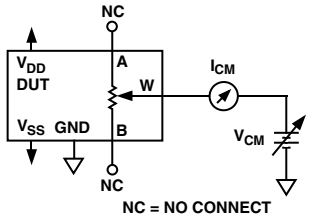


Figure 19. Common-Mode Leakage Current Test Circuit

FLASH/EEMEM RELIABILITY

The Flash/EE Memory array on the AD5231 is fully qualified for two key Flash/EE memory characteristics, namely Flash/EE Memory Cycling Endurance and Flash/EE Memory Data Retention.

Endurance quantifies the ability of the Flash/EE memory to be cycled through many Program, Read, and Erase cycles. In real terms, a single endurance cycle is composed of four independent, sequential events. These events are defined as:

- Initial Page Erase Sequence
- Read/Verify Sequence
- Byte Program Sequence
- Second Read/Verify Sequence

During reliability qualification Flash/EE memory is cycled from 000_H to $3FF_H$ until a first fail is recorded signifying the endurance limit of the on-chip Flash/EE memory.

As indicated in the specification pages of this data sheet, the AD5231 Flash/EE Memory Endurance qualification has been carried out in accordance with JEDEC Specification A117 over the industrial temperature range of –40°C to +85°C. The results allow the specification of a minimum endurance figure over supply and temperature of 100,000 cycles, with an endurance figure of 700,000 cycles being typical of operation at 25°C.

Retention quantifies the ability of the Flash/EE memory to retain its programmed data over time. Again, the AD5231 has been qualified in accordance with the formal JEDEC Retention Lifetime Specification (A117) at a specific junction temperature (T_J = 55°C). As part of this qualification procedure, the Flash/EE memory is cycled to its specified endurance limit described above, before data retention is characterized. This means that the Flash/EE memory is guaranteed to retain its data for its full specified retention lifetime every time the Flash/EE memory is reprogrammed. It should also be noted that retention lifetime, based on an activation energy of 0.6 eV, will derate with T_J as shown in Figure 20. For example, the data is retained for 100 years at 55°C operation, but reduces to 15 years at 85°C operation. Beyond such limit, the part must be reprogrammed so that the data can be restored.

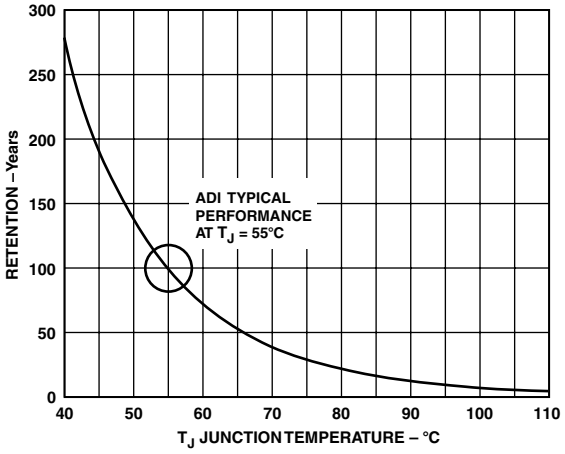


Figure 20. Flash/EE Memory Data Retention

APPLICATIONS

Bipolar Operation From Dual Supplies

The AD5231 can be operated from dual supplies ±2.5 V, which enables control of ground referenced ac signals or bipolar operation. AC signal, as high as V_{DD}/V_{SS}, can be applied directly across terminals A-B with output taking from terminal W. (See Figure 21 for a typical circuit connection.)

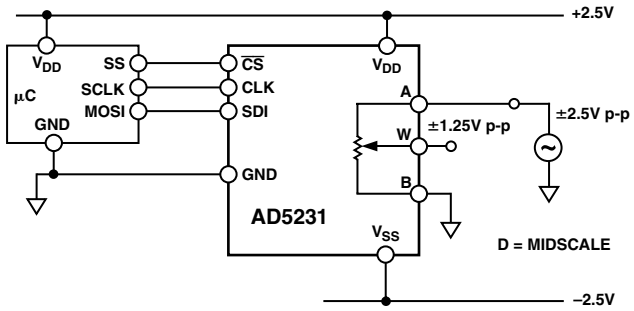


Figure 21. Bipolar Operation from Dual Supplies

High Voltage Operation

The Digital Potentiometer can be placed directly in the feedback or input path of an op amp for gain control, provided that the voltage across terminals A-B, W-A, or W-B does not exceed |5 V|. When high voltage gain is needed, users should set a fixed gain in an op amp operated at +15 V, and let the digital potentiometer control the adjustable input. Figure 22 shows a simple implementation.

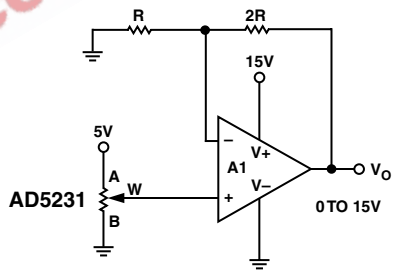


Figure 22. 15 V Voltage Span Control

Bipolar Programmable Gain Amplifier

There are several ways to achieve bipolar gain. Figure 23 shows one versatile implementation. Digital potentiometer U1 sets the adjustment range, the wiper voltage V_{W2} can therefore be programmed between V_i and $-KV_i$ at a given U2 setting. For linear adjustment, configure A2 as a noninverting amplifier and the transfer function becomes:

$$\frac{V_O}{V_i} = \left(1 + \frac{R2}{R1}\right) \times \left(\frac{D_2}{1024} \times (1+K) - K\right) \quad (4)$$

where:
K is the ratio of R_{WB}/R_{WA} which is set by U1.
D = Decimal Equivalent of the Input Code

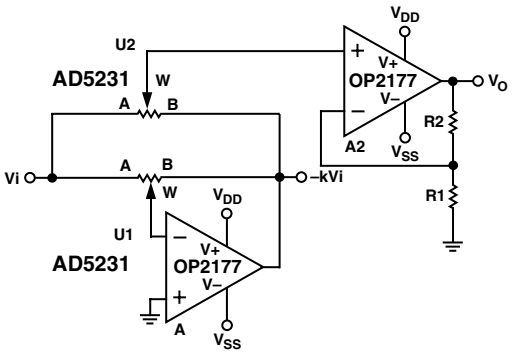


Figure 23. Bipolar Programmable Gain Amplifier

In the simpler (and much more usual) case where K = 1, a pair of matched resistors can replace U1. Equation 4 simplifies to:

$$\frac{V_O}{V_I} = \left(1 + \frac{R2}{R1}\right) \times \left(\frac{2D_2}{1024} - 1\right) \quad (5)$$

Table XVI shows the result of adjusting D with A2 configured as a unity gain, a gain of 2, and a gain of 10. The result is a bipolar amplifier with linearly programmable gain and 1024-step resolution.

Table XVI. Result of Bipolar Gain Amplifier

D	R1 = ∞, R2 = 0	R1 = R2	R2 = 9 R1
0	–1	–2	–10
256	–0.5	–1	–5
512	0	0	0
768	0.5	1	5
1023	0.992	1.984	9.92

10-Bit Bipolar DAC

If the circuit is changed in Figure 23 with the input taking from a voltage reference and configure A2 as a buffer, a 10-bit bipolar DAC can be realized. Compared to the conventional DAC, this circuit offers comparable resolution but not the precision because of the wiper resistance effects. Degradation of the nonlinearity and temperature coefficient are prominent near both ends of the adjustment range. On the other hand, this circuit offers a unique nonvolatile memory feature which in some cases outweigh the shortfall of nonprecision. The output of this circuit is:

$$V_O = \left(\frac{2D_2}{1024} - 1\right) \times V_{REF} \quad (6)$$

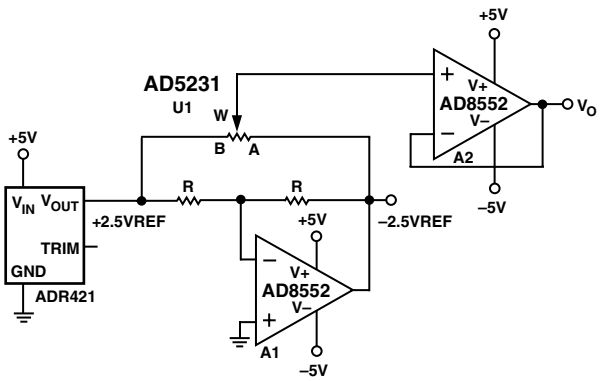


Figure 24. 10-Bit Bipolar DAC

Programmable Voltage Reference

For programmable voltage divider mode operation (Figure 25) it is common to buffer the output of the digital potentiometer unless the load is much larger than the source resistance R_{WB}. In addition, the current handling of the digital potentiometer is limited by its maximum operating voltage, power dissipation, and the maximum current handling of the internal switches at a given resistance (see TPC 20). As a result, the added buffer can be used to deliver the current needed to the load as long as it is within its current handling capability.

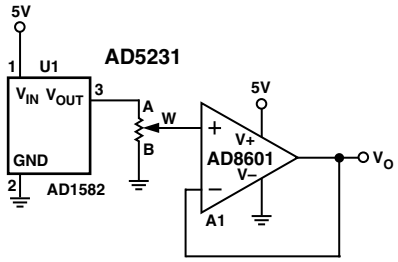


Figure 25. Programmable Voltage Reference

Programmable Voltage Source with Boosted Output

For applications such as laser diode driver or turnable laser, requiring high current adjustment a boosted voltage source can be considered (see Figure 26).

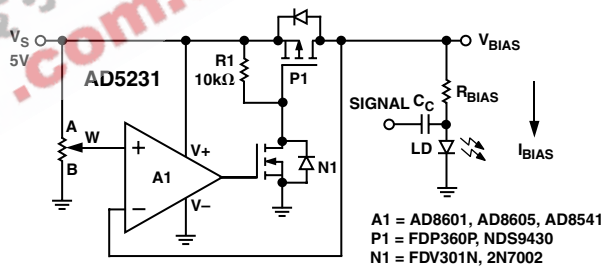


Figure 26. Boosted Voltage Source

In this circuit, the inverting input of the op amp forces the V_{BIAS} to be equal to the wiper voltage set by the digital potentiometer. The load current is then delivered by the supply via the P-Ch FET P1. The N-Ch FET N1 simplifies the op amp driving requirement. Resistor R1 is needed to prevent P1 for not turning off once it is on. The choice of R1 is a balance between the power loss of this resistor and the output turn off time. N1 can be any general purpose signal FET; on the other hand, P1 is driven in the saturation state and therefore its power handling must be adequate to dissipate $(V_S - V_{BIAS}) \times I_{BIAS}$ power. This circuit can source maximum of 100 mA at 5 V supply. Higher current can be achieved with P1 in larger package. Note a single N-Ch FET can replace P1, N1, and R1 altogether. However, the output swing will be limited unless separate power supplies are used. For precision application, a voltage reference such as ADR423, ADR292, and AD1584, can be applied at the input of the digital potentiometer.

Programmable 4 mA to 20 mA Current Source

A programmable 4 mA to 20 mA current source can be implemented with the circuit shown in Figure 27.

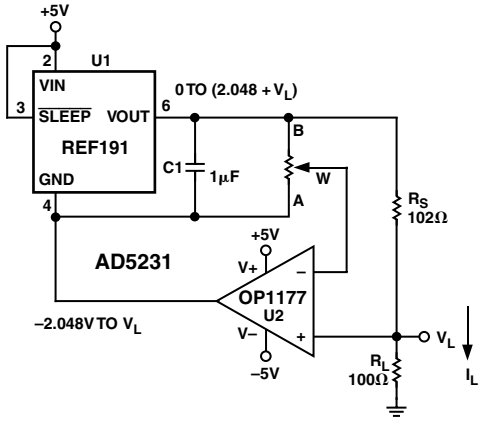


Figure 27. Programmable 4 mA to 20 mA Current Source

REF191 is a unique low supply headroom precision reference that can deliver the 20 mA needed at 2.048 V. The load current is simply the voltage across terminals B-to-W of the digital potentiometer divided by R_S:

$$I_L = \left(\frac{V_{REF} \times D}{R_S}\right) \quad (7)$$

The circuit is simple, but be aware that there are two issues. First, dual supply op amps are ideal because the ground potential of REF191 can swing from –2.048 V at zero scale to V_L at full scale of the potentiometer setting. Although the circuit works under single supply, the programmable resolution of the system will be reduced. Second, the voltage compliance at V_L is limited to 2.5 V or equivalently a 125 Ω load. Should higher voltage compliance be needed, users may consider digital potentiometers AD5260, AD5280, and AD7376. Figure 28 below shows an alternate circuit for high voltage compliance.

Programmable Bidirectional Current Source

For applications that require bidirectional current control or higher voltage compliance, a Howland current pump can be a solution. If the resistors are matched, the load current is:

$$I_L = \frac{\frac{(R2A + R2B)}{R1}}{R2B} \times V_W \quad (8)$$

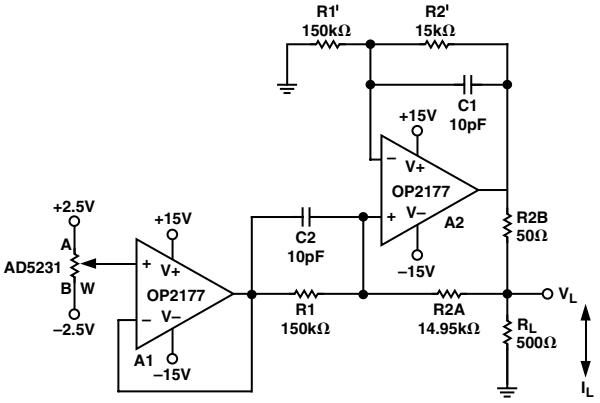


Figure 28. Programmable Bidirectional Current Source

R2B in theory can be made as small as needed to achieve the current needed within A2 output current driving capability. In this circuit OP2177 delivers ±5 mA in both directions and the voltage compliance approaches 15 V. It can be shown that the output impedance is:

$$Z_O = \frac{R1}{\left(\frac{R1 \times R2'}{R1' \times R2} - 1\right)} \quad (9)$$

Z_O can be infinite if resistors $R1$ and $R2$ match precisely with $R1$ and $R2A + R2B$ respectively. On the other hand, Z_O can be negative if the resistors are not matched. As a result, C1 and C2, in the range of 1 pF to 10 pF, are needed to prevent the oscillation.

Resistance Scaling

AD5231 offers 10 kΩ, 50 kΩ, and 100 kΩ nominal resistance. For users who need lower resistance but want to maintain the numbers of step adjustment, they can parallel multiple devices. For example, Figure 29 shows a simple scheme of paralleling two AD5231. In order to adjust half of the resistance linearly per step, users need to program both devices coherently with the same settings and tie the terminals as shown.

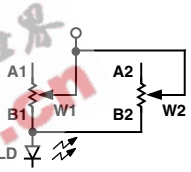


Figure 29. Reduce Resistance by Half with Linear Adjustment Characteristics

In voltage divider mode, a much lower resistance can be achieved by paralleling a discrete resistor as shown in Figure 30. The equivalent resistance become:

$$R_{WB_{eq}} = \frac{D}{1024}(R1//R2) + R_W \quad (10)$$

$$R_{WA_{eq}} = \left(1 - \frac{D}{1024}\right)(R1//R2) + R_W \quad (11)$$

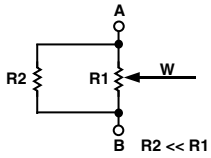


Figure 30. Lowering the Nominal Resistance

Figures 29 and 30 show that the digital potentiometers change steps linearly. On the other hand, log taper adjustment is usually preferred in applications like audio control. Figure 31 shows another way of resistance scaling. In this configuration, the smaller the R2 with respect to R1, the more the pseudo log taper characteristic behaves.

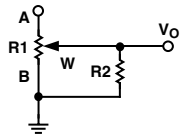


Figure 31. Resistor Scaling with Pseudo Log Adjustment Characteristics

RDAC CIRCUIT SIMULATION MODEL

The internal parasitic capacitances and the external load dominates the ac characteristics of the RDACs. Configured as a potentiometer divider the –3 dB bandwidth of the AD5231BRU10 (10 kΩ resistor) measures 370 kHz at half scale. TPC 10 provides the large signal BODE plot characteristics. A parasitic simulation mode is shown in Figure 32. Listing I provides a macro model net list for the 10 kΩ RDAC:

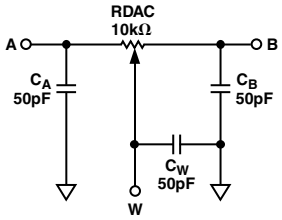


Figure 32. RDAC Circuit Simulation Model for RDAC = 10 kΩ

Listing I. Macro Model Net List for RDAC

```
.PARAM D = 1024, RDAC = 10E3
*
.SUBCKT DPOT (A, W, B)
*
CA      A       0       50E-12
RAW     A       W       {(1-D/1024)*RDAC+15}
CW      W       0       50E-12
RBW     W       B       {D/1024*RDAC+15}
CB      B       0       50E-12
*
.ENDS DPOT
```

DIGITAL POTENTIOMETER FAMILY SELECTION GUIDE

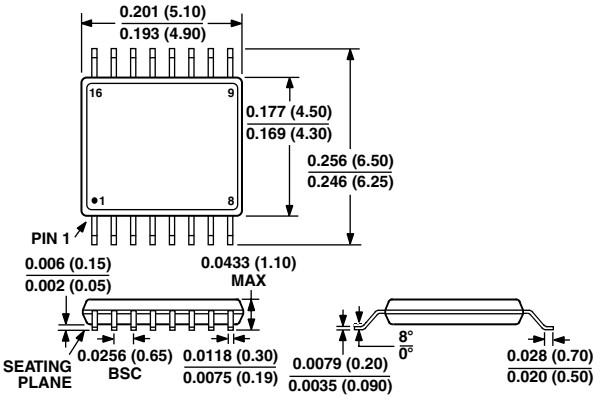
Part Number	Number of VRs per Package	Terminal Voltage Range (V)	Interface Data Control	Nominal Resistance (kΩ)	Resolution (Number of Wiper Positions)	Power Supply Current (I_{DD}) (μA)	Packages	Comments
AD5201	1	±3, +5.5	3-Wire	10, 50	33	40	μSOIC-10	Full ac Specs, Dual Supply, Power-On Reset, Low Cost
AD5220	1	5.5	UP/ DOWN	10, 50, 100	128	40	PDIP, SO-8, μSOIC-8	No Rollover, Power-On Reset
AD7376	1	±15, +28	3-Wire	10, 50, 100, 1000	128	100	PDIP-14, SOL-16, TSSOP-14	Single 28 V or Dual ±15 V Supply Operation
AD5200	1	±3, +5.5	3-Wire	10, 50	256	40	μSOIC-10	Full ac Specs, Dual Supply, Power-On Reset
AD8400	1	5.5	3-Wire	1, 10, 50, 100	256	5	SO-8	Full ac Specs
AD5260	1	±5, +15	3-Wire	20, 50, 200	256	60	TSSOP-14	5 V to 15 V or ±5 V Operation, TC < 50 ppm/°C
AD5241	1	±3, +5.5	2-Wire	10, 100, 1000	256	50	SO-14, TSSOP-14	I^2C Compatible, TC < 50 ppm/°C
AD5231	1	±2.75, +5.5	3-Wire	10, 50, 100	1024	20	TSSOP-16	Nonvolatile Memory, Direct Program, I/D, ±6 dB Settability
AD5222	2	±3, +5.5	UP/ DOWN	10, 50, 100, 1000	128	80	SO-14, TSSOP-14	No Rollover, Stereo Power-On Reset, TC < 50 ppm/°C
AD8402	2	5.5	3-Wire	1, 10, 50, 100	256	5	PDIP, SO-14, TSSOP-14	Full ac Specs, nA Shutdown Current
AD5207	2	±3, +5.5	3-Wire	10, 50, 100	256	40	TSSOP-14	Full ac Specs, Dual Supply, Power-On Reset, SDO
AD5232	2	±2.75, +5.5	3-Wire	10, 50, 100	256	20	TSSOP-16	Nonvolatile Memory, Direct Program, I/D, ±6 dB Settability
AD5235	2	±2.75, +5.5	3-Wire	25, 250	1024	20	TSSOP-16	Nonvolatile Memory, Direct Program, TC < 50 ppm/°C
AD5242	2	±3, +5.5	2-Wire	10, 100, 1000	256	50	SO-16, TSSOP-16	I^2C Compatible, TC < 50 ppm/°C
AD5262	2	±5, +15	3-Wire	20, 50, 200	256	60	TSSOP-16	5 V to 15 V or ±5 V Operation, TC < 50 ppm/°C
AD5203	4	5.5	3-Wire	10, 100	64	5	PDIP, SOL-24, TSSOP-24	Full ac Specs, nA Shutdown Current
AD5233	4	±2.75, +5.5	3-Wire	10, 50, 100	64	20	TSSOP-24	Nonvolatile Memory, Direct Program, I/D, ±6 dB settability
AD5204	4	±3, +5.5	3-Wire	10, 50, 100	256	60	PDIP, SOL-24, TSSOP-24	Full ac Specs, Dual Supply, Power-On Reset
AD8403	4	5.5	3-Wire	1, 10, 50, 100	256	5	PDIP, SOL-24, TSSOP-24	Full ac Specs, nA Shutdown Current
AD5206	6	±3, +5.5	3-Wire	10, 50, 100	256	60	PDIP, SOL-24, TSSOP-24	Full AC specs, Dual Supply, Power-On Reset

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

16-Lead TSSOP

(RU-16)



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