Integrated LCD Grayscale Generator

ADD8502

FEATURES

Two Mask Programmable Sets of Five Reference Levels
Dual 10-Bit DACs for Flicker Offset and Range Adjustment
Integrated V_{COM} Switching
Single-Supply Operation: 5.0 V
Low Supply Current: 300 μA
Global Power Save Mode: 1 μA Max
Fast Settling Time for Load Change: 20 μs
Stable with 20 nF/100 Ω Loads
CMOS/TTL Input Levels

APPLICATIONS

Color TFT Cell Phones
Color TFT PDAs

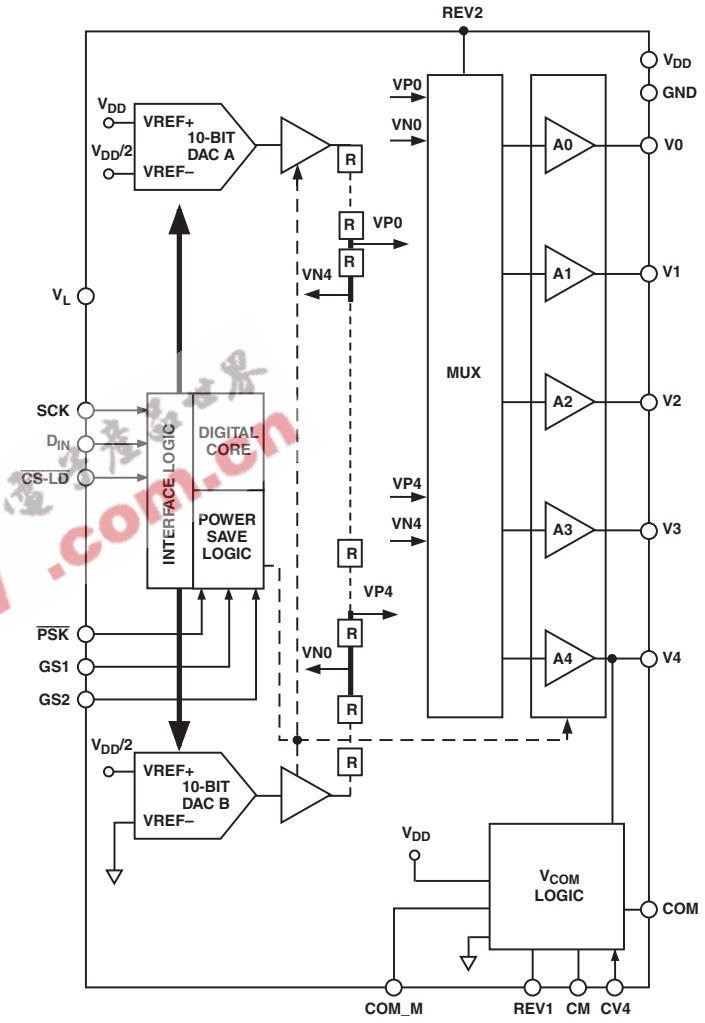
GENERAL DESCRIPTION

The ADD8502 is an integrated, high accuracy, programmable grayscale generator. Two sets of five output reference voltages are mask programmed to 0.2% resolution. The outputs switch between the two sets of five levels. The reference levels are selected from a 512 tap resistor network using a via mask.

ADD8502 includes two serially addressable, 10-bit digital-to-analog converters (DACs) and five fast, low current buffers. The dual DACs set the endpoint voltages applied to the resistor network to adjust for flicker and range. The two power save modes can reduce the total current to less than 1 μA and feature fast recovery time from Shutdown/Sleep Mode. The ADD8502 accepts CMOS or TTL inputs for all controls, including the common drive circuit levels.

ADD8502 operates over the industrial temperature range from –40°C to +85°C and is available in a space-saving 24-lead 4 mm × 4 mm frame chip scale package.

FUNCTIONAL BLOCK DIAGRAM



REV. 0

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ADD8502–SPECIFICATIONS (@ V_{DD} = 5.0 V, −40°C ≤ T_A ≤ +85°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SYSTEM ACCURACY						
V_{OUT} Error				3	20	mV
Swing Error[1]		$(V_{Pn} - V_{Nn}) - (V_{Pi} - V_{Ni})$		1	17	mV
Mean Error[2]		$(V_{Pn} + V_{Nn})/2 - (V_{Pi} + V_{Ni})/2)$		3	21	mV
Mean Error between Adjacent Channels[3]				3	21	mV
Mean Error between V0 and V4[4]				3	25	mV
DAC ACCURACY						
Resolution				10		Bits
Differential Nonlinearity	DNL			±0.25		LSB
Integral Nonlinearity[5]	INL			±0.5		LSB
Offset Error				±0.4		% of FSR
Gain Error				±0.15		% of FSR
OUTPUT CHARACTERISTICS						
Output Current	I_{OUT}	$(V_{DD} - 1\ V)$		25		mA
Short Circuit Current	I_{SC}	Short to Ground		60		mA
Output Leakage Current in High-Z Mode	$I_{LEAKAGE}$	High-Z Mode		0.01	1.0	µA
Slew Rate	SR	R_L = 100 kΩ		1.25		V/µs
Settling Time to 1%	t_S	V0 to V4 Step Size		8	12	µs
Slew Rate[5]	SR	L_D =100 Ω Series 16 nF		0.7		V/µs
Settling Time to 1%[5]	t_S	V0 to V4 Step Size		8	12	µs
Phase Margin	ϕo			67		Degrees
V_{COM} SWITCHES ACTIVE IMPEDANCE						
COM to V_{DD}	Z	See Table IV		25	50	Ω
COM to GND	Z			25	50	Ω
COM to COM_M	Z	I = 20 mA		25	50	Ω
COM to V4	Z			25	50	Ω
MASK PROGRAMMABLE RESISTOR CHAIN						
Resistor Matching	R_{MATCH}	Any Two Segments between 512 Resistor String		1		%
POWER SUPPLY						
Supply Voltage	V_{DD}		4.5	5	5.5	V
Supply Current	I_{SY}	V_{DD} = 5 V; No Load	190	270	400	µA
Shutdown Supply Current	I_{SY-GLB}	Full Shutdown Mode		0.2	1	µA
Sleep Supply Current	$I_{SY-GS1-3}$	Mid 3 Buffers Shutdown	140	175	210	µA
Shutdown Recovery Time		Global PD to 1%		23	30	µs
Sleep Recovery Time		V1–V3 Off to 1%		10	15	µs
LOGIC SUPPLY						
Logic Input Voltage Level	V_L		2.3	3.3	5.5	V
Logic Input Current	I_{VL}			0.01	1	µA
DIGITAL I/O						
Digital Input High Voltage	V_{IH}		$V_L \times 0.7$			V
Digital Input Low Voltage	V_{IL}				$V_L \times 0.3$	V
Digital Input Current	I_{IN}	$GND \le V_{IN} \le 5.5\ V$			±1	µA
Digital Input Capacitance	C_{IN}				10	pF

NOTES

[1]Swing error is a comparison of measured V_{OUT} step versus theoretical V_{OUT} step. Theoretical values can be found on the Mask Tap Point Option sheet.

[2]Mean error is measured V_{OUT} mean versus theoretical V_{OUT} mean (see Figure 3).

[3]Mean errors between two adjacent channels versus theoretical (see Figure 3).

[4]Mean errors between V0 and V4 versus theoretical (see Figure 3).

[5]Slew rate and settling time are measured between the output resistor and the capacitor (see Figure 1).

Specifications subject to change without notice.

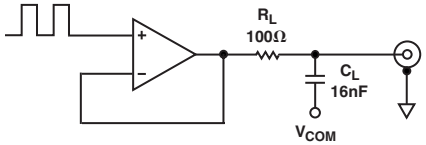


Figure 1. Slew Rate Diagram

Table I. Serial Data Timing Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
SCK Cycle Time	t_1	100			ns
SCK High Time	t_2	45			ns
SCK Low Time	t_3	45			ns
$\overline{\text{CS-LD}}$ Setup Time	t_4	20			ns
Data Setup Time	t_5	5			ns
Data Hold Time	t_6	5			ns
LSB SCK High to $\overline{\text{CS-LD}}$ High	t_7	5			ns
Minimum $\overline{\text{CS-LD}}$ High Time	t_8	10			ns
SCK to $\overline{\text{CS-LD}}$ Active Edge Setup Time	t_9	5			ns
$\overline{\text{CS-LD}}$ High to SCK Positive Edge	t_{10}	10			ns
SCK Frequency (Square Wave)				10	MHz

NOTES
[1]All input signals are specified with rise/fall time –5 ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_S + V_{IH})/2$.
[2]See Figure 2.

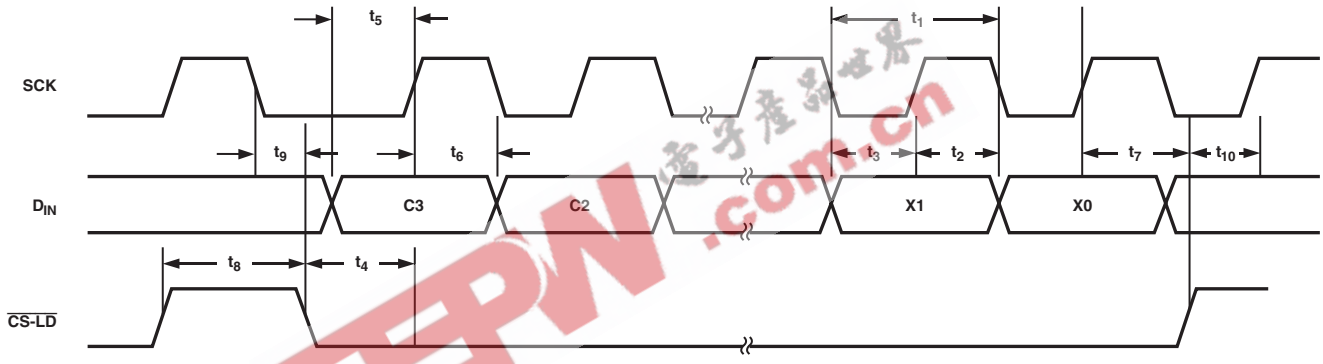


Figure 2. Serial Write Interface

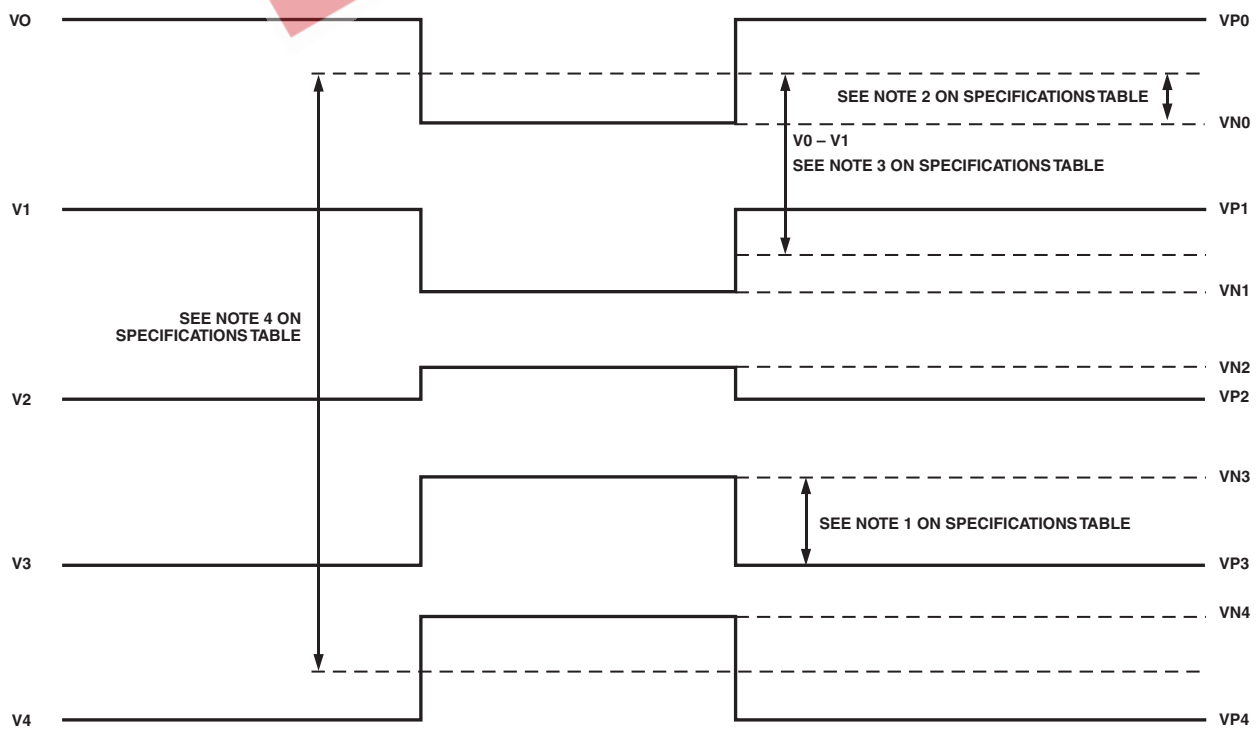


Figure 3. Output Wave Form Diagram

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to GND . . . . . –0.3 V to +7 V
V_L to GND . . . . . –0.3 V to +7 V
Digital Input Voltage to GND . . . . . –0.3 V to +7 V
V_{OUT} to GND . . . . . –0.3 V to V_{DD} +0.3 V
V_{COM} to GND . . . . . –0.3 V to V_{DD} +0.3 V
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature Range (Soldering, 10 sec)
Vapor Phase (60 sec) . . . . . 300°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Type	θ_{JA}[1]	Ψ_{JB}[2]	Unit
24-Lead LFCSP (ACP)	34.8	13	°C/W

NOTES
[1]θ_{JA} is specified for worst-case conditions, i.e., θ_{JA} is specified for device soldered in circuit board for surface-mount packages.
[2]Ψ_{JB} is applied for calculating the junction temperature by reference to the board temperature.

ORDERING GUIDE

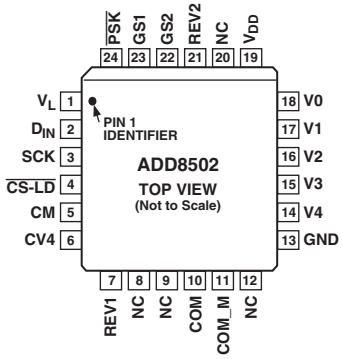
Model	Temperature Range	Package Description	Package Option
ADD8502ACP	–40°C to +85°C	24-Lead LFCSP	CP-24

Available in 7" reel only.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADD8502 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



NC = NO CONNECT

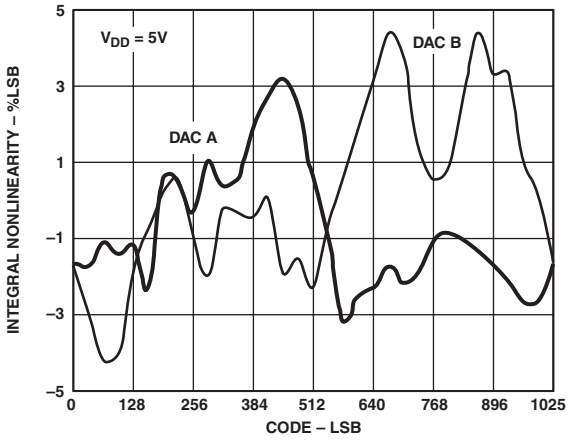
PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Name	I/O	Description
1	V_L	Logic Select Pin	I	Logic Supply Voltage. Connect to supply used for system logic. Can accept 2.7 V to V_{DD}.
2	D_{IN}	Serial Data Input	I	When CS is LOW, the input on this pin is shifted into the internal shift register on the rising edge of SCK.
3	SCK	Serial Clock	I	Accepts up to 10 MHz input. The rising edge on this clock will shift the data on D_{IN} Pin into the internal shift registers.
4	$\overline{\text{CS-LD}}$	Load	I	When $\overline{\text{CS-LD}}$ is LOW, SCK is enabled for shifting data on the D_{IN} input into the internal shift register on the rising edge of SCK. Data is loaded MSB first.
5	CM	Logic Control 2 for V_{COM}	I	When CM is LOW, COM will output the voltage level input on COM_M. When CM is HIGH, COM levels will be determined by the input on REV1.
6	CV4	Logic Control V4	I	If CV4 is HIGH, V4 output is the output of the op amp A4. If CV4 is LOW, V4 is connected to COM and op amp A4 is shut down. Refer to Table II.
7	REV1	Logic Control 1 for V_{COM}	I	With CM HIGH, a HIGH on REV1 will cause COM to output the voltage level input at V_{DD}. A LOW on REV1 will cause COM to output the voltage level input at GND.
8	NC	No Connect		Unused Pin
9	NC	No Connect		Unused Pin
10	COM	Common Output	O	If CM is LOW, COM will output the voltage input at COM_M. If CM is HIGH, COM will output the voltage input at V_{DD} when REV1 is HIGH and will output the voltage input at GND when REV1 is LOW. Refer to Table II.
11	COM_M	Common System V_{REF}	I	COM_M is a system voltage reference input between 2.5 V and 3.5 V. This may be the system 3.3 V supply.
12	NC	No Connect		Unused Pin
13	GND	Ground	I	Ground. Nominally 0 V.
14	V4	Output	O	Buffers are rail-to-rail buffers that can drive high capacitive loads (>16.5 nF). When $\overline{\text{PSK}}$ is LOW, these outputs will be Hi-Z.
15	V3	Output	O	Buffers are rail-to-rail buffers that can drive high capacitive loads (>16.5 nF). When $\overline{\text{PSK}}$ is LOW or GS1 and GS2 = HIGH, these outputs will be Hi-Z.
16	V2	Output	O	Buffers are rail-to-rail buffers that can drive high capacitive loads (>16.5 nF). When $\overline{\text{PSK}}$ is LOW or GS1 and GS2 = HIGH, these outputs will be Hi-Z.
17	V1	Output	O	Buffers are rail-to-rail buffers that can drive high capacitive loads (>16.5 nF). When $\overline{\text{PSK}}$ is LOW or GS1 and GS2 = HIGH, these outputs will be Hi-Z.
18	V0	Output	O	Buffers are rail-to-rail buffers that can drive high capacitive loads (>16.5 nF). When $\overline{\text{PSK}}$ is LOW, these outputs will be Hi-Z.
19	V_{DD}	Supply	I	Supply Voltage. Nominally 5 V.
20	NC	No Connect		Unused Pin

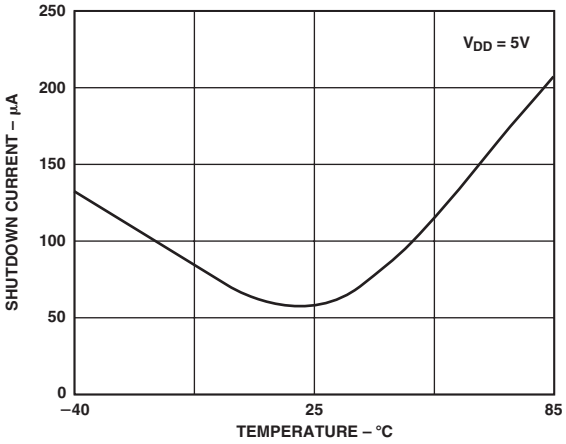
Pin No.	Mnemonic	Name	I/O	Description
21	REV2	Reference Output Select	I	When $\overline{PSK}$ is HIGH and GS1 or GS2 is LOW, then INVERT selects the output levels on V0 to V4. If INVERT is HIGH, outputs V0 to V4 are connected to reference levels VP0 to VP4, respectively. If INVERT is LOW, outputs V0 to V4 are connected to reference levels VN0 to VN4, respectively. When $\overline{PSK}$ is HIGH and GS1 and GS2 are HIGH, V1–V3 are, Hi-Z state, but V0 and V4 are still connected to reference levels VP0 and VP4 when INVERT is HIGH. Outputs V0 and V4 switch to VN0 and VN4 when REV is LOW.
22	GS2	Sleep Mode Select	I	When GS1 and GS2 are HIGH, the middle three output buffers are shut down and V1, V2, and V3 are put into Hi-Z states. Other combinations of GS1 and GS2 leave the outputs of A1 to A3 fully active.
23	GS1	Sleep Mode Select	I	When GS1 and GS2 are HIGH, the middle three output buffers are shut down and V1, V2, and V3 are Hi-Z. Other combinations of GS1 and GS2 leave the outputs of A1 to A3 fully active.
24	$\overline{PSK}$	Global Power Shutdown	I	When $\overline{PSK}$ is pulled LOW, the chip will be put into the full Power-Down Mode. The DACs, resistor ladder network preamps, and output buffers will all be shut down, and A0 to A4 will be in Hi-Z states. Recovery from full power-down to normal operation is within 30 µs.

All digital inputs accept CMOS or TTL logic levels.

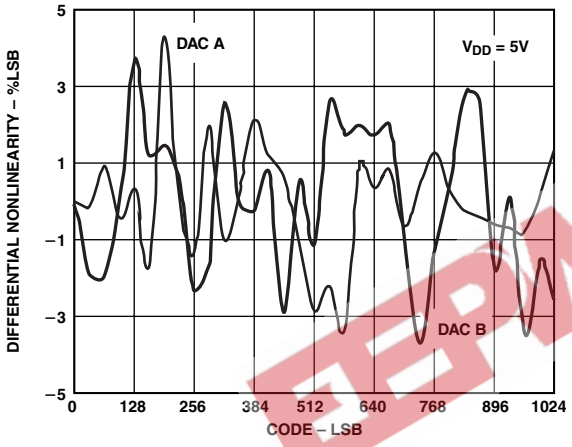
Typical Performance Characteristics–ADD8502



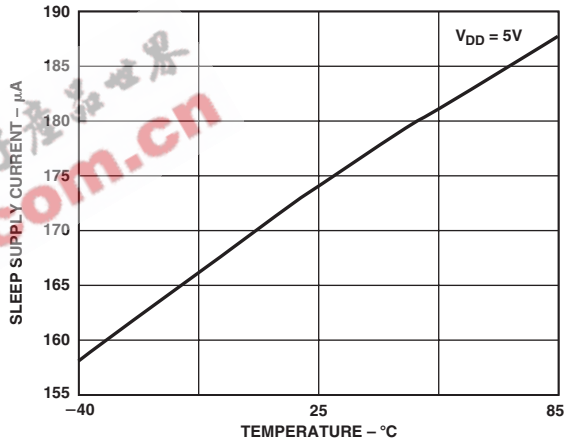
TPC 1. DAC Integral Nonlinearity



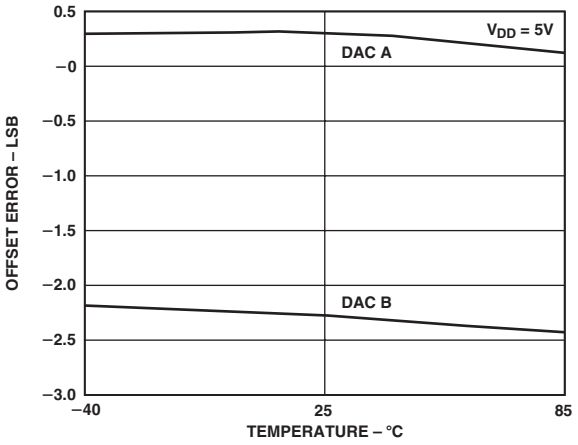
TPC 4. Shutdown Current vs. Temperature



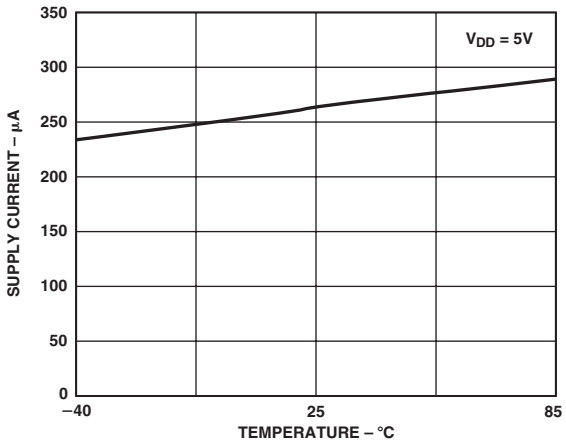
TPC 2. DAC Differential Nonlinearity



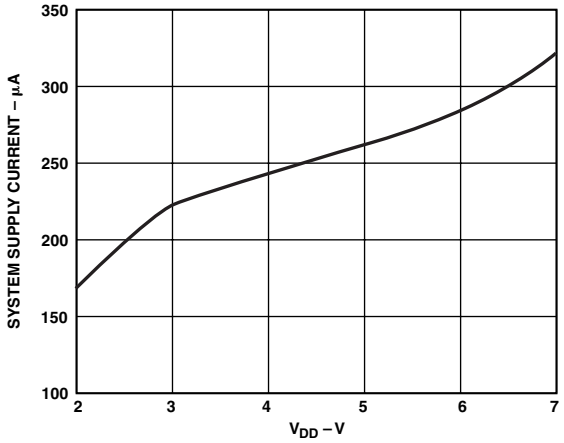
TPC 5. Sleep Supply Current vs. Temperature



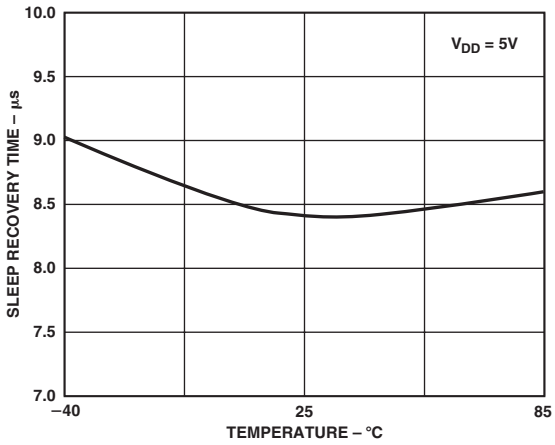
TPC 3. Offset Error vs. Temperature



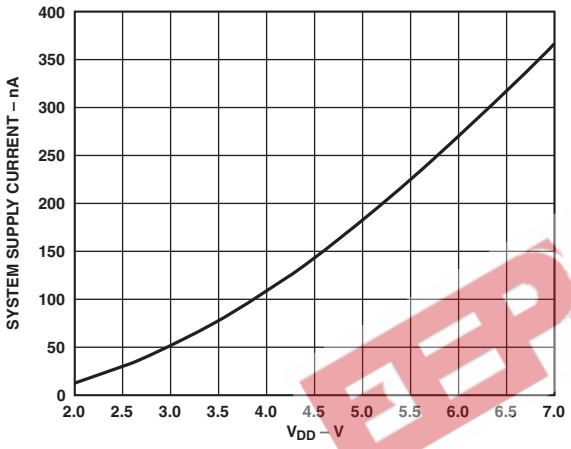
TPC 6. Supply Current vs. Temperature



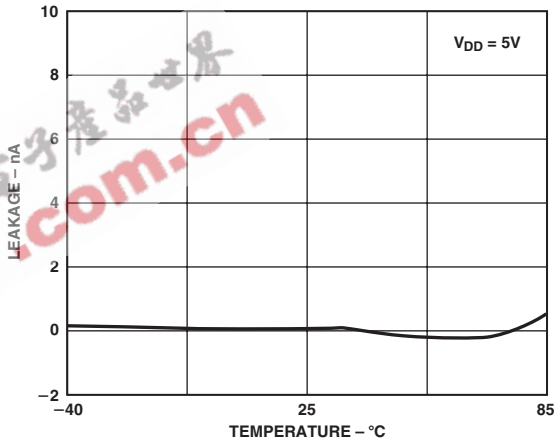
TPC 7. System Supply Current at Full Power



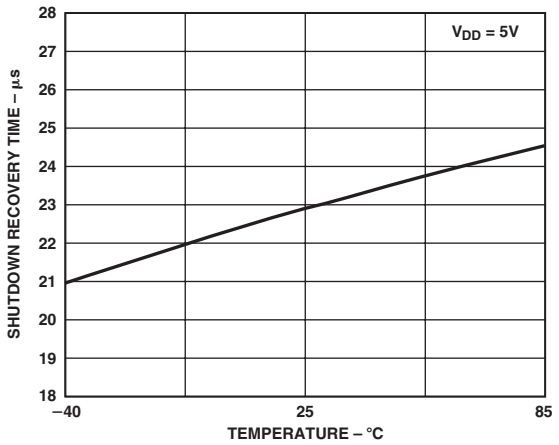
TPC 10. Sleep Recovery Time vs. Temperature



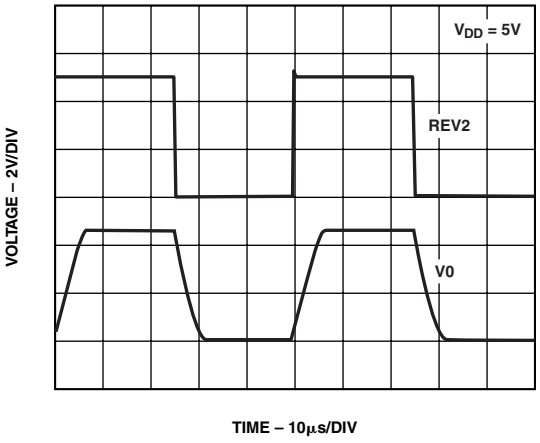
TPC 8. System Supply Current at Shutdown



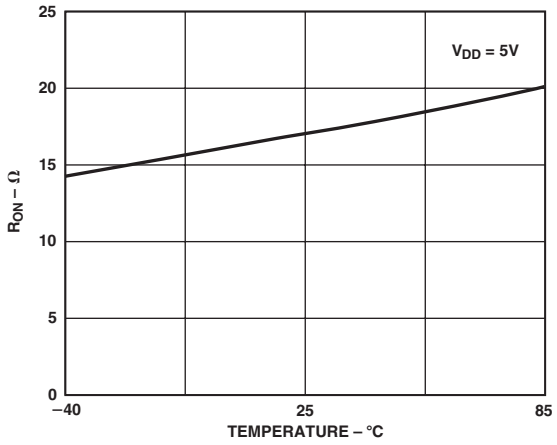
TPC 11. Output Leakage



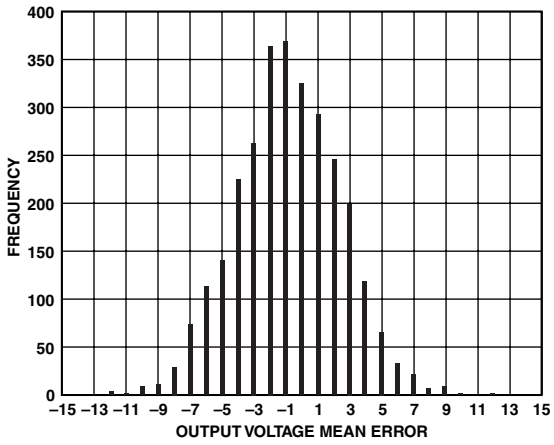
TPC 9. Shutdown Recovery Time vs. Temperature



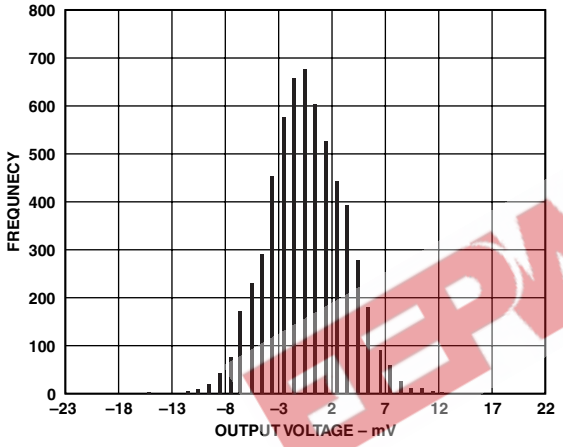
TPC 12. V0 Output Swing Response to REV2



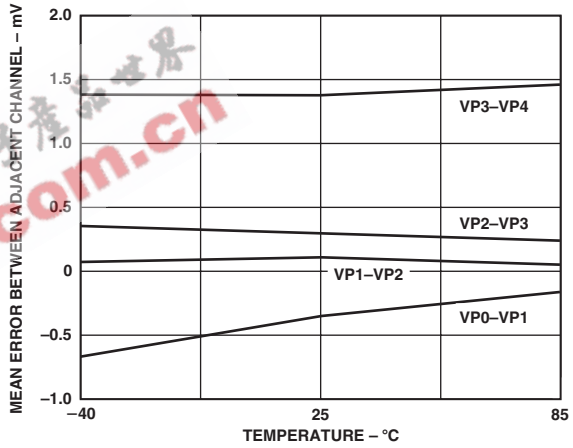
TPC 13. V_{COM} Switch-On-Resistance vs. Temperature



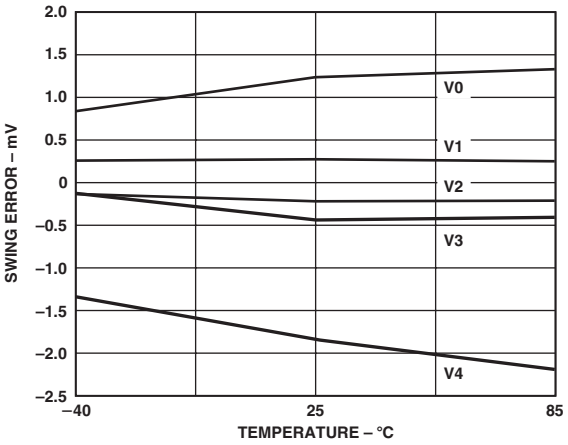
TPC 16. V_{OUT} Swing Mean vs. Distribution



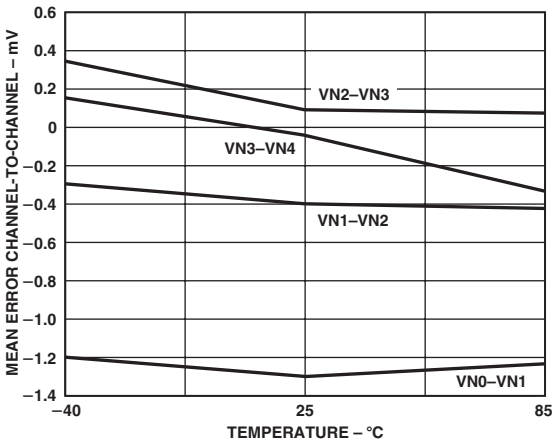
TPC 14. V_{OUT} Error Distribution



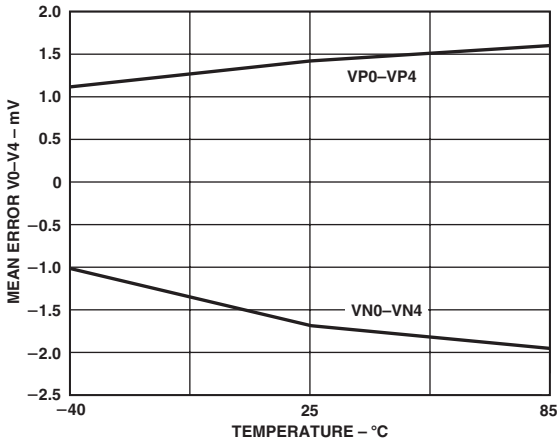
TPC 17. Mean Error between Adjacent Channel vs. Temperature



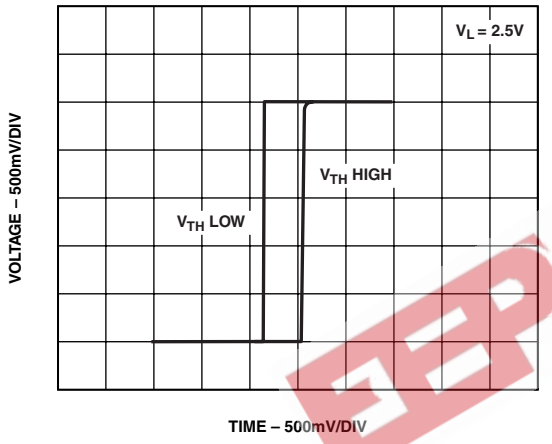
TPC 15. Swing Error vs. Temperature



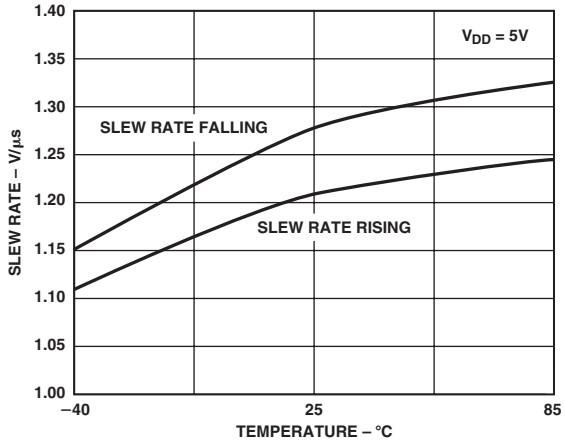
TPC 18. Mean Error between Adjacent Channel vs. Temperature



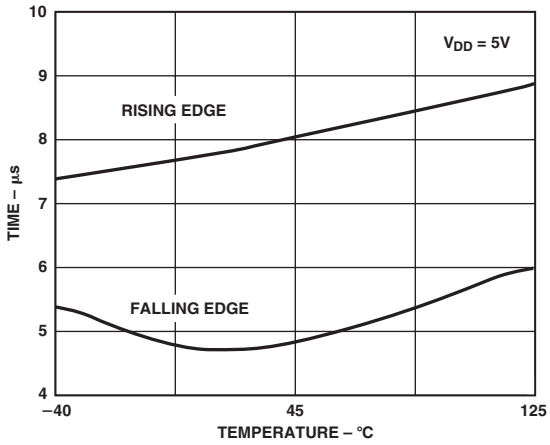
TPC 19. Mean Error between V0 and V4 vs. Temperature



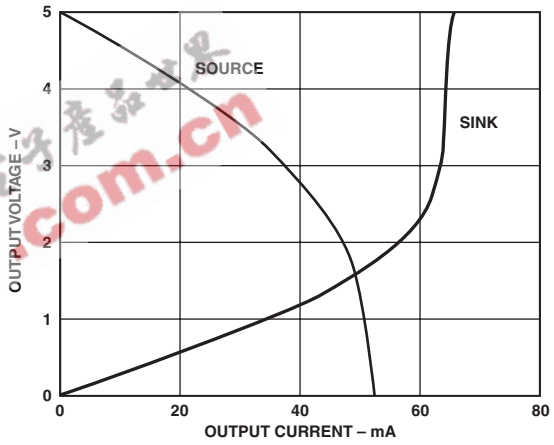
TPC 20. REV1 Hysteresis



TPC 21. Slew Rate vs. Temperature



TPC 22. Settling Time at V_{OUT} vs. Temperature



TPC 23. Output Current Source and Sink

OPERATION

Transfer Function

The transfer function for the ADD8502 is given in the following equations:

1. Digital-to-analog transfer function for DAC A. An output can be derived from Equation 1 as:

$$V_{OUTA} = \left(\frac{V_{DD}}{2}\right)\left(1 + \frac{D_A}{1024}\right) \quad (1)$$

2. Digital-to-analog transfer function for DAC B. An output can be derived from Equation 2 as:

$$V_{OUTB} = \left(\frac{D_B}{1024}\right)\left(\frac{V_{DD}}{2}\right) \quad (2)$$

Where D_A and D_B are decimal equivalents of the binary codes that are loaded to the DAC Register from 0 to 1023.

3. Using any programmed tap point from the 512 resistor string, the system output can be derived from Equation 3:

$$V_{TX} = (V_{OUTA} - V_{OUTB})\left(\frac{T_X}{512}\right) + V_{OUTB} \quad (3)$$

Where T_X is any tap point of the 512 resistor string. It is mask programmable. V_{TX} is the voltage output at any output (VO, ... V4) and will switch between two voltages depending on the mask programmed tap points.

Example: V_{DD} = 5 V, D_A = 1,000, D_B = 100, and T_X = 500.

V_{OUTA} = 4.941 V
V_{OUTB} = 0.244 V
V_{TX} = 4.831 V

Equations 1–3 will provide a theoretical calculation of the outputs. The actual will vary with load, process, and architecture. See Specifications table.

SERIAL INTERFACE

The ADD8502 has a 3-wire serial interface ($\overline{\text{CS-LD}}$, SCK, and D_{IN}). The writing sequence begins by bringing the $\overline{\text{CS-LD}}$ line LOW. Data on the D_{IN} line is clocked into the 16-bit shift register on the rising edge of SCK. The serial clock frequency can be as high as 10 MHz. When the last data bit is clocked in, $\overline{\text{CS-LD}}$ line needs to be brought HIGH to load the DAC registers and the operation mode is dependent upon the control bits.

Input Shift Register

The input shift register is 16 bits wide (see Figure 4). The first four control bits (C3, C2, C1, and C0) are used to set the different operating modes of the device. The next 10 bits are the data bits and the last two bits are "Don't Cares." This composes a full word that is transferred to the DAC register on the rising edge of $\overline{\text{CS-LD}}$.

In a normal write sequence, the $\overline{\text{CS-LD}}$ line is kept LOW for at least 16 rising edges of SCK and then it is brought HIGH to update the DACs. However, if $\overline{\text{CS-LD}}$ is brought HIGH before the 16th rising edge, this acts as an interrupt to the write sequence. The shift register is reset and the write sequence is seen as invalid. Neither an update of the DAC register contents nor a change in the operation mode occurs.

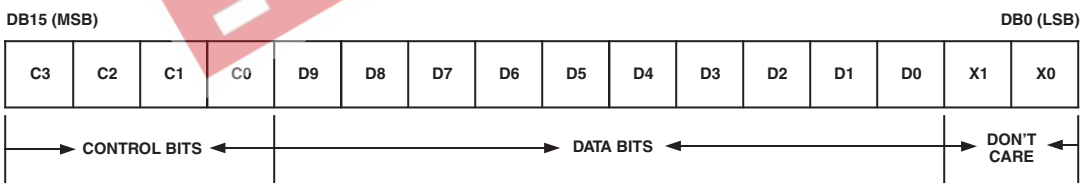


Figure 4. Input Register Contents

Table II. DAC Control Function

Control Code C3	C2	C1	C0	Status	Input Register Status	DAC Register (Sleep/Wake)	Power-Down Status Comments
0	0	0	0	No Change	No Update	No Change	No operation; power-down status unchanged (part stays in Wake or Sleep Mode).
0	0	0	1	Load DAC A	No Update	No Change	Load input Register A with data. DAC outputs unchanged. Power-down status unchanged.
0	0	1	0	Load DAC B	No Update	No Change	Load input Register B with data. DAC outputs unchanged. Power-down status unchanged.
0	0	1	1		Not Used		
0	1	0	0		Not Used		
0	1	0	1		Not Used		
0	1	1	0		Not Used		
0	1	1	1		Not Used		
1	0	0	0	No Change	Update Outputs	Wake	Load both DAC registers with existing contents of input registers. Update DAC outputs. Part wakes up.
1	0	0	1	Load DAC A	Update Outputs	Wake	Load input Register A. Load DAC registers with new contents of input register A and existing contents of Register B. Update DAC outputs. Part wakes up.
1	0	1	0	Load DAC B	Update Outputs	Wake	Load input Register B. Load DAC registers with new contents of input Register B and existing contents of Register A. Update DAC outputs. Part wakes up.
1	0	1	1		Not Used		
1	1	0	0		Not Used		
1	1	0	1	No Change	No Update	Wake	Part wakes up. Input and DAC registers unchanged. DAC outputs reflect existing contents of DAC registers.
1	1	1	0	No Change	No Update	Sleep	Power down the IC, put in into Sleep Mode.
1	1	1	1	Load DACs A, B with Same 10-Bit Code	Update Outputs	Wake	Load both input registers. Load both DAC registers with new contents of input registers. Update DAC outputs. Part wakes up.

Modes of Operation

The ADD8502 has various modes of operation, such as updating both DACs simultaneously or changing the power-down status (Sleep/Wake). These are selected by writing the appropriate 4-bit control code (C0–C3). The details for each mode are summarized in Table II.

Low Power Serial Interface

To reduce the power consumption of the device ever further, the interface only powers up fully when the device is being written to. As soon as the 16-bit control word has been written to the part, the SCK and D_{IN} input buffers are powered down. They only power up again following a falling edge of $\overline{CS\text{-}LD}$.

Double-Buffered Interface

The ADD8502 has double-buffered interfaces consisting of two banks of registers: input and DAC. The input register is connected directly to the input shift register, and the digital code is transferred to the relevant input register on completion of a valid write sequence. The DAC register contains the digital code used by the resistor string.

Access to the DAC register is controlled by the control codes, C0 to C3. The user can update both DACs simultaneously as well as individually. It depends on the selected control codes to update individual output or both outputs simultaneously.

Initial Power-Up Condition

The ADD8502 has preset DAC conditions when its initially powered on. The DACs are loaded with 1110 1011 11 for the upper DAC and 0000 1010 00 for the lower DAC. The part is powered up in a normal operation mode (Wake Status).

Power-Down Modes

The ADD8502 has two shutdown modes. One mode is to fully shut down the device using $\overline{PSK}$ or the digital serial control code, and the other mode is to shut down V1 to V3 buffers using GS1 and GS2. See Table III for the priority of the shutdown control functions.

The ADD8502 will have a quiescent current less than 1 μA when it is fully shut down and all output buffers are switched to a high impedance state. The only active circuitries are the digital logics and the latches for the serial control. When the device is brought back from Sleep Mode to normal operation, it will use the last serial word to update the DACs or a new control code or data if any was loaded when the part was in Sleep Mode; i.e., the contents of the input register, DAC register, and power-down status shown in Table II is retained as long as V_{DD} and V_L are on.

The second power save mode (mid 3 buffers are shut down) is using GS1 and GS2. In a condition where both GS1 and GS2 logics are HIGH, the output buffers (V1, V2, and V3) are shut down and switched into a high impedance state.

Table III. Shutdown Control Function

$\overline{PSK}$	Serial Control	GS1	GS2	Operation Mode
H	Wake	L	L	Normal Operation
H	Wake	L	H	Normal Operation
H	Wake	H	L	Normal Operation
H	Wake	H	H	Mid 3 Buffers are Shutdown
H	Sleep	X	X	Full Shutdown
L	X	X	X	Full Shutdown

X = Don't Care

V_{COM} Logic

V_{COM} operation is described in Table IV. The V_{COM} logic is always active and its logic inputs are CM, REV1, and CV4. When CM is LOW, COM is connected to COM_M. When CM is HIGH, COM is determined by the logic input of REV1. If REV1 is HIGH, COM is connected to V_{DD}. When REV1 is LOW, COM is connected to GND.

CV4 controls the V4 output. If CV4 goes LOW, V4 is connected to COM and A4 is shut down with its output in a Hi-Z state. When CV4 is HIGH, the switch connecting V4 to COM is open and A4 is in normal operation mode.

Table IV. V_{COM} Logic Control

Inputs			Outputs	
CM	REV1	CV4	V_{COM}	V4
L	X	L	COM_M	COM
L	X	H	COM_M	A4
H	L	L	GND	COM
H	H	L	V_{DD}	COM
H	L	H	GND	A4
H	H	H	V_{DD}	A4

X = Don't Care

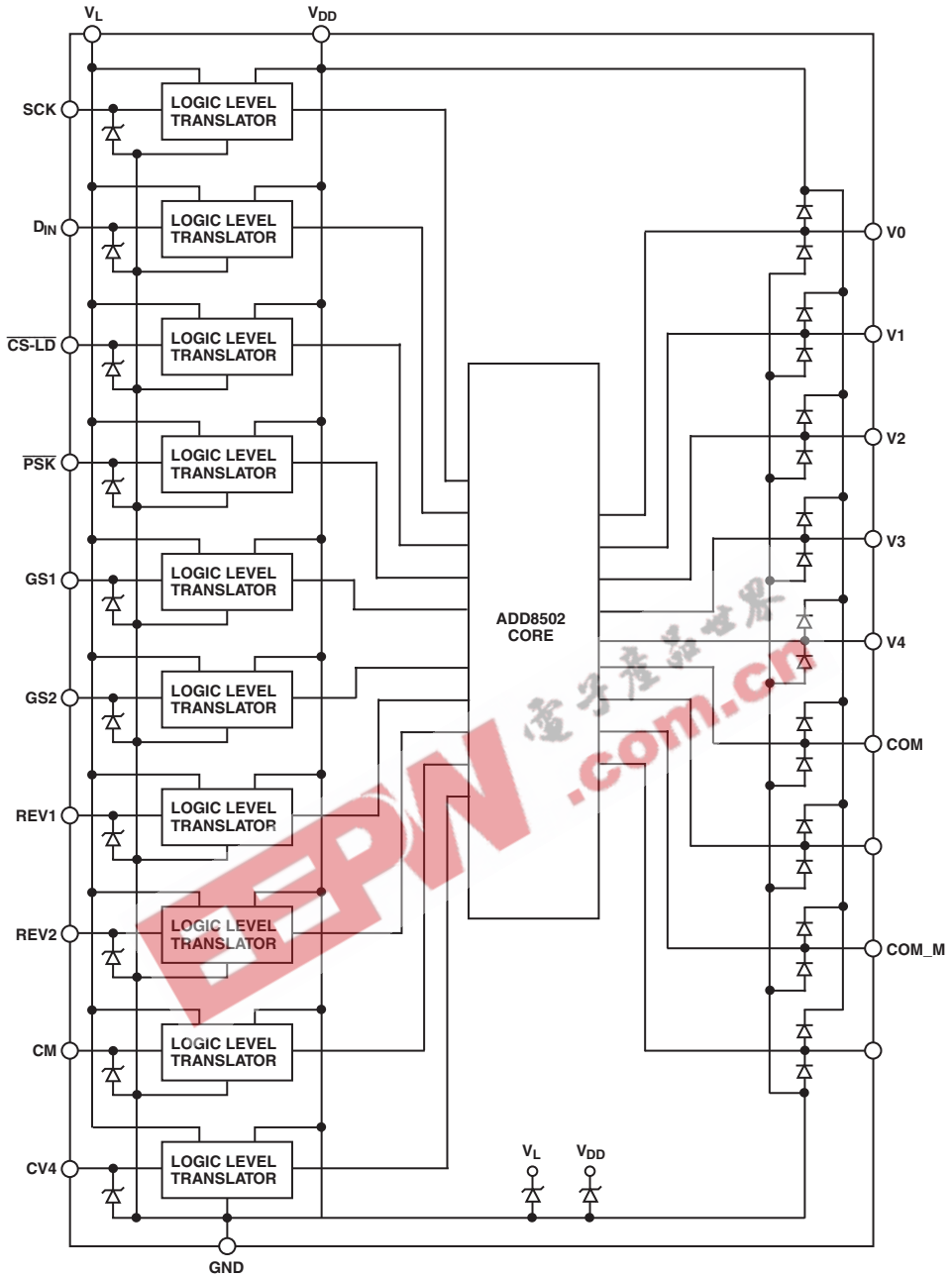


Figure 5. CST ESD and Logic Level Translation Scheme

ADD8502 Description

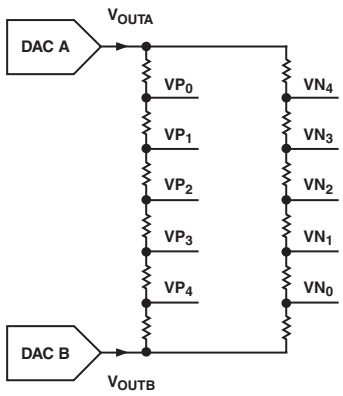
- The ADD8502 uses logic level translators to convert external logic levels to levels suitable for use in the ADD8502 core.
- The logic level translators are intended to be powered from the same supply voltage as is used to power the external logic driving the ADD8502.
- V_{DD} may be powered down while normal voltages are present on the V_L and logic input pins.
- V_{DD} and V_L are independent and can be in the range 0 V to 5.5 V.
- No damage to the digital inputs will occur with applied voltages up to 7 V (see Absolute Maximum Ratings section of data sheet).
- No current will flow between V_{DD} and V_L under normal operating conditions.
- Logic voltages can be present on the logic input pins even if V_L is powered down. Inputs are limited by max supply rating of 7 V.
- Digital input pins have ESD protection connected to GND.
- All other input and output pins have ESD protection connected to GND and V_{DD}.

ADD8502-000 MASK OPTION

Table V. Default Power-Up Conditions

DAC Setpoints (0 ≤ D ≤ 1023)			
	Decimal Code	**Voltage**	**Unit**
Upper DAC	943	4.8022	V
Lower DAC	40	0.0977	V
Resistor Tap Points (0 ≤ X ≤ 512)			
	Tap Point	**Voltage**	**Unit**
VP0	450	4.2325	V
VP1	271	2.5878	V
VP2	203	1.9630	V
VP3	137	1.3565	V
VP4	3	0.1252	V
VN0	31	0.3825	V
VN1	215	2.0732	V
VN2	290	2.7624	V
VN3	367	3.4699	V
VN4	509	4.7747	V

Supply voltage = 5 V



Figrue 6. Tap Point References

Tap point voltages can be derived from the following equation:

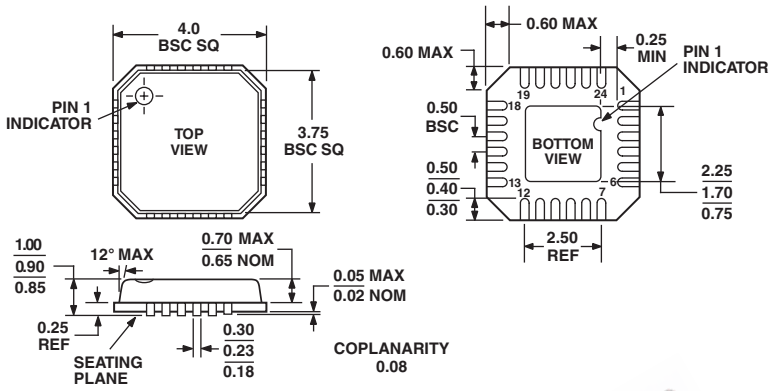
$$Vx = V_{OUTB} + \frac{X}{512}\left[V_{OUTA} - V_{OUTB}\right]$$

Where V_{OUTA} and V_{OUTB} can be derived from the transfer functions under the Operation Section of the datasheet.

The ADD8502 uses a single resistor string consisting of 512 individual elements. Both sets of reference voltages (V_{P0}–V_{P4}, V_{N0}–V_{N4}) are generated from this single string. Two separate resistor networks are shown to demonstrate the tap points, which are changeable by mask option and completely independent of each other.

OUTLINE DIMENSIONS

24-Lead Frame Chip Scale Package [LFCSP]
4x4 mm Body
(CP-24)



COMPLIANT TO JEDEC STANDARDS MO-220-VGGD-2