Ultralow Distortion High Speed Amplifiers

AD8007/AD8008

FEATURES

Extremely Low Distortion
- **Second Harmonic**
  - **–88 dBc @ 5 MHz**
  - **–83 dBc @ 20 MHz (AD8007)**
  - **–77 dBc @ 20 MHz (AD8008)**
- **Third Harmonic**
  - **–101 dBc @ 5 MHz**
  - **–92 dBc @ 20 MHz (AD8007)**
  - **–98 dBc @ 20 MHz (AD8008)**

High Speed
- **650 MHz, –3 dB Bandwidth (G = +1)**
- **1000 V/μs Slew Rate**

Low Noise
- **2.7 nV/√Hz Input Voltage Noise**
- **22.5 pA/√Hz Input Inverting Current Noise**

Low Power
- **9 mA/Amplifier Typ Supply Current**

Wide Supply Voltage Range
- **5 V to 12 V**

0.5 mV Typical Input Offset Voltage

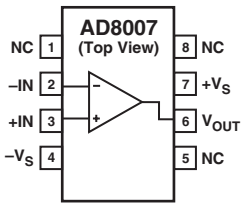
Small Packaging
- **SOIC-8, MSOP, and SC70 Packages Available**

APPLICATIONS

Instrumentation
IF and Baseband Amplifiers
Filters
A/D Drivers
DAC Buffers

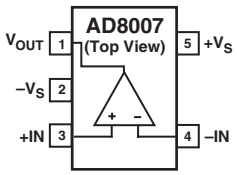
CONNECTION DIAGRAMS

SOIC (RN-8)

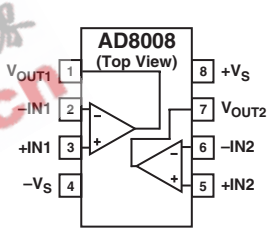


NC = NO CONNECT

SC70 (KS-5)



SOIC (RN) and MSOP (RM)



GENERAL DESCRIPTION

The AD8007 (single) and AD8008 (dual) are high performance current feedback amplifiers with ultralow distortion and noise. Unlike other high performance amplifiers, the low price and low quiescent current allow these amplifiers to be used in a wide range of applications. ADI's proprietary second generation eXtra-Fast Complementary Bipolar (XFCB) process enables such high performance amplifiers with low power consumption.

The AD8007/AD8008 have 650 MHz bandwidth, 2.7 nV/√Hz voltage noise, –83 dB SFDR @ 20 MHz (AD8007), and –77 dBc SFDR @ 20 MHz (AD8008).

With the wide supply voltage range (5 V to 12 V) and wide bandwidth, the AD8007/AD8008 are designed to work in a variety of applications. The AD8007/AD8008 amplifiers have a low power supply current of 9 mA/amplifier.

The AD8007 is available in a tiny SC70 package as well as a standard 8-lead SOIC. The dual AD8008 is available in both 8-lead SOIC and 8-lead MSOP packages. These amplifiers are rated to work over the industrial temperature range of –40°C to +85°C.

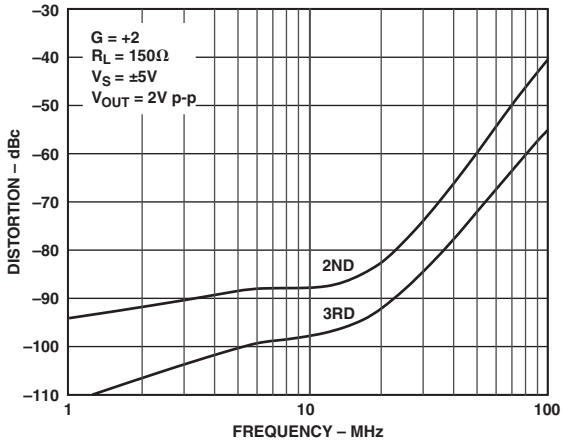


Figure 1. AD8007 Second and Third Harmonic Distortion vs. Frequency

REV. C

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AD8007/AD8008–SPECIFICATIONS

$V_S = \pm 5$ V (@ T_A = 25°C, R_S = 200 Ω, R_L = 150 Ω, R_F = 499 Ω, Gain = +2, unless otherwise noted.)

Parameter	Conditions	AD8007/AD8008 Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Bandwidth	G = +1, V_O = 0.2 V p-p, R_L = 1 kΩ	540	650		MHz
	G = +1, V_O = 0.2 V p-p, R_L = 150 Ω	250	500		MHz
	G = +2, V_O = 0.2 V p-p, R_L = 150 Ω	180	230		MHz
	G = +1, V_O = 2 V p-p, R_L = 1 kΩ	200	235		MHz
Bandwidth for 0.1 dB Flatness	V_O = 0.2 V p-p, G = +2, R_L = 150 Ω	50	90		MHz
Overdrive Recovery Time	±2.5 V Input Step, G = +2, R_L = 1 kΩ		30		ns
Slew Rate	G = +1, V_O = 2 V Step	900	1000		V/µs
Settling Time to 0.1%	G = +2, V_O = 2 V Step		18		ns
Settling Time to 0.01%	G = +2, V_O = 2 V Step		35		ns
NOISE/HARMONIC PERFORMANCE					
Second Harmonic	f_C = 5 MHz, V_O = 2 V p-p		–88		dBc
	f_C = 20 MHz, V_O = 2 V p-p		–83/–77		dBc
Third Harmonic	f_C = 5 MHz, V_O = 2 V p-p		–101		dBc
	f_C = 20 MHz, V_O = 2 V p-p		–92/–98		dBc
IMD	f_C = 19.5 MHz to 20.5 MHz, R_L = 1 kΩ, V_O = 2 V p-p		–77		dBc
Third Order Intercept	f_C = 5 MHz, R_L = 1 kΩ		43.0/42.5		dBm
	f_C = 20 MHz, R_L = 1 kΩ		42.5		dBm
Crosstalk (AD8008)	f = 5 MHz, G = +2		–68		dB
Input Voltage Noise	f = 100 kHz		2.7		nV/√Hz
Input Current Noise	–Input, f = 100 kHz		22.5		pA/√Hz
	+Input, f = 100 kHz		2		pA/√Hz
Differential Gain Error	NTSC, G = +2, R_L = 150 Ω		0.015		%
Differential Phase Error	NTSC, G = +2, R_L = 150 Ω		0.010		Degree
DC PERFORMANCE					
Input Offset Voltage			0.5	4	mV
Input Offset Voltage Drift			3		µV/°C
Input Bias Current	+Input		4	8	µA
	–Input		0.4	6	µA
Input Bias Current Drift	+Input		16		nA/°C
	–Input		9		nA/°C
Transimpedance	V_O = ±2.5 V, R_L = 1 kΩ	1.0	1.5		MΩ
	R_L = 150 Ω	0.4	0.8		MΩ
INPUT CHARACTERISTICS					
Input Resistance	+Input		4		MΩ
Input Capacitance	+Input		1		pF
Input Common-Mode Voltage Range			–3.9 to +3.9		V
Common-Mode Rejection Ratio	V_{CM} = ±2.5 V	56	59		dB
OUTPUT CHARACTERISTICS					
Output Saturation Voltage	$V_{CC} - V_{OH}$, $V_{OL} - V_{EE}$, R_L = 1 kΩ		1.1	1.2	V
Short Circuit Current, Source			130		mA
Short Circuit Current, Sink			90		mA
Capacitive Load Drive	30% Overshoot		8		pF
POWER SUPPLY					
Operating Range		5		12	V
Quiescent Current per Amplifier			9	10.2	mA
Power Supply Rejection Ratio					
+PSRR		59	64		dB
–PSRR		59	65		dB

V_S = +5 V (@ T_A = 25°C, R_S = 200 Ω, R_L = 150 Ω, R_F = 499 Ω, Gain = +2, unless otherwise noted.)

Parameter	Conditions	AD8007/AD8008 Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Bandwidth	G = +1, V_O = 0.2 V p-p, R_L = 1 kΩ	520	580		MHz
	G = +1, V_O = 0.2 V p-p, R_L = 150 Ω	350	490		MHz
	G = +2, V_O = 0.2 V p-p, R_L = 150 Ω	190	260		MHz
	G = +1, V_O = 1 V p-p, R_L = 1 kΩ	270	320		MHz
Bandwidth for 0.1 dB Flatness	Vo = 0.2 V p-p, G = +2, R_L = 150 Ω	72	120		MHz
Overdrive Recovery Time	2.5 V Input Step, G = +2, R_L = 1 kΩ		30		ns
Slew Rate	G = +1, V_O = 2 V Step	665	740		V/µs
Settling Time to 0.1%	G = +2, V_O = 2 V Step		18		ns
Settling Time to 0.01%	G = +2, V_O = 2 V Step		35		ns
NOISE/HARMONIC PERFORMANCE					
Second Harmonic	f_C = 5 MHz, V_O = 1 V p-p		–96/–95		dBc
	f_C = 20 MHz, V_O = 1 V p-p		–83/–80		dBc
Third Harmonic	f_C = 5 MHz, V_O = 1 V p-p		–100		dBc
	f_C = 20 MHz, V_O = 1 V p-p		–85/–88		dBc
IMD	f_C = 19.5 MHz to 20.5 MHz, R_L = 1 kΩ, V_O = 1 V p-p		–89/–87		dBc
Third Order Intercept	f_C = 5 MHz, R_L = 1 kΩ		43.0		dBm
	f_C = 20 MHz, R_L = 1 kΩ		42.5/41.5		dBm
Crosstalk (AD8008)	Output to Output f = 5 MHz, G = +2		–68		dB
Input Voltage Noise	f = 100 kHz		2.7		nV/√Hz
Input Current Noise	–Input, f = 100 kHz		22.5		pA/√Hz
	+Input, f = 100 kHz		2		pA/√Hz
DC PERFORMANCE					
Input Offset Voltage			0.5	4	mV
Input Offset Voltage Drift			3		µV/°C
Input Bias Current	+Input		4	8	µA
	–Input		0.7	6	µA
Input Bias Current Drift	+Input		15		nA/°C
	–Input		8		nA/°C
Transimpedance	V_O = 1.5 V to 3.5 V, R_L = 1 kΩ	0.5	1.3		MΩ
	R_L = 150 Ω	0.4	0.6		MΩ
INPUT CHARACTERISTICS					
Input Resistance	+Input		4		MΩ
Input Capacitance	+Input		1		pF
Input Common-Mode Voltage Range			1.1 to 3.9		V
Common-Mode Rejection Ratio	V_{CM} = 1.75 V to 3.25 V	54	56		dB
OUTPUT CHARACTERISTICS					
Output Saturation Voltage	$V_{CC} - V_{OH}$, $V_{OL} - V_{EE}$, R_L = 1 kΩ		1.05	1.15	V
Short Circuit Current, Source			70		mA
Short Circuit Current, Sink			50		mA
Capacitive Load Drive	30% Overshoot		8		pF
POWER SUPPLY					
Operating Range		5		12	V
Quiescent Current per Amplifier			8.1	9	mA
Power Supply Rejection Ratio					
+PSRR		59	62		dB
–PSRR		59	63		dB

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage	12.6 V
Power Dissipation	See Figure 2
Common-Mode Input Voltage	$\pm V_S$
Differential Input Voltage	±1.0 V
Output Short Circuit Duration	See Figure 2
Storage Temperature	–65°C to +125°C
Operating Temperature Range	–40°C to +85°C
Lead Temperature Range (soldering 10 sec)	300°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation in the AD8007/AD8008 packages is limited by the associated rise in junction temperature (T_J) on the die. The plastic encapsulating the die will locally reach the junction temperature. At approximately 150°C, which is the glass transition temperature, the plastic will change its properties. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the AD8007/AD8008. Exceeding a junction temperature of 175°C for an extended period of time can result in changes in the silicon devices, potentially causing failure.

The still-air thermal properties of the package and PCB (θ_{JA}), ambient temperature (T_A), and the total power dissipated in the package (P_D) determine the junction temperature of the die. The junction temperature can be calculated as follows:

$$T_J = T_A + (P_D \times \theta_{JA})$$

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). Assuming the load (R_L) is referenced to midsupply, the total drive power is $V_S/2 \times I_{OUT}$, some of which is dissipated in the package and some in the load ($V_{OUT} \times I_{OUT}$). The difference between the total drive power and the load power is the drive power dissipated in the package.

P_D = quiescent power + (total drive power – load power):

$$P_D = (V_S \times I_S) + \left(\frac{V_S}{2} \times \frac{V_{OUT}}{R_L}\right) - \frac{V_{OUT}^2}{R_L}$$

RMS output voltages should be considered. If R_L is referenced to V_S, as in single-supply operation, then the total drive power is $V_S \times I_{OUT}$.

If the rms signal levels are indeterminate, then consider the worst case, when $V_{OUT} = V_S/4$ for R_L to midsupply:

$$P_D = (V_S \times I_S) + \frac{\left(\frac{V_S}{4}\right)^2}{R_L}$$

In single-supply operation, with R_L referenced to V_S, worst case is:

$$V_{OUT} = \frac{V_S}{2}$$

Airflow will increase heat dissipation, effectively reducing θ_{JA}. Also, more metal directly in contact with the package leads from metal traces, through holes, ground, and power planes will reduce the θ_{JA}. Care must be taken to minimize parasitic capacitances at the input leads of high speed op amps as discussed in the board layout section.

Figure 2 shows the maximum safe power dissipation in the package versus the ambient temperature for the SOIC-8 (125°C/W), MSOP (150°C/W), and SC70 (210°C/W) packages on a JEDEC standard 4-layer board. θ_{JA} values are approximations.

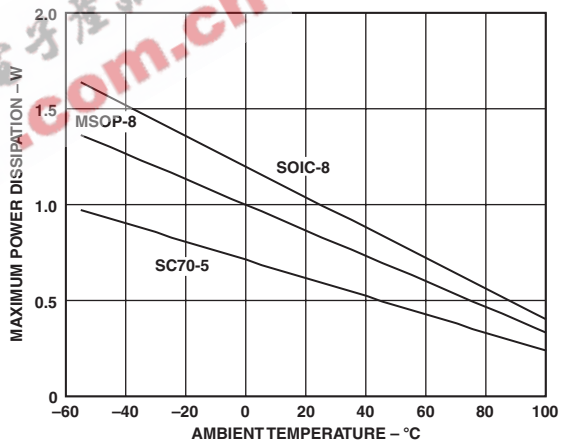


Figure 2. Maximum Power Dissipation vs. Temperature for a 4-Layer Board

OUTPUT SHORT CIRCUIT

Shorting the output to ground or drawing excessive current for the AD8007/AD8008 will likely cause catastrophic failure.

CAUTION

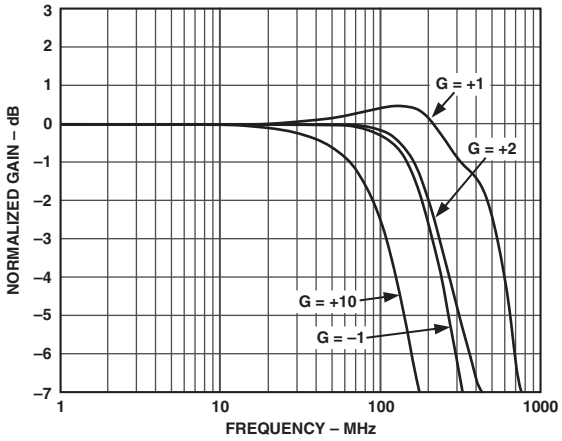
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8007/AD8008 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ORDERING GUIDE

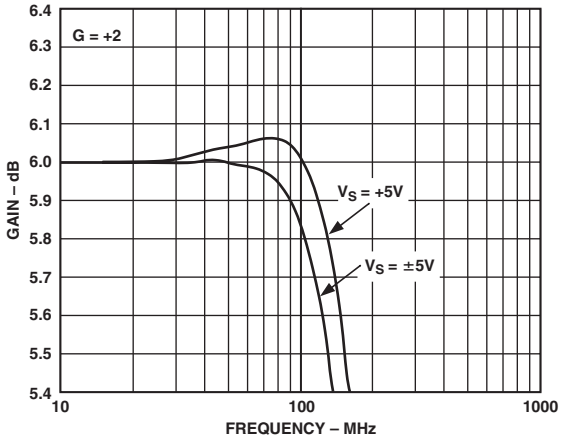
Model	Temperature Range	Package Description	Package Outline	Branding Information
AD8007AR	–40°C to +85°C	8-Lead SOIC	RN-8	
AD8007AR-REEL	–40°C to +85°C	8-Lead SOIC	RN-8	
AD8007AR-REEL7	–40°C to +85°C	8-Lead SOIC	RN-8	
AD8007AKS-REEL	–40°C to +85°C	5-Lead SC70	KS-5	HTA
AD8007AKS-REEL7	–40°C to +85°C	5-Lead SC70	KS-5	HTA
AD8008AR	–40°C to +85°C	8-Lead SOIC	RN-8	
AD8008AR-REEL7	–40°C to +85°C	8-Lead SOIC	RN-8	
AD8008AR-REEL	–40°C to +85°C	8-Lead SOIC	RN-8	
AD8008ARM-REEL	–40°C to +85°C	8-Lead MSOP	RM-8	H2B
AD8008ARM-REEL7	–40°C to +85°C	8-Lead MSOP	RM-8	H2B

AD8007/AD8008–Typical Performance Characteristics

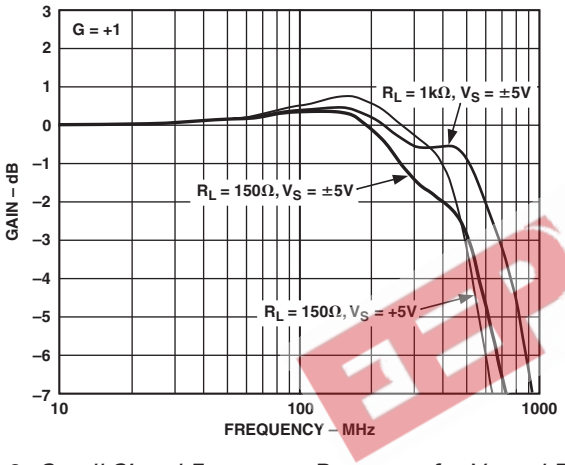
(V_S = ±5 V, R_L = 150 Ω, R_S = 200 Ω, R_F = 499 Ω, unless otherwise noted.)



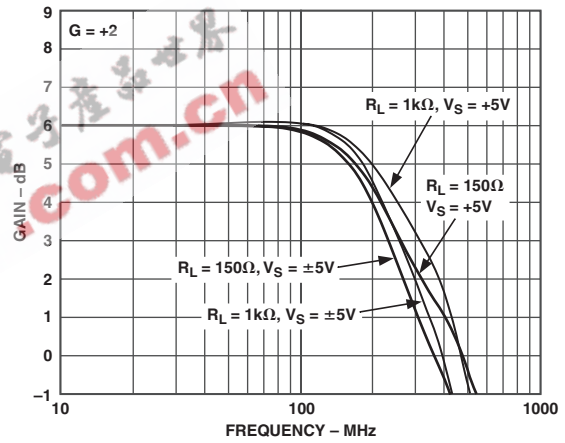
TPC 1. Small Signal Frequency Response for Various Gains



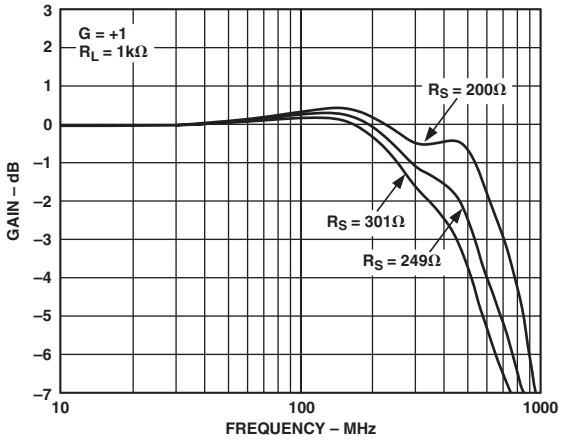
TPC 4. 0.1 dB Gain Flatness; V_S = +5, ±5 V



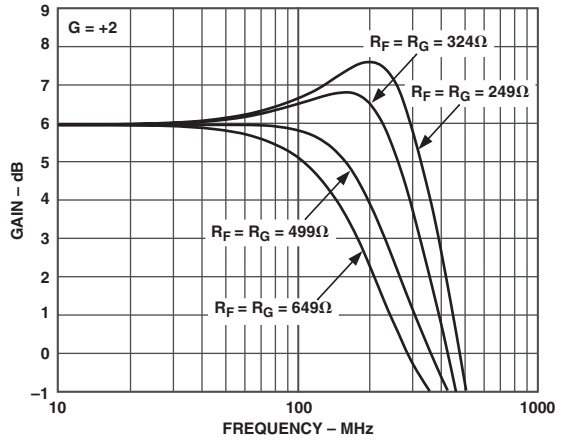
TPC 2. Small Signal Frequency Response for V_S and R_{LOAD}



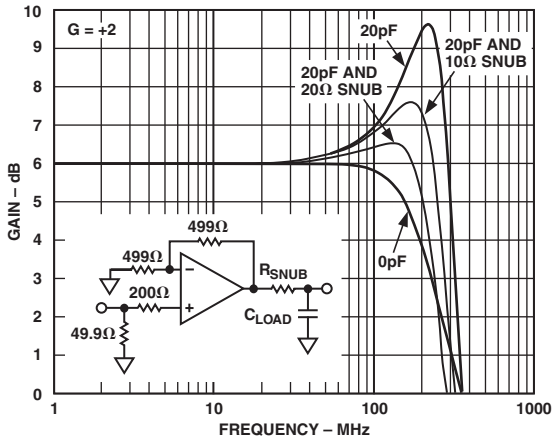
TPC 5. Small Signal Frequency Response for V_S and R_{LOAD}



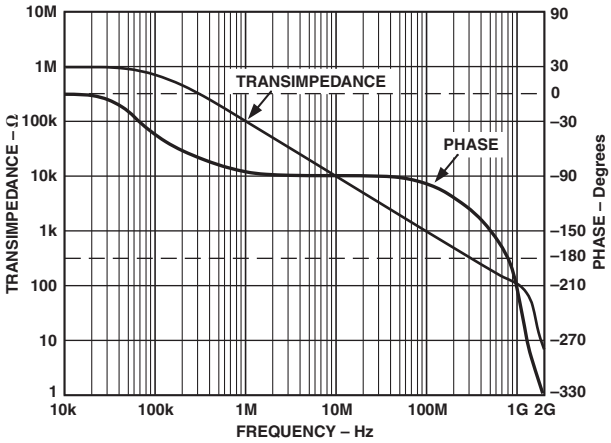
TPC 3. Small Signal Frequency Response for Various R_S Values



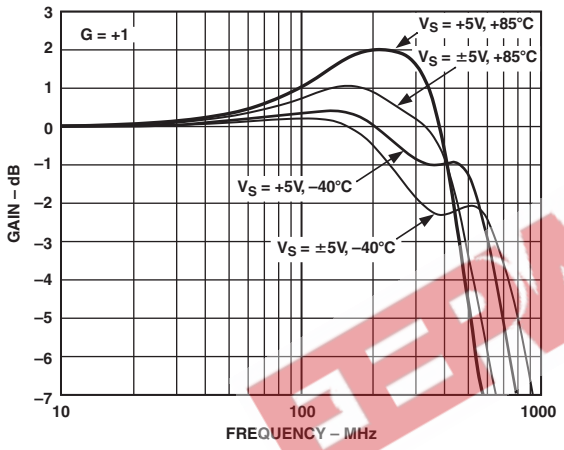
TPC 6. Small Signal Frequency Response for Various Feedback Resistors, $R_F = R_G$



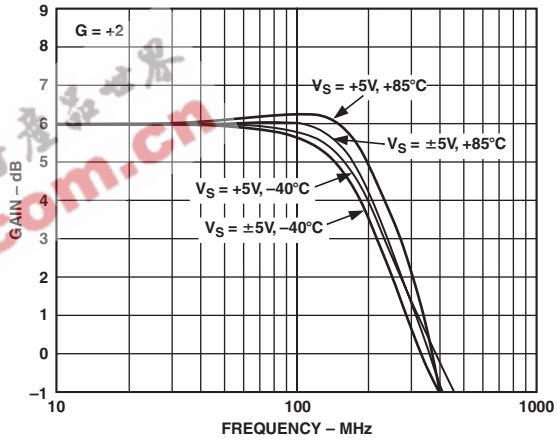
TPC 7. Small Signal Frequency Response for Capacitive Load and Snub Resistor



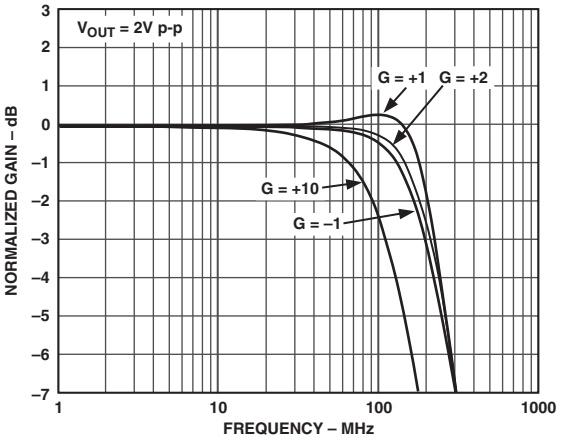
TPC 10. Transimpedance and Phase vs. Frequency



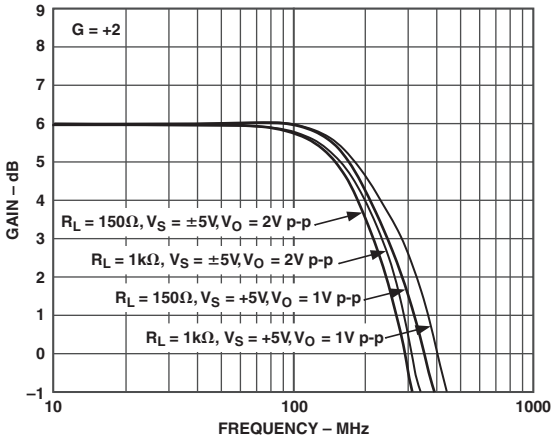
TPC 8. Small Signal Frequency Response over Temperature, V_S = +5 V, ±5 V



TPC 11. Small Signal Frequency Response over Temperature, V_S = +5 V, ±5 V

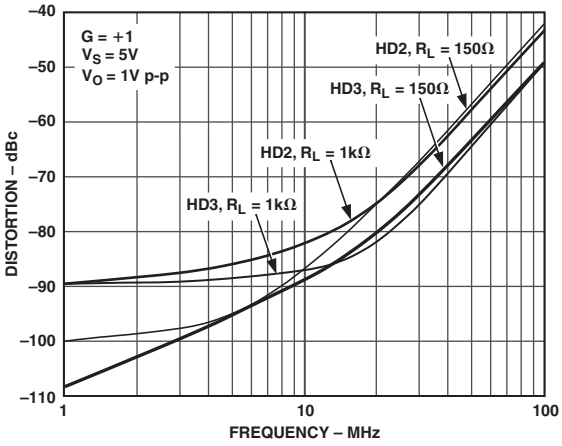


TPC 9. Large Signal Frequency Response for Various Gains

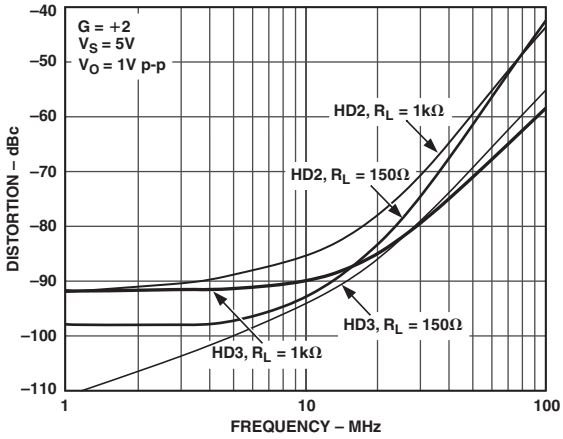


TPC 12. Large Signal Frequency Response for V_S and R_{LOAD}

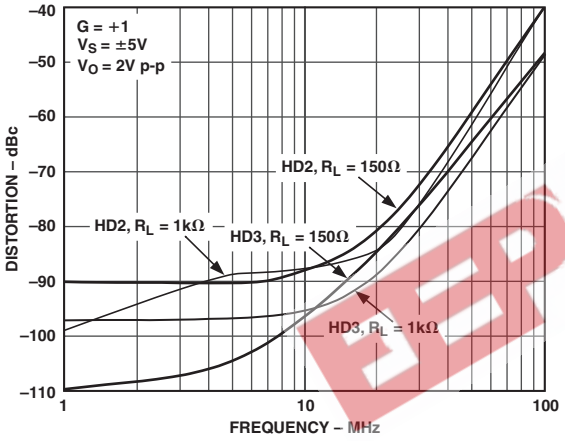
(V_S = ±5 V, R_L = 150 Ω, R_S = 200 Ω, R_F = 499 Ω, unless otherwise noted.)



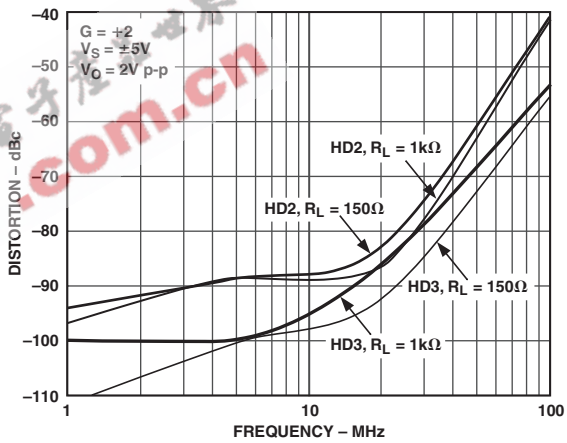
TPC 13. AD8007 Second and Third Harmonic Distortion vs. Frequency and R_L



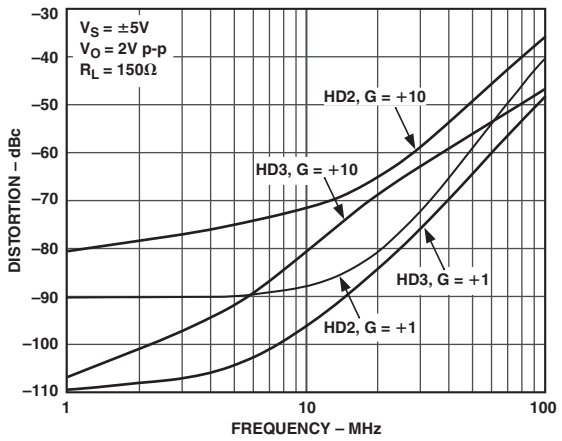
TPC 16. AD8007 Second and Third Harmonic Distortion vs. Frequency and R_L



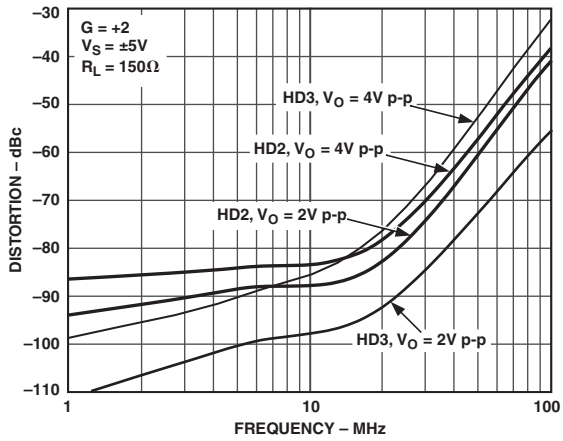
TPC 14. AD8007 Second and Third Harmonic Distortion vs. Frequency and R_L



TPC 17. AD8007 Second and Third Harmonic Distortion vs. Frequency and R_L

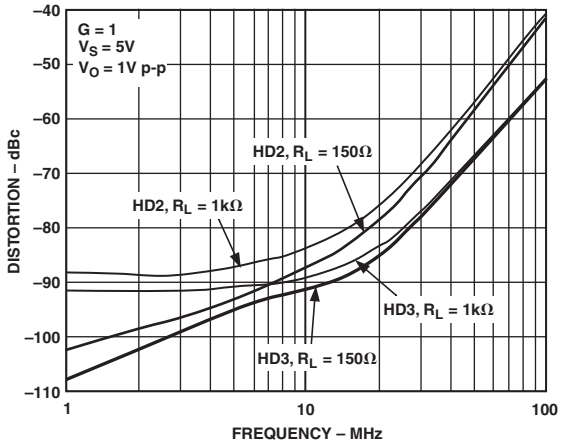


TPC 15. AD8007 Second and Third Harmonic Distortion vs. Frequency and Gain

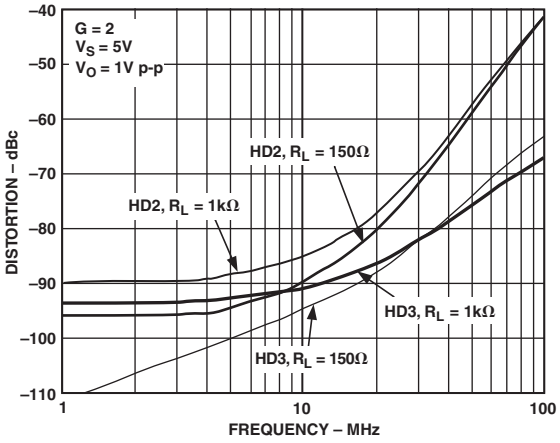


TPC 18. AD8007 Second and Third Harmonic Distortion vs. Frequency and V_{OUT}

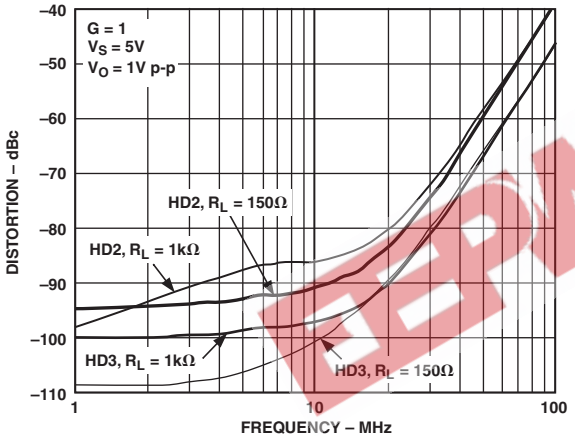
(V_S = ±5 V, R_S = 200 Ω, R_F = 499 Ω, R_L = 150 Ω, @25°C, unless otherwise noted.)



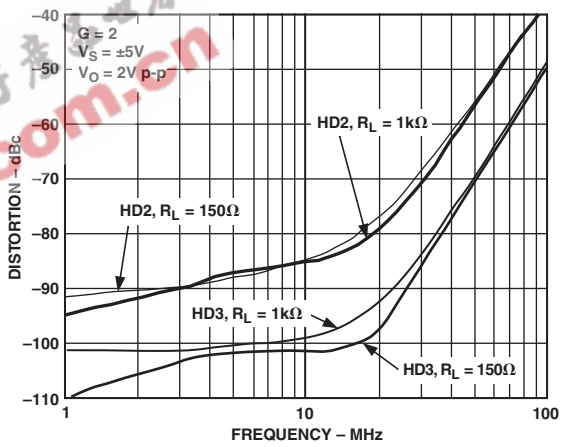
TPC 19. AD8008 Second and Third Harmonic Distortion vs. Frequency and R_L



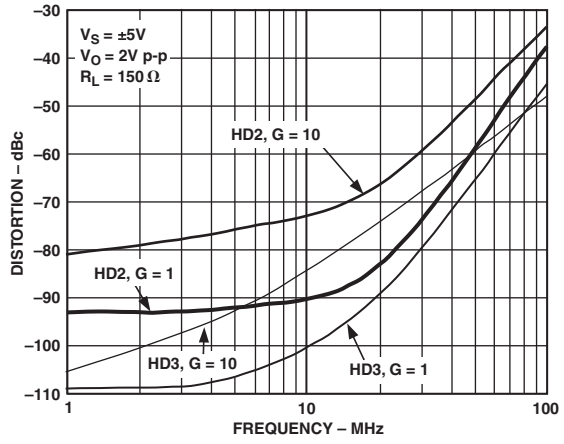
TPC 22. AD8008 Second and Third Harmonic Distortion vs. Frequency and R_L



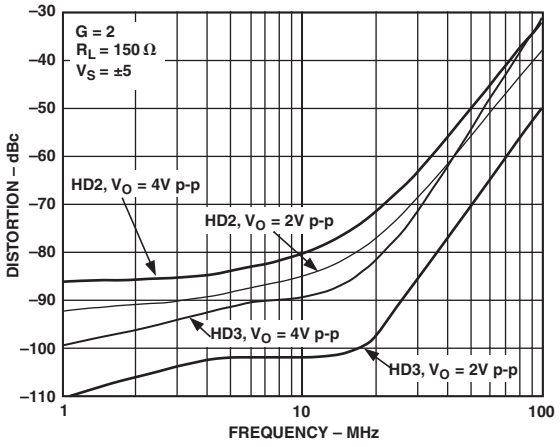
TPC 20. AD8008 Second and Third Harmonic Distortion vs. Frequency and R_L



TPC 23. AD8008 Second and Third Harmonic Distortion vs. Frequency and R_L

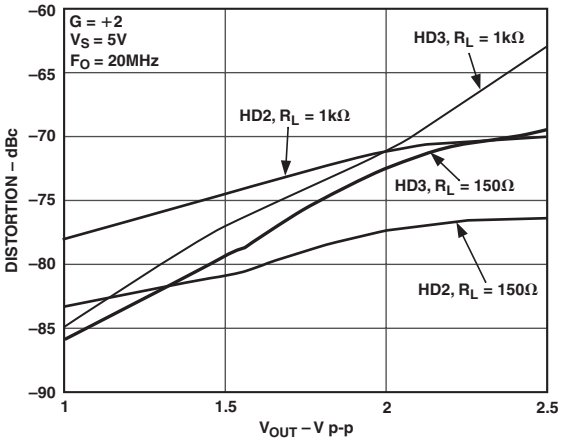


TPC 21. AD8008 Second and Third Harmonic Distortion vs. Frequency and Gain

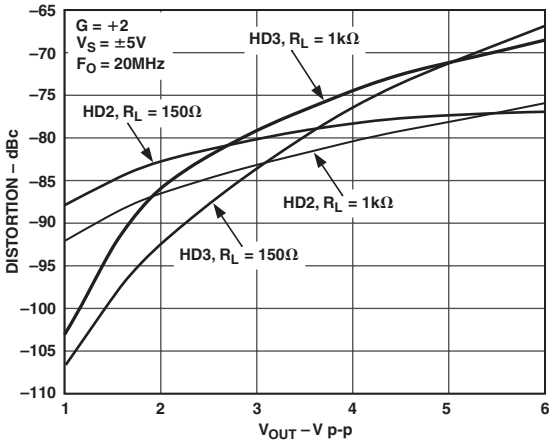


TPC 24. AD8008 Second and Third Harmonic Distortion vs. Frequency and V_{OUT}

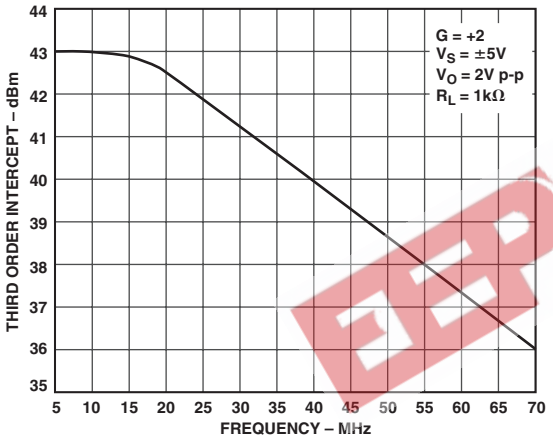
(V_S = ±5 V, R_S = 200 Ω, R_F = 499 Ω, R_L = 150 Ω, @25°C unless otherwise noted.)



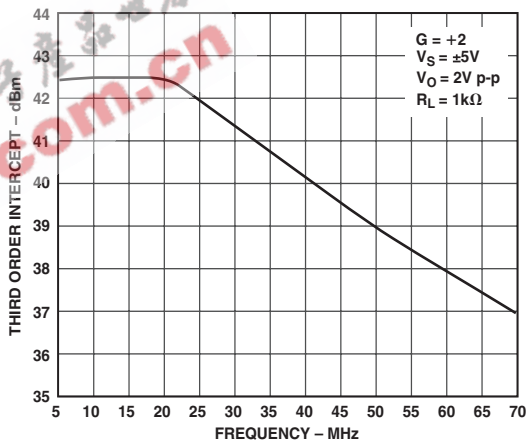
TPC 25. AD8007 Second and Third Harmonic Distortion vs. V_{OUT} and R_L



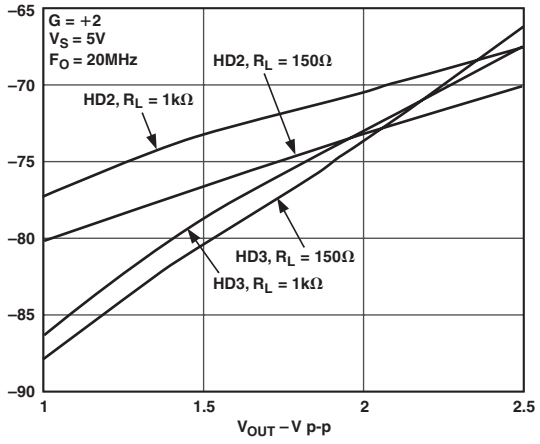
TPC 28. AD8007 Second and Third Harmonic Distortion vs. V_{OUT} and R_L



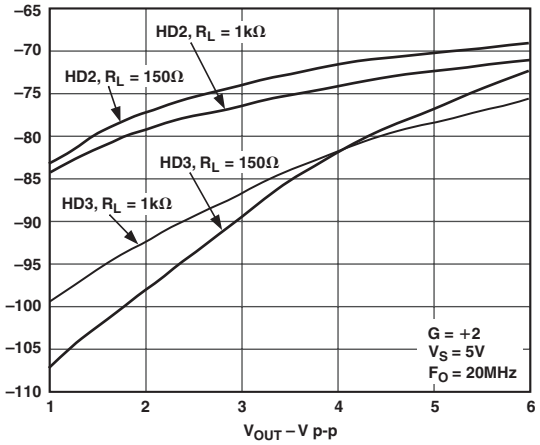
TPC 26. AD8007 Third Order Intercept vs. Frequency



TPC 29. AD8008 Third Order Intercept vs. Frequency

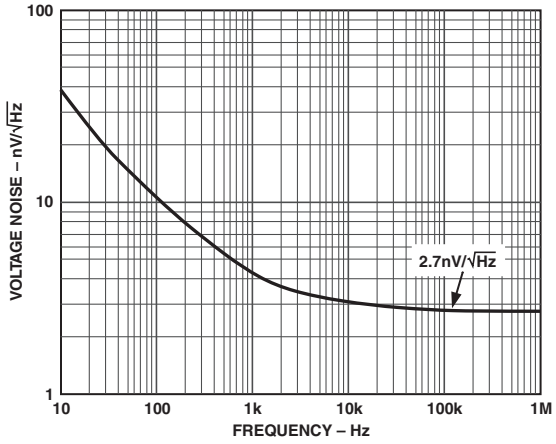


TPC 27. AD8008 Second and Third Harmonic Distortion vs. V_{OUT} and R_L

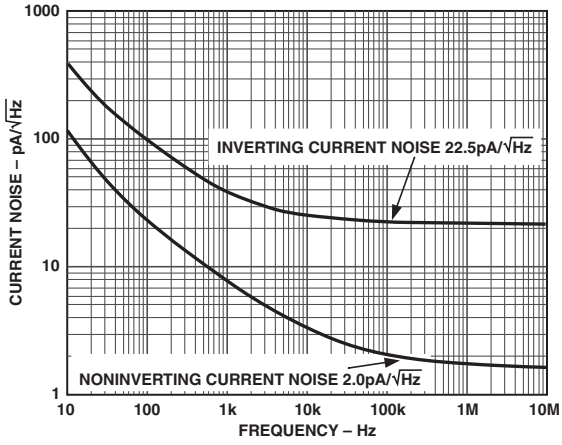


TPC 30. AD8008 Second and Third Harmonic Distortion vs. V_{OUT} and R_L

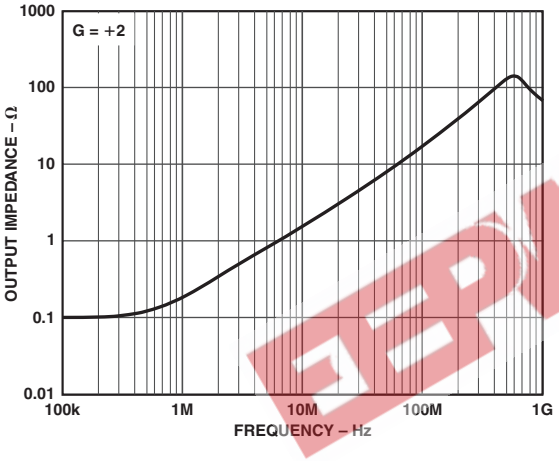
(V_S = ±5 V, R_L = 150 Ω, R_S = 200 Ω, R_F = 499 Ω, unless otherwise noted.)



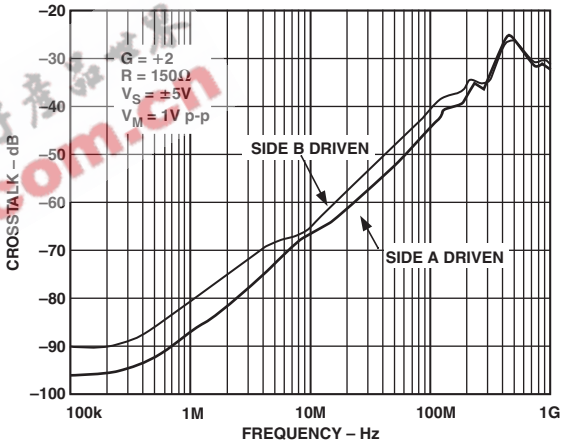
TPC 31. Input Voltage Noise vs. Frequency



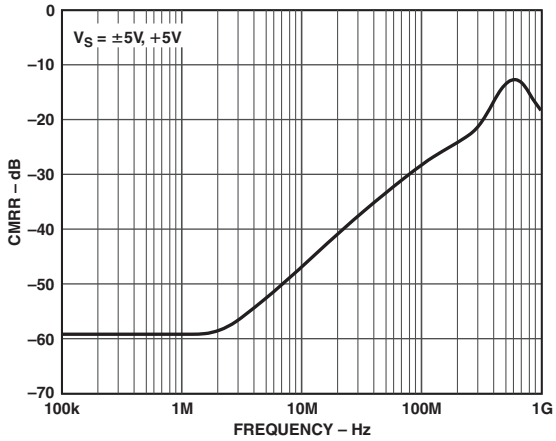
TPC 34. Input Current Noise vs. Frequency



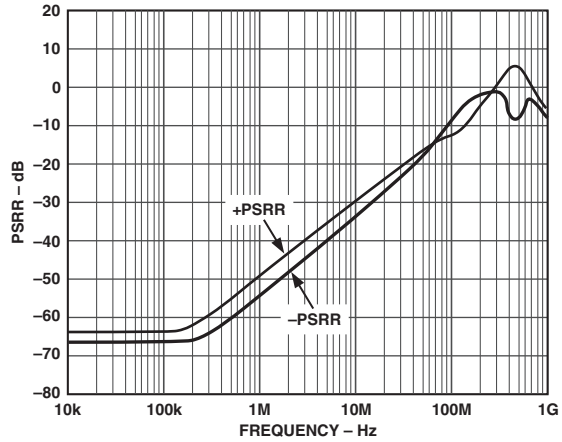
TPC 32. Output Impedance vs. Frequency



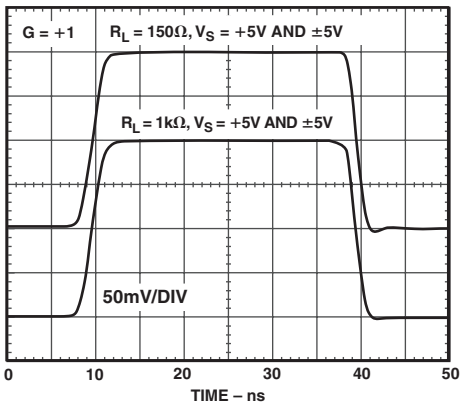
TPC 35. AD8008 Crosstalk vs. Frequency (Output to Output)



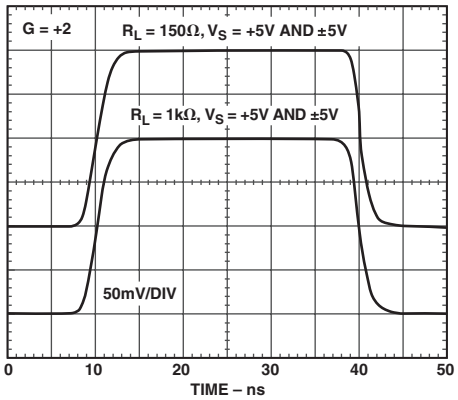
TPC 33. CMRR vs. Frequency



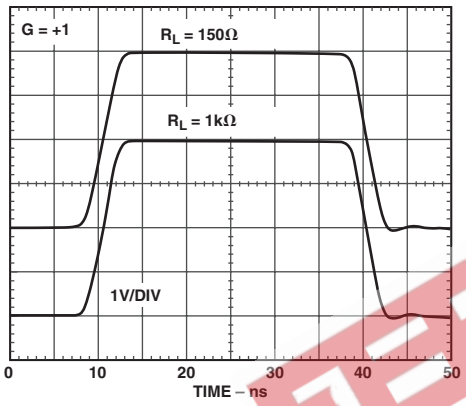
TPC 36. PSRR vs. Frequency



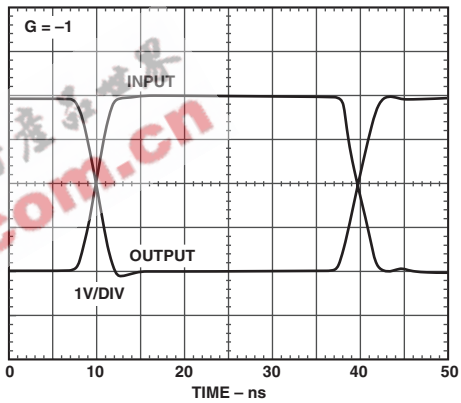
TPC 37. Small Signal Transient Response for R_L = 150 Ω, 1 kΩ and V_S = +5 V, ±5 V



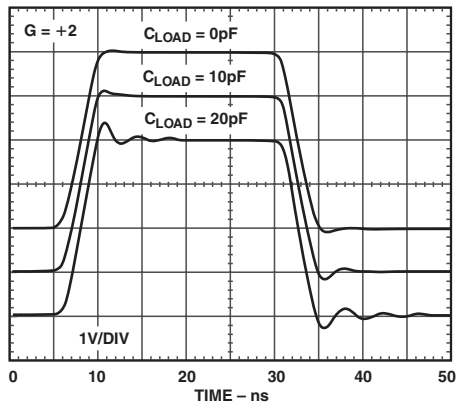
TPC 40. Small Signal Transient Response for R_L = 150 Ω, 1 kΩ and V_S = +5 V, ±5 V



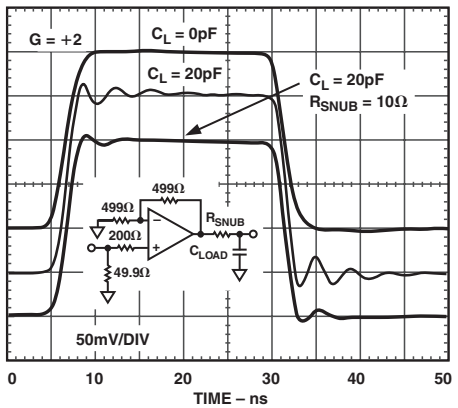
TPC 38. Large Signal Transient Response for R_L = 150 Ω, 1 kΩ



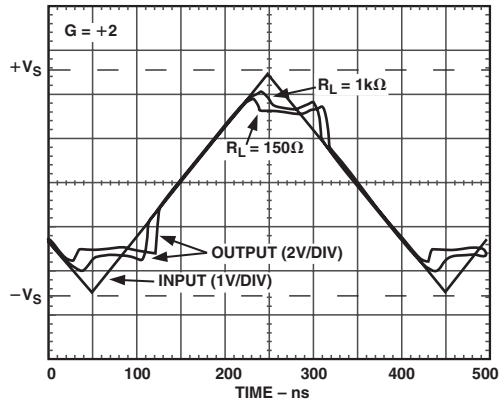
TPC 41. Large Signal Transient Response, G = –1, R_L = 150 Ω



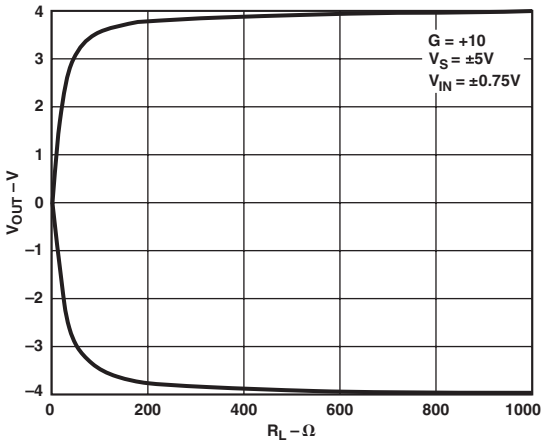
TPC 39. Large Signal Transient Response for Capacitive Load = 0 pF, 10 pF, and 20 pF



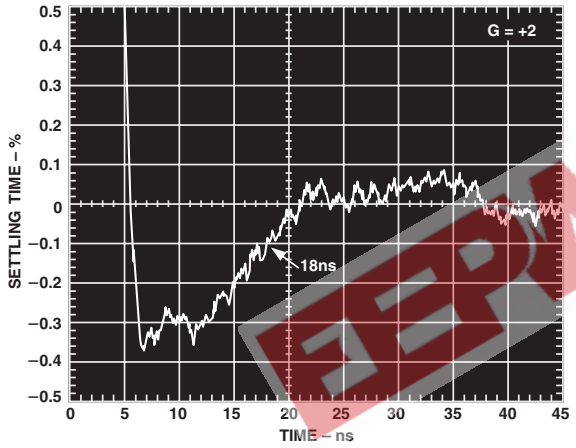
TPC 42. Small Signal Transient Response: Effect of Series Snub Resistor when Driving Capacitive Load



TPC 43. Output Overdrive Recovery, R_L = 1 kΩ, 150 Ω, V_{IN} = ±2.5 V



TPC 45. V_{OUT} Swing vs. R_{LOAD}, V_S = ±5 V, G = +10, V_{IN} = ±0.75 V



TPC 44. 0.1% Settling Time, 2 V Step

THEORY OF OPERATION

The AD8007 (single) and AD8008 (dual) are current feedback amplifiers optimized for low distortion performance. A simplified conceptual diagram of the AD8007 is shown in Figure 3. It closely resembles a classic current feedback amplifier comprised of a complementary emitter-follower input stage, a pair of signal mirrors, and a diamond output stage. However, in the case of the AD8007/AD8008, several modifications have been made to greatly improve the distortion performance over that of a classic current feedback topology.

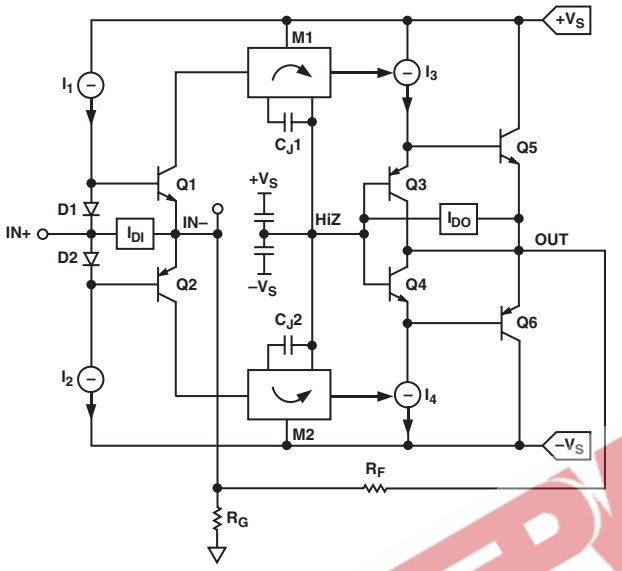


Figure 3. Simplified Schematic of AD8007

The signal mirrors have been replaced with low distortion, high precision mirrors. They are shown as "M1" and "M2" in Figure 3. Their primary function from a distortion standpoint is to greatly reduce the effect of highly nonlinear distortion caused by capacitances C_J1 and C_J2. These capacitors represent the collector-to-base capacitances of the mirrors' output devices.

A voltage imbalance arises across the output stage, as measured from the high impedance node "HiZ" to the output node "Out." This imbalance is a result of delivering high output currents and is the primary cause of output distortion. Circuitry is included to sense this output voltage imbalance and generate a compensating current "I_{DO}." When injected into the circuit, I_{DO} reduces the distortion that would be generated at the output stage. Similarly, the nonlinear voltage imbalance across the input stage (measured from the noninverting to the inverting input) is sensed, and a current "I_{DI}" is injected to compensate for input-generated distortion.

The design and layout are strictly top-to-bottom symmetric in order to minimize the presence of even-order harmonics.

USING THE AD8007/AD8008

Supply Decoupling for Low Distortion

Decoupling for low distortion performance requires careful consideration. The commonly adopted practice of returning the high frequency supply decoupling capacitors to physically separate (and possibly distant) grounds can lead to degraded even-order harmonic performance. This situation is shown in Figure 4 using the AD8007 as an example. Note that for a sinusoidal input, each decoupling capacitor returns to its ground a quasi-rectified current carrying high even-order harmonics.

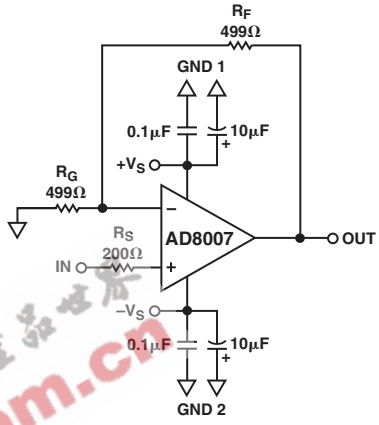


Figure 4. High Frequency Capacitors Returned to Physically Separate Grounds (Not Recommended)

The decoupling scheme shown in Figure 5 is preferable. Here, the two high frequency decoupling capacitors are first tied together at a common node, and are then returned to the ground plane through a single connection. By first adding the two currents flowing through each high frequency decoupling capacitor, one is ensuring that the current returned into the ground plane is only at the fundamental frequency.

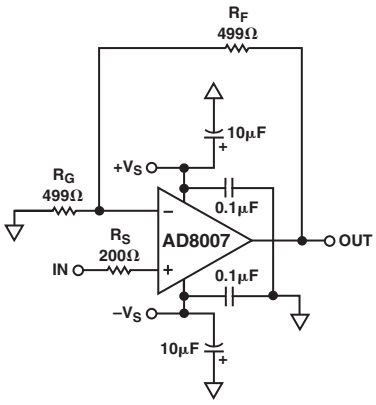


Figure 5. High Frequency Capacitors Returned to Ground at a Single Point (Recommended)

Whenever physical layout considerations prevent the decoupling scheme shown in Figure 5, the user can connect one of the high frequency decoupling capacitors directly across the supplies and connect the other high frequency decoupling capacitor to ground. This is shown in Figure 6.

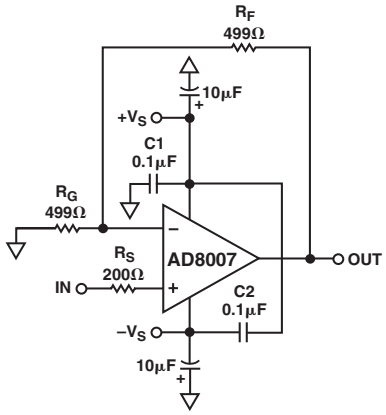


Figure 6. High Frequency Capacitors Connected across the Supplies (Recommended)

Layout Considerations

The standard noninverting configuration with recommended power supply bypassing is shown in Figure 6. This is also the bypassing scheme used on the evaluation board shown in Figure 7. The 0.1 μF high frequency decoupling capacitors should be X7R or NPO chip components. Connect C2 from the $+V_S$ pin to the $-V_S$ pin. Connect C1 from the $+V_S$ pin to signal ground.

The length of the high frequency bypass capacitor leads is critical. Parasitic inductance due to long leads will work against the low impedance created by the bypass capacitor. The ground for the load impedance should be at the same physical location as the bypass capacitor grounds. For the larger value capacitors, which are intended to be effective at lower frequencies, the current return path distance is less critical.

LAYOUT AND GROUNDING CONSIDERATIONS

Grounding

A ground plane layer is important in densely packed PC boards to minimize parasitic inductances. However, an understanding of where the current flows in a circuit is critical to implementing effective high speed circuit design. The length of the current path is directly proportional to the magnitude of parasitic inductances and thus the high frequency impedance of the path. High speed currents in an inductive ground return will create an unwanted voltage noise. Broad ground plane areas will reduce the parasitic inductance.

Input Capacitance

Along with bypassing and ground, high speed amplifiers can be sensitive to parasitic capacitance between the inputs and ground. Even 1 pF or 2 pF of capacitance will reduce the input impedance at high frequencies, in turn increasing the amplifier's gain, causing peaking of the frequency response or even oscillations if severe enough. It is recommended that the external passive components that are connected to the input pins be placed as close as possible to the inputs to avoid parasitic capacitance. The ground and power planes must be kept at a distance of at least 0.05 mm from the input pins on all layers of the board.

Output Capacitance

To a lesser extent, parasitic capacitances on the output can cause peaking of the frequency response. There are two methods to effectively minimize its effect:

1. Put a small value resistor in series with the output to isolate the load capacitance from the amplifier's output stage. (See TPC 7.)
2. Increase the phase margin by (a) increasing the amplifier's gain or (b) adding a pole by placing a capacitor in parallel with the feedback resistor.

Input-to-Output Coupling

To minimize capacitive coupling, the input and output signal traces should not be parallel. This helps reduce unwanted positive feedback.

External Components and Stability

The AD8007 and AD8008 are current feedback amplifiers and, to a first order, the feedback resistor determines the bandwidth and stability. The gain, load impedance, supply voltage, and input impedances also have an effect.

TPC 6 shows the effect of changing R_F on bandwidth and peaking for a gain of +2. Increasing R_F will reduce peaking but also reduce the bandwidth. TPC 1 shows that for a given R_F, increasing the gain will also reduce peaking and bandwidth. Table I shows the recommended R_F and R_G values that optimize bandwidth with minimal peaking.

Table I. Recommended Component Values

Gain	$R_F(\Omega)$	$R_G(\Omega)$	R_S
–1	499	499	200
+1	499	NA	200
+2	499	499	200
+5	499	124	200
+10	499	54.9	200

The load resistor will also affect bandwidth as shown in TPCs 2 and 5. A comparison between TPCs 2 and 5 also demonstrates the effect of gain and supply voltage.

When driving loads with a capacitive component, stability is improved by using a series snub resistor "R_{SNUB}" at the output. The frequency and pulse responses for various capacitive loads are illustrated in TPCs 7 and 42, respectively.

For noninverting configurations, a resistor in series with the input, R_S, is needed to optimize stability for Gain = +1, as illustrated in TPC 3. For larger noninverting gains, the effect of a series resistor is reduced.

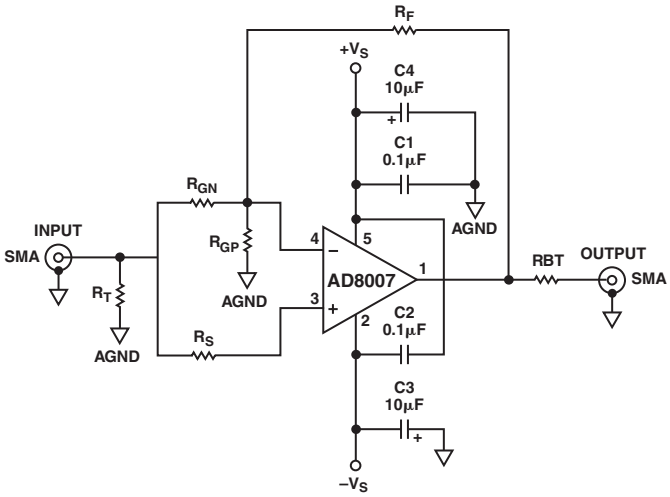


Figure 7. Schematic of AD8007 Evaluation Board for the SC70 Package

EVALUATION BOARD

The SC70 board schematic is shown in Figure 7. To use the SC70 board in an inverting configuration, R_{GN} is used and R_{GP} is left open. The position of R_S can be shifted so that it connects Pin 3 to ground. When used as a noninverter, R_{GP} is populated and R_{GN} is left open. In both configurations, R_T allows for a 50 Ω termination resistor. Universal (inverting or noninverting) AD8007 SOIC, AD8008 SOIC, and AD8008 MSOP boards are also available. The SC70 and MSOP evaluation boards are shown in Figures 8–15.

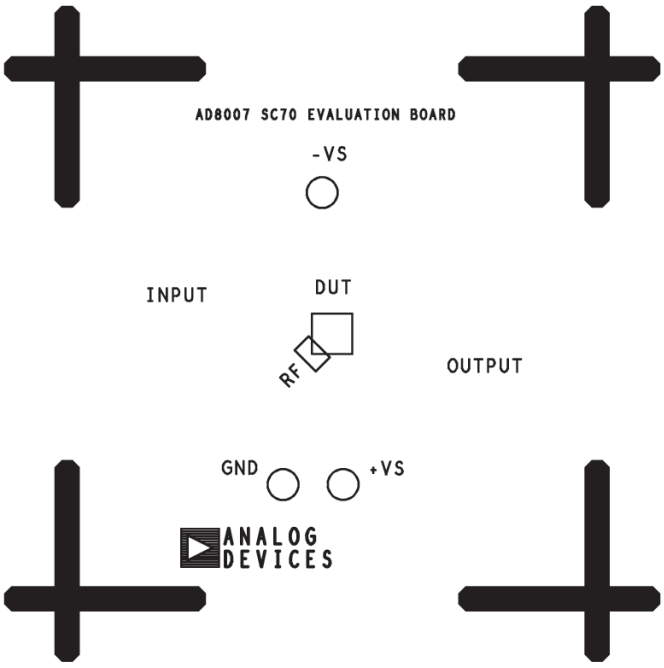


Figure 8. SC70 Evaluation Board Silkscreen (Top)

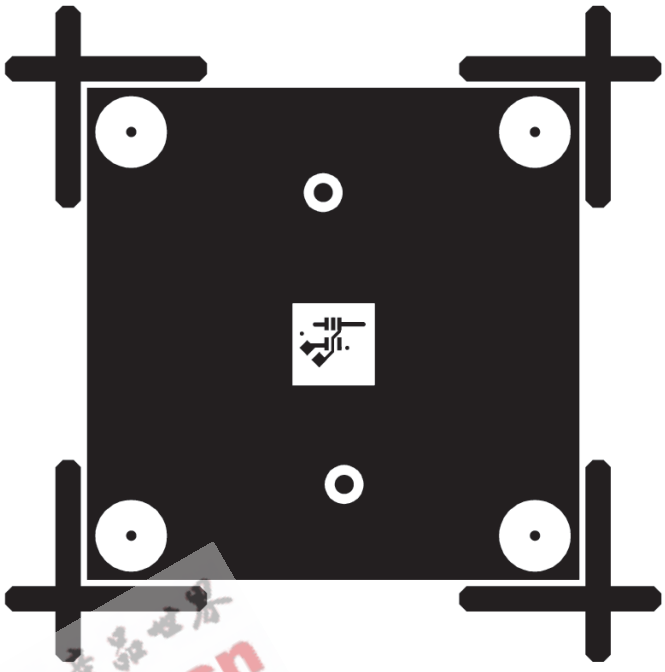


Figure 10. SC70 Evaluation Board, Amplifier Side (Top)

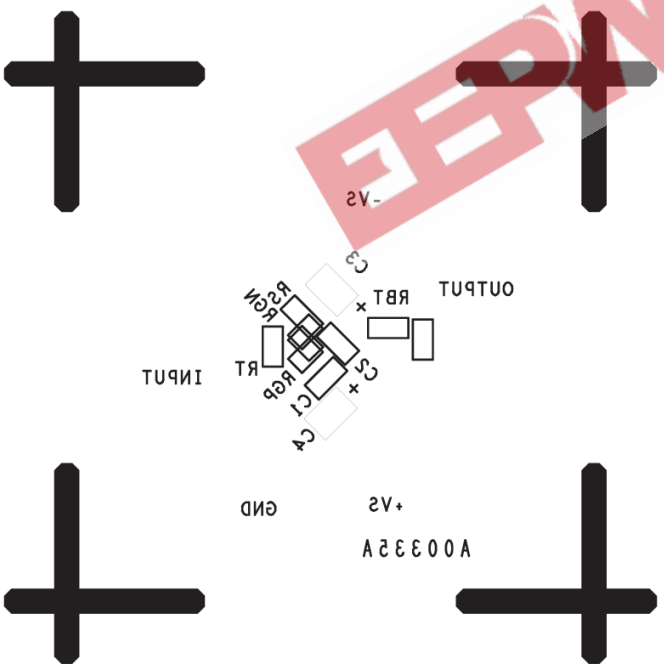


Figure 9. SC70 Evaluation Board Silkscreen (Bottom)

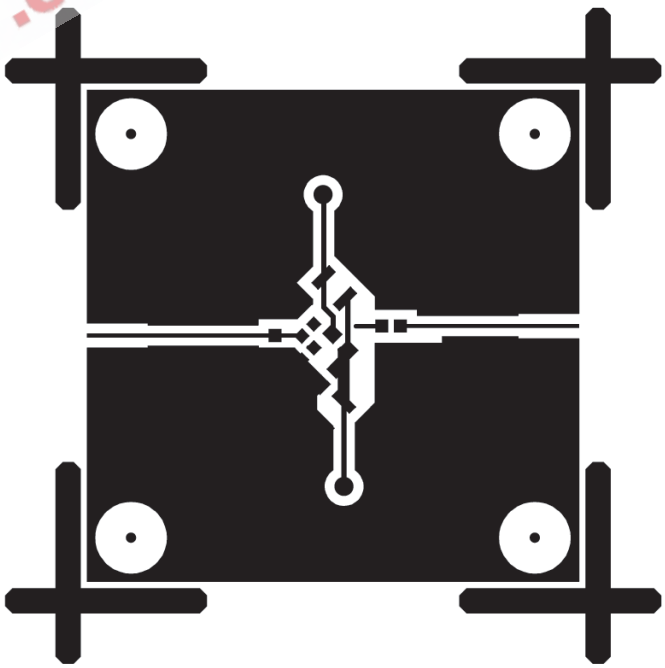


Figure 11. SC70 Evaluation Board, Component Side (Bottom)

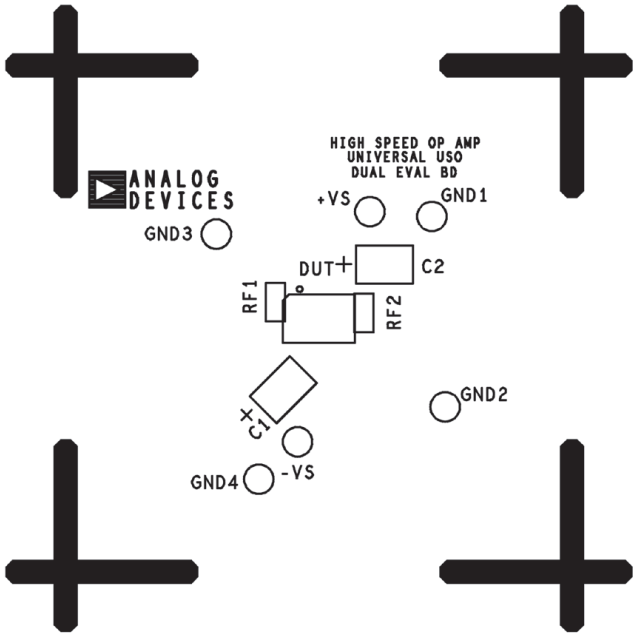


Figure 12. MSOP Evaluation Board Silkscreen (Top)

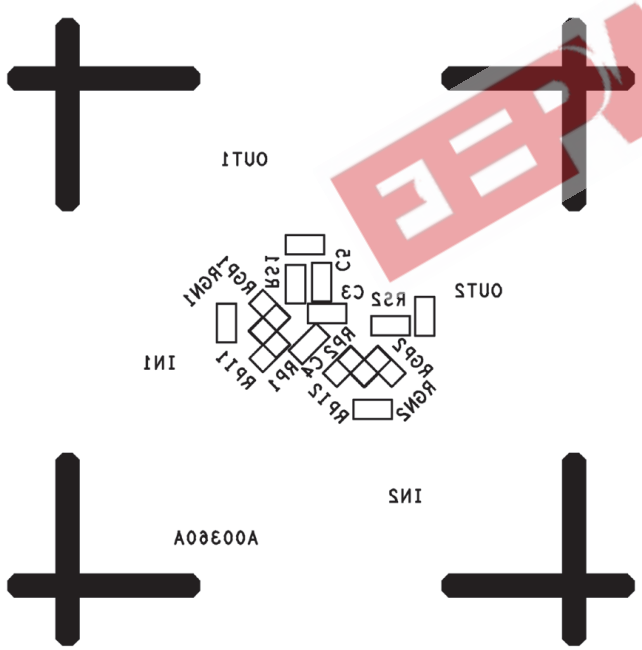


Figure 13. MSOP Evaluation Board Silkscreen (Bottom)

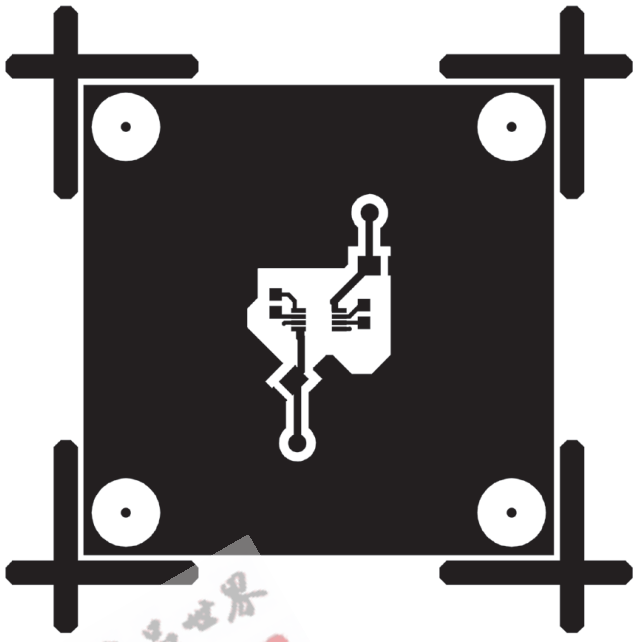


Figure 14. MSOP Evaluation Board, Amplifier Side (Top)

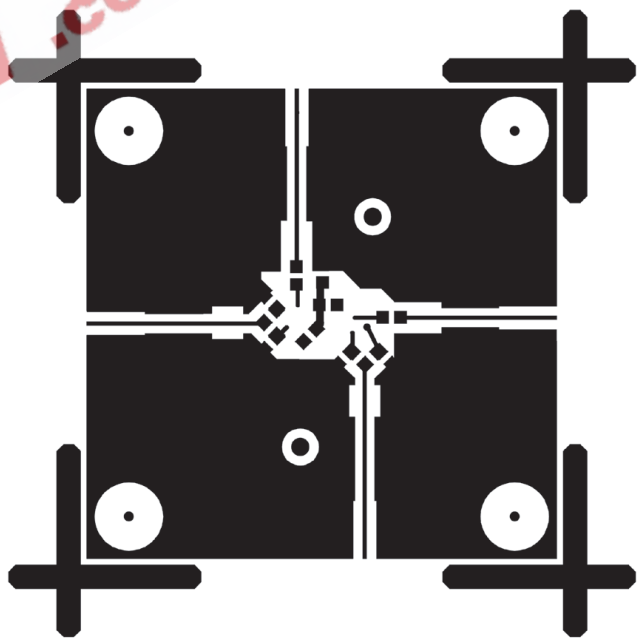
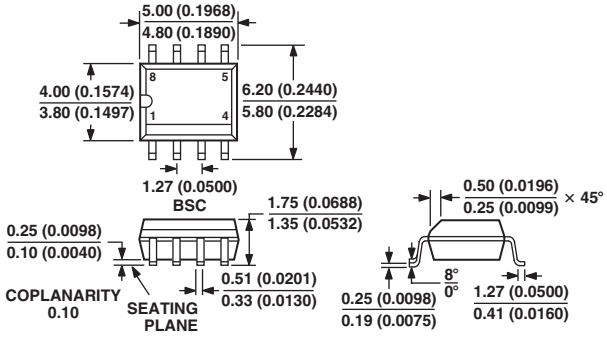


Figure 15. MSOP Evaluation Board, Amplifier Side (Bottom)

OUTLINE DIMENSIONS

8-Lead Standard Small Outline Package [SOIC]
Narrow Body
(RN-8)

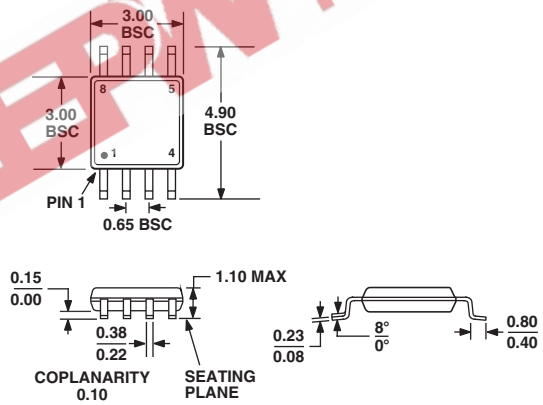
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-012AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

8-Lead MSOP Package [MSOP]
(RM-8)

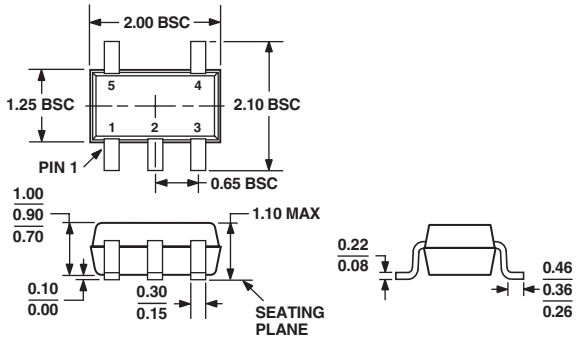
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-187AA

5-Lead Pastic Surface Mount Package [SC70]
(KS-5)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-203AA

Revision History

Location	Page
10/02—Data Sheet changed from REV. B to REV. C	
CONNECTION DIAGRAMS captions updated	1
ORDERING GUIDE updated	5
Figure 5 edited	14
Updated OUTLINE DIMENSIONS	19
9/02—Data Sheet changed from REV. A to REV. B.	
Updated OUTLINE DIMENSIONS	19
8/02—Data Sheet changed from REV. 0 to REV. A.	
Added AD8008	Universal
Added SOIC-8 (RN) and MSOP-8 (RM)	1
Changes to FEATURES	1
Changes to GENERAL DESCRIPTION	1
Changes to SPECIFICATIONS	2
Edits to MAXIMUM POWER DISSIPATION SECTION	4
New Figure 2	4
Changes to ORDERING GUIDE	5
New TPCs 19–24 and TPCs 27, 29, 30, and 35	9
Changes to EVALUATION BOARD section	16
MSOP-8 (RM) added	19

C02866–0–10/02(C)

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