1.1 Scope.

This specification covers the detail requirements for a high speed sample-and-hold amplifier.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
−1	AD346SD/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-H-1000: package outline: DH-14A

1.3 Absolute Maximum Ratings. (T_A = +25°C unless otherwise noted)

$+V_{CC}$ to GND (Pin 11)	+18V
$-V_{CC}$ to GND (Pin 14)	−18V
Digital Input (Pin 1)	0 to +7V
Analog Input (Pin 13)	±15V
Junction Temperature	+175°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 10sec)	+300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 20°C/W
θ_{JA} = 60°C/W

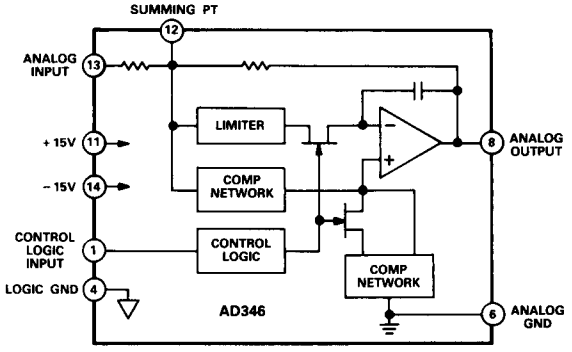
AD346—SPECIFICATIONS

Table 1.

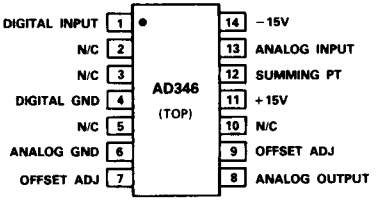
Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition[1]	Units
Analog Input Voltage Range	V_{IN}	−1	10			10		± V min
Overvoltage, No Damage	V_{OV}	−1	15					± V max
Digital Input Logic "1" Current	I_{IH}	−1	20					μA max
Digital Input Logic "0" Current	I_{IL}	−1	360					−μA max
Digital Input Track Mode Logic "1"	V_{IH}	−1	2.0 5.5					V min V max
Digital Input Hold Mode Logic "0"	V_{IL}	−1	0 0.8					V min V max
Analog Output Voltage[2]	V_O	−1	10.0			10.0		± V min
Offset Voltage[3]	V_{OS}	−1	3	3				± mV max
Offset Voltage Temperature Coefficient	V_{OSTC}	−1	20		20			± mV max
Gain Error	A_E	−1	0.02	0.02			% of −1V/V	± % max
Gain Error Over Temperature	TCA_E		0.05		0.05		% of −1V/V	± % max
Offset Step (Pedestal)	O_S	−1	4	4				± mV max
Pedestal Over Temperature	TCO_S	−1	20		20			± mV max
Droop Rate	T_{DR}	−1	0.5	0.5				mV/ms max
Droop Rate over Temperature	T_{DRTC}	−1	650		650			mV/ms max
Acquisition Time to ± 0.01% 10V Step	t_{A1}	−1	2.0					μs max
Acquisition Time to ± 0.01% 20V Step	t_{A2}	−1	2.5			2.5		μs max
Settling Time Sample Mode	t_{S1}	−1	2.0					μs max
Sample to Hold	t_{S2}	−1	1.0					μs max
Feedthrough (Hold Mode)	FT	−1	0.02			0.02	@ $C_L \leq 200pF$	% FSR max
Nominal Voltages for Rated Performance	V_S	−1	15				(± 3%)	± V typ
Power Supply Rejection Ratio	PSRR	−1	300					μV/V max
Supply Currents	$+I_{SS}$	−1	18	18			V_{SS} = ± 15V	mA max
	$-I_{SS}$	−1	10	10			V_{SS} = ± 15V	−mA max
Supply Currents Over Temperature	$+I_{SSTC}$	−1	20		20		V_{SS} = ± 15V	mA max
	$-I_{SSTC}$	−1	10		10		V_{SS} = ± 15V	−mA max

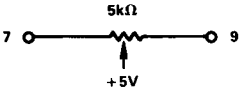
NOTES
[1]T_A = +25°C and ± V_S = ± 15V unless otherwise specified.
[2]Max Output Swing is 4V less than + V_S.
[3]Voltage Offset is externally adjustable to zero.

3.2.1 Functional Block Diagram and Terminal Assignments.



DH-14A Package





TRIM ADJUSTMENT

3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (I).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).