Nonvolatile Memory Digital Potentiometers

AD5231/AD5232/AD5233

FEATURES

Nonvolatile Memory Preset Maintains Wiper Settings
AD5231 Single, 1024 Position Resolution
AD5232 Dual, 256 Position Resolution
AD5233 Quad, 64 Position Resolution
10K, 50K, 100K Ohm Terminal Resistance
Linear or Log taper Settings
Increment/Decrement Commands, Push Button Command
SPI Compatible Serial Data Input with Readback Function
+3 to +5V Single Supply or ±2.5V Dual Supply Operation
User EEMEM nonvolatile memory for constant storage

APPLICATIONS

Mechanical Potentiometer Replacement
Instrumentation: Gain, Offset Adjustment
Programmable Voltage to Current Conversion
Programmable Filters, Delays, Time Constants
Line Impedance Matching
Power Supply Adjustment
DIP Switch Setting

GENERAL DESCRIPTION

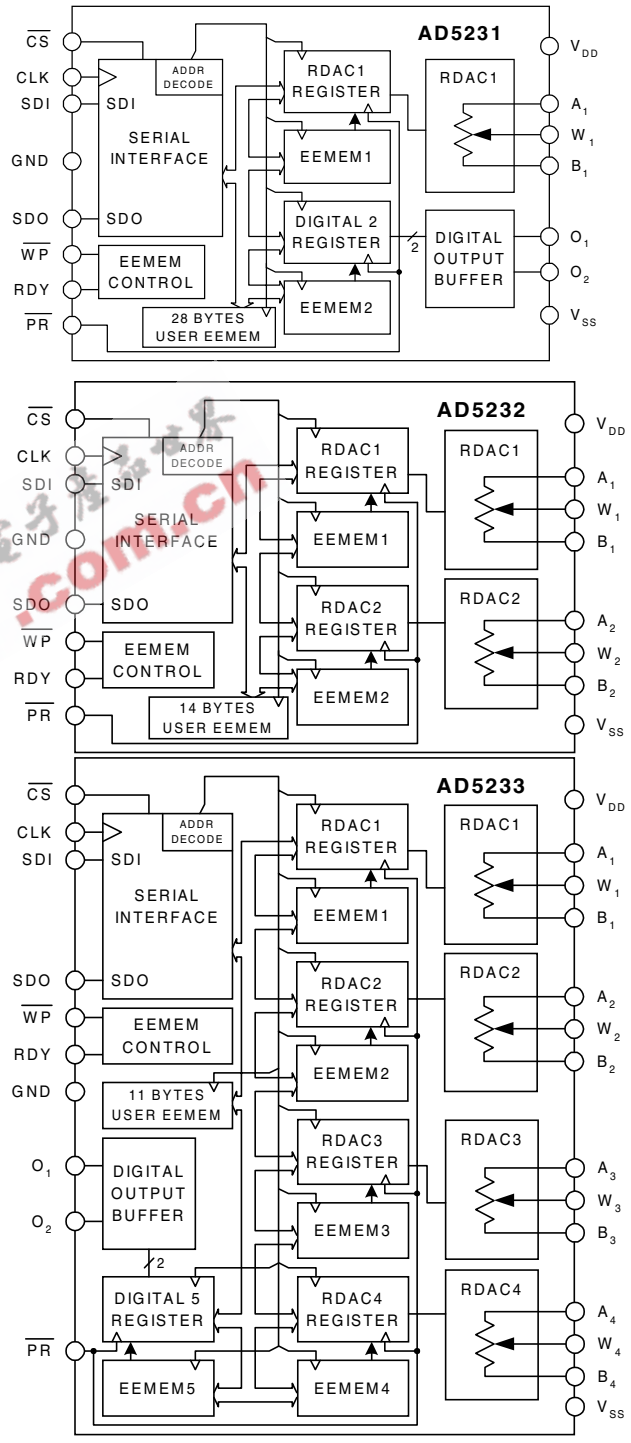
The AD5231/AD5232/AD5233 family provides a single-/dual-/quad-channel, digitally controlled variable resistor (VR) with resolutions of 1024/256/64 positions respectively. These devices perform the same electronic adjustment function as a potentiometer or variable resistor. The AD523X's versatile programming via a Micro Controller allows multiple modes of operation and adjustment.

In the direct program mode a predetermined setting of the RDAC register can be loaded directly from the micro controller. Another key mode of operation allows the RDAC register to be refreshed with the setting previously stored in the EEMEM register. When changes are made to the RDAC register to establish a new wiper position, the value of the setting can be saved into the EEMEM by executing an EEMEM save operation. Once the settings are saved in the EEMEM register these values will be transferred automatically to the RDAC register to set the wiper position at system power ON. Such operation is enabled by the internal preset strobe and the preset can also be accessed externally.

The basic mode of adjustment is the increment and decrement command controlling the present setting of the Wiper position setting (RDAC) register. An internal scratch pad RDAC register can be moved UP or DOWN, one step of the nominal terminal resistance between terminals A-and-B. This linearly changes the wiper to B terminal resistance (R_{WB}) by one position segment of the device's end-to-end resistance (R_{AB}). For exponential/logarithmic changes in wiper setting, a left/right shift command adjusts levels in +/-6dB steps, which can be useful for sound and light alarm applications.

The AD523X are available in the thin TSSOP package. All parts are guaranteed to operate over the extended industrial temperature range of -40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAMS



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AD5231/AD5232/AD5233 - SPECIFICATIONS

ELECTRICAL CHARACTERISTICS 10K, 50K, 100K OHM VERSIONS (V_{DD} = +3V±10% or +5V±10% and V_{SS}=0V, V_A = $+V_{DD}$, V_B = 0V, -40°C < T_A < +85°C unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Units
DC CHARACTERISTICS RHEOSTAT MODE	Specifications apply to all VRs					
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}, V_A=NC	-1	±1/4	+1	LSB
Resistor Nonlinearity[2]	R-INL	R_{WB}, V_A=NC	-1	±1/2	+1	%FS
Nominal resistor tolerance	ΔR	T_A = 25°C, V_{AB} = V_{DD},Wiper (V_W) = No connect	-30		30	%
Resistance Temperature Coefficent	$R_{AB}/\Delta T$	V_{AB} = V_{DD}, Wiper (V_W) = No Connect		500		ppm/°C
Wiper Resistance	R_W	I_W = 1 V/R, V_{DD} = +5V		50	100	Ω
Wiper Resistance	R_W	I_W = 1 V/R, V_{DD} = +3V		200		Ω
DC CHARACTERISTICS POTENTIOMETER DIVIDER MODE	Specifications apply to all VRs					
Resolution	N	AD5231/AD5232/AD5233	10 / 8 / 6			Bits
Integral Nonlinearity[3]	INL		–1	±1/2	+1	%FS
Differential Nonlinearity[3]	DNL		–1	±1/4	+1	LSB
Voltage Divider Temperature Coefficent	$\Delta V_W/\Delta T$	Code = Half-scale		15		ppm/°C
Full-Scale Error	V_{WFSE}	Code = Full-scale	–3		+0	%FS
Zero-Scale Error	V_{WZSE}	Code = Zero-scale	0		+3	%FS
RESISTOR TERMINALS						
Voltage Range[4]	$V_{A,B,W}$		V_{SS}		V_{DD}	V
Capacitance[5] Ax, Bx	$C_{A,B}$	f = 1 MHz, measured to GND, Code = Half-scale		45		pF
Capacitance[5] Wx	C_W	f = 1 MHz, measured to GND, Code = Half-scale		60		pF
Common-mode Leakage Current[6]	I_{CM}	V_A = V_B = V_{DD}/2		0.01	1	µA
DIGITAL INPUTS & OUTPUTS						
Input Logic High	V_{IH}	with respect to GND, VDD = 5V	2.4			V
Input Logic Low	V_{IL}	with respect to GND, VDD = 5V			0.8	V
Input Logic High	V_{IH}	with respect to GND, VDD = 3V	2.1			V
Input Logic Low	V_{IL}	with respect to GND, VDD = 3V			0.6	V
Output Logic High	V_{OH}	$R_{PULL-UP}$ = 2.2KΩ to +5V	4.9			V
Output Logic High	V_{OH}	I_{OH} = 40µA, V_{LOGIC} = +5V	4			V
Output Logic Low	V_{OL}	I_{OL} = 1.6mA, V_{LOGIC} = +5V			0.4	V
Input Current	I_{IL}	V_{IN} = 0V or V_{DD}			±1	µA
Input Capacitance[5]	C_{IL}			5		pF
POWER SUPPLIES						
Single-Supply Power Range	V_{DD}	V_{SS} = 0V	2.7		5.5	V
Dual-Supply Power Range	V_{DD}/V_{SS}		±2.25		±2.75	V
Positive Supply Current	I_{DD}	V_{IH} = V_{DD} or V_{IL} = GND		2	20	µA
Programming Mode Current	$I_{DD(PG)}$	V_{IH} = V_{DD} or V_{IL} = GND		35		mA
Read Mode Current[13]	$I_{DD(READ)}$	V_{IH} = V_{DD} or V_{IL} = GND	0.9		9	mA
Negative Supply Current	I_{SS}	V_{IH} = V_{DD} or V_{IL} = GND, V_{DD} = 2.5V, V_{SS} = -2.5V			10	µA
Power Dissipation[7]	P_{DISS}	V_{IH} = V_{DD} or V_{IL} = GND			0.1	mW
Power Supply Sensitivity	PSS	ΔV_{DD} = +5V ±10%		0.002	0.01	%/%
DYNAMIC CHARACTERISTICS[5, 8]						
Bandwidth –3dB	BW_10K	R = 10KΩ		600		KHz
Total Harmonic Distortion	THD_W	V_A =1Vrms, V_B = 0V, f=1KHz		0.003		%
V_W Settling Time	t_S	V_A= V_{DD}, V_B=0V, 50% of final value				
		For R_{AB} = 10K/50K/100K		1 / 3 / 6		µs
Resistor Noise Voltage	e_{N_WB}	R_{WB} = 5KΩ, f = 1KHz		9		nV√Hz
Crosstalk (C_{W1}/C_{W2})	C_T	V_A = V_{DD}, V_B = 0V, Measure V_W with adjacent				
		VR making full scale change		-65		dB

NOTES: See bottom of table next page.

AD5231/AD5232/AD5233 - SPECIFICATIONS

ELECTRICAL CHARACTERISTICS 10K, 50K, 100K OHM VERSIONS (V_{DD} = +3V±10% to +5V±10% and V_{SS}=0V, V_A = +V_{DD}, V_B = 0V, -40°C < T_A < +85°C unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Units
INTERFACE TIMING CHARACTERISTICS applies to all parts(Notes 5, 9)						
Clock Cycle Time	t_1		20			ns
Input Clock Pulse Width	t_2, t_3	Clock level high or low	10			ns
$\overline{CS}$ Setup Time	t_4		10			ns
Data Setup Time	t_5	From Positive CLK transition	5			ns
Data Hold Time	t_6	From Positive CLK transition	5			ns
CLK Shutdown Time	t_7		0			ns
$\overline{CS}$ Rise to Clock Rise Setup	t_8		10			ns
$\overline{CS}$ High Pulse Width	t_9		10			ns
CLK to SDO Propagation Delay[10]	t_{10}	R_P = 1KΩ, C_L < 20pF	1		25	ns
Store to Nonvolatile EEMEM Save Time[11]	t_{12}	Applies to Command 2_H, 3_H, 9_H			25	ms
$\overline{CS}$ to SDO - SPI line acquire	t_{13}					ns
$\overline{CS}$ to SDO - SPI line release	t_{14}					ns
RDY Rise to $\overline{CS}$ Fall	t_{15}					ns
Startup Time	t_{16}					ms
CLK Setup Time	t_{17}	For 1 CLK period (t_4 - t_3 = 1 CLK period)				ns
Preset Pulse Width (Asynchronous)	t_{PR}		50			ns
Preset Response Time	t_{PRESP}	$\overline{PR}$ pulsed low then high		70		us

NOTES:

1. Typicals represent average readings at +25°C and V_{DD} = +5V.
2. Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic. I_W = V_{DD}/R for both V_{DD}=+3V or V_{DD}=+5V.
3. INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter. V_A = V_{DD} and V_B = V_{SS}. DNL specification limits of ±1LSB maximum are Guaranteed Monotonic operating conditions.
4. Resistor terminals A, B, W have no limitations on polarity with respect to each other.
5. Guaranteed by design and not subject to production test.
6. Common mode leakage current is a measure of the DC leakage from any terminal A, B, W to a common mode bias level of V_{DD} / 2.
7. P_{DISS} is calculated from (I_{DD} x V_{DD}) + (I_{SS} X V_{SS}).
8. All dynamic characteristics use V_{DD} = +5V.
9. See timing diagram for location of measured values. All input control voltages are specified with t_R=t_F=2.5ns(10% to 90% of 3V) and timed from a voltage level of 1.5V. Switching characteristics are measured using both V_{DD} = +3V or +5V.
10. Propagation delay depends on value of V_{DD}, R_{PULL_UP}, and C_L see applications text.
11. Low only for instruction commands 8, 9,10, 2, 3. CMD_8 ~ 1ms; CMD_9,10 ~0.12ms; CMD_2,3 ~20ms
12. Dual Supply Operation primarily affects the POT terminals.
13. Read Mode current is not continuous.

Timing Diagram

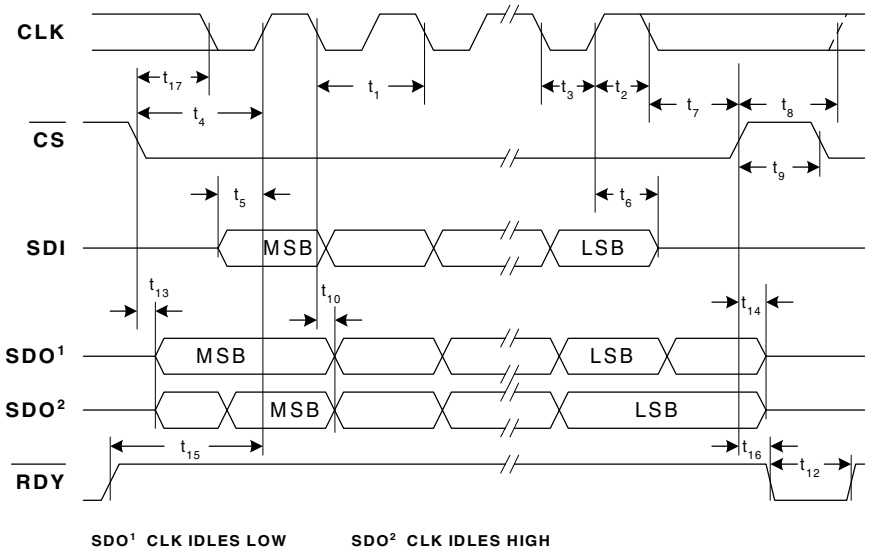


Figure 1. Timing Diagram

Absolute Maximum Rating (T_A = +25°C, unless otherwise noted)

V_{DD} to GND ..... -0.3, +7V
V_{SS} to GND ..... 0V, -7V
V_{DD} to V_{SS} ..... +7V
V_A, V_B, V_W to GND ..... V_{SS}, V_{DD}
A_X – B_X, A_X – W_X, B_X – W_X
Intermittent ..... ±20mA
Continuous ..... ±1.3mA
O_x to GND ..... 0V, V_{DD}
Digital Inputs & Output Voltage to GND ..... 0V, +7V
Operating Temperature Range ..... -40°C to +85°C
Maximum Junction Temperature ($T_{J\ MAX}$) ..... +150°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Package Power Dissipation ..... (T_{JMAX} - T_A) / θ_{JA}
Thermal Resistance θ_{JA},
TSSOP-16 ..... 150°C/W
TSSOP-24 ..... 128°C/W

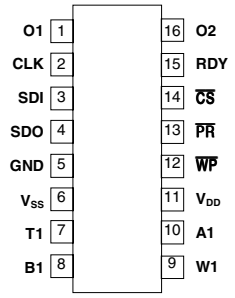
Ordering Guide

Model	Number of Channels	End to End R (k Ohm)	Temp Range	Package Description	Package Option	#Devices per Container	Top Mark
AD5231BRU10	X1	10	-40/+85°C	TSSOP-16	RU-16		
AD5231BRU10-REEL7	X1	10	-40/+85°C	TSSOP-16	RU-16	1,000	
AD5231BRU50	X1	50	-40/+85°C	TSSOP-16	RU-16		
AD5231BRU50-REEL7	X1	50	-40/+85°C	TSSOP-16	RU-16	1,000	
AD5231BRU100	X1	100	-40/+85°C	TSSOP-16	RU-16		
AD5231BRU100-REEL7	X1	100	-40/+85°C	TSSOP-16	RU-16	1,000	
AD5232BRU10	X2	10	-40/+85°C	TSSOP-16	RU-16		
AD5232BRU10-REEL7	X2	10	-40/+85°C	TSSOP-16	RU-16	1,000	
AD5232BRU50	X2	50	-40/+85°C	TSSOP-16	RU-16		
AD5232BRU50-REEL7	X2	50	-40/+85°C	TSSOP-16	RU-16	1,000	
AD5232BRU100	X2	100	-40/+85°C	TSSOP-16	RU-16		
AD5232BRU100-REEL7	X2	100	-40/+85°C	TSSOP-16	RU-16	1,000	
AD5233BRU10	X4	10	-40/+85°C	TSSOP-24	RU-24		
AD5233BRU10-REEL7	X4	10	-40/+85°C	TSSOP-24	RU-24		
AD5233BRU50	X4	50	-40/+85°C	TSSOP-24	RU-24		
AD5233BRU50-REEL7	X4	50	-40/+85°C	TSSOP-24	RU-24		
AD5233BRU100	X4	100	-40/+85°C	TSSOP-24	RU-24		
AD5233BRU100-REEL7	X4	100	-40/+85°C	TSSOP-24	RU-24		

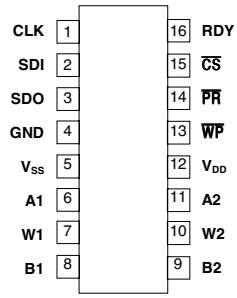
The AD5231/AD5232/AD5233 contains 9,646 transistors.
Die size: 69 mil x 115 mil, 7,993 sq. mil

Nonvolatile Memory Digital Potentiometers AD5231/AD5232/AD5233

AD5231 PIN CONFIGURATION



AD5232 PIN CONFIGURATION



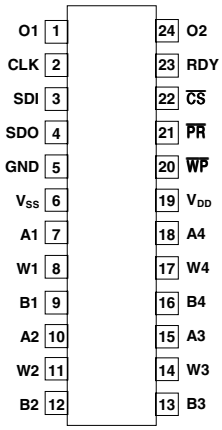
AD5231 PIN FUNCTION DESCRIPTION

#	Name	Description
1	O1	Non-Volatile Digital Output #1, ADDR(O1) = 1H, data bit position D0
2	CLK	Serial Input Register clock pin. Shifts in one bit at a time on positive clock CLK edges.
3	SDI	Serial Data Input Pin.
4	SDO	Serial Data Output Pin. Open Drain Output requires external pull-up resistor. Commands 9 & 10 activate the SDO output. See Instruction operation Truth Table. Other commands shift out the previously loaded bit pattern delayed by 24 clock pulses. This allows daisy-chain operation of multiple packages.
5	GND	Ground pin, logic ground reference.
6	V_{SS}	Negative Supply. Connect to zero volts for single supply applications.
7	T1	Used as digital input during factory test mode. Leave pin floating or connect to V_{DD} or V_{SS}.
8	B1	B terminal of RDAC1.
9	W1	Wiper terminal of RDAC1, ADDR(RDAC1) = 0_H
10	A1	A terminal of RDAC1.
11	V_{DD}	Positive Power Supply Pin. Should be ≥ the input-logic HIGH voltage.
12	$\overline{WP}$	Write Protect Pin. When active low $\overline{WP}$ prevents any changes to the present contents except retrieving EEMEM contents and RESET.
13	$\overline{PR}$	Hardware over ride preset pin. Refreshes the scratch pad register with current contents of the EEMEM register. Factory default loads midscale 200_H until EEMEM loaded with a new value by the user ($\overline{PR}$ is activated at the rising logic high transition)
14	$\overline{CS}$	Serial Register chip select active low. Serial register operation takes place when $\overline{CS}$ returns to logic high.
15	RDY	Ready. Active-high open drain output. Identifies completion of commands 2, 3, 8, 9, 10.
16	O2	Non-Volatile Digital Output #2, ADDR(O2) = 1H, data bit position D1.

AD5232 PIN FUNCTION DESCRIPTION

#	Name	Description
1	CLK	Serial Input Register clock pin. Shifts in one bit at a time on positive clock edges.
2	SDI	Serial Data Input Pin. Shifts in one bit at a time on positive clock CLK edges.
3	SDO	Serial Data Output Pin. Open Drain Output requires external pull-up resistor. Commands 9 & 10 activate the SDO output. See Instruction operation Truth Table. Other commands shift out the previously loaded bit pattern delayed by 16 clock pulses. This allows daisy-chain operation of multiple packages.
4	GND	Ground pin, logic ground reference
5	V_{SS}	Negative Supply. Connect to zero volts for single supply applications.
6	A1	A terminal of RDAC1.
7	W1	Wiper terminal of RDAC1, ADDR(RDAC1) = 0_H.
8	B1	B terminal of RDAC1.
9	B2	B terminal of RDAC2.
10	W2	Wiper terminal of RDAC2, ADDR(RDAC2) = 1_H.
11	A2	A terminal of RDAC2.
12	V_{DD}	Positive Power Supply Pin. Should be ≥ the input-logic HIGH voltage.
13	$\overline{WP}$	Write Protect Pin. When active low, $\overline{WP}$ prevents any changes to the present contents, except retrieving EEMEM content and RESET.
14	$\overline{PR}$	Hardware over ride preset pin. Refreshes the scratch pad register with current contents of the EEMEM register. Factory default loads midscale 80_H until EEMEM loaded with a new value by the user ($\overline{PR}$ is activated at the logic high transition).
15	$\overline{CS}$	Serial Register chip select active low. Serial register operation takes place when $\overline{CS}$ returns to logic high.
16	RDY	Ready. Active-high open drain output. Identifies completion of commands 2, 3, 8, 9, 10.

AD5233 PIN CONFIGURATION



AD5233 PIN FUNCTION DESCRIPTION

#	Name	Description
1	O1	Non-Volatile Digital Output #1, ADDR(O1) = 4_H, data bit position D0.
2	CLK	Serial Input Register clock pin. Shifts in one bit at a time on positive clock CLK edges.
3	SDI	Serial Data Input Pin.
4	SDO	Serial Data Output Pin. Open Drain Output requires external pull-up resistor. Commands 9 & 10 activate the SDO output. See Instruction operation Truth Table. Other commands shift out the previously loaded bit pattern delayed by 16 clock pulses. This allows daisy-chain operation of multiple packages.
5	GND	Ground pin, logic ground reference
6	V_{SS}	Negative Supply. Connect to zero volts for single supply applications.
7	A1	A terminal of RDAC1.
8	W1	Wiper terminal of RDAC1, ADDR(RDAC1) = 0_H.
9	B1	B terminal of RDAC1.
10	A2	A terminal of RDAC2.
11	W2	Wiper terminal of RDAC2, ADDR(RDAC2) = 1_H.
12	B2	B terminal of RDAC2.
13	B3	B terminal of RDAC3.
14	W3	Wiper terminal of RDAC3, ADDR(RDAC3) = 2_H.
15	A3	A terminal of RDAC3.
16	B4	B terminal of RDAC4.
17	W4	Wiper terminal of RDAC4, ADDR(RDAC4) = 3_H.
18	A4	A terminal of RDAC4.
19	V_{DD}	Positive Power Supply Pin. Should be ≥ the input-logic HIGH voltage.
20	$\overline{WP}$	Write Protect Pin. When active low, $\overline{WP}$ prevents any changes to the present contents, except retrieving EEMEM content and RESET.
21	$\overline{PR}$	Hardware over ride preset pin. Refreshes the scratch pad register with current contents of the EEMEM register. Factory default loads midscale 20_H until EEMEM loaded with a new value by the user ($\overline{PR}$ is activated at the logic high transition).
22	$\overline{CS}$	Serial Register chip select active low. Serial register operation takes place when $\overline{CS}$ returns to logic high.
23	RDY	Ready. Active-high open drain output. Identifies completion of commands 2, 3, 8, 9, 10.
24	O2	Non-Volatile Digital Output #2, ADDR(O2) = 4_H, data bit position D1.

OPERATIONAL OVERVIEW

The AD5231/32/33 digital potentiometer family is designed to operate as a true variable resistor replacement device for analog signals that remain within the terminal voltage range of $V_{SS}<V_{TERM}<V_{DD}$. The basic voltage range is limited to a $|V_{DD} - V_{SS}| < 5.5V$.

Control of the digital potentiometer allows both scratch pad register (RDAC register) changes to be made, as well as, 100,000 nonvolatile electrically erasable memory (EEMEM) register operations. The EEMEM update process takes approximately 20.2ms, during this time the shift register is locked preventing any changes from taking place. The RDY pin flags the completion of this EEMEM save. The EEMEM retention is designed to last 15 years at 85°C, which is equivalent to 90 years at 55°C, without refresh.

The scratch pad register can be changed incrementally by using the software controlled Increment/Decrement instruction or the Shift Left/Right instruction command. Once an Increment, Decrement or Shift command has been loaded into the shift register subsequent $\overline{CS}$ strobes will repeat this command. This is useful for push button control applications. Alternately the scratch pad register can be programmed with any position value using the standard SPI serial interface mode by loading the representative data word. The scratch pad register can be loaded with the current contents of the nonvolatile EEMEM register under program control. At system power ON, the default value of the scratch pad memory is the value previously saved in the EEMEM register. The factory EEMEM preset value is midscale.

The scratch pad (wiper) register can be loaded with the current contents of the nonvolatile EEMEM register under hardware control by pulsing the $\overline{PR}$ pin. Beware that the $\overline{PR}$ pulse first sets the wiper at midscale when brought to logic zero, and then on the positive transition to logic high, it reloads the DAC wiper register with the contents of EEMEM. Similarly, the saved EEMEM value will automatically be retrieved to the scratch pad register during system power ON.

A serial data output pin is available for daisy chaining and for readout of the internal register contents. The serial input data register uses a 16 or 24-bit instruction/address/data WORD. Write protect ($\overline{WP}$) disables any changes of current content in the scratch pad register regardless of the commands, except that EEMEM setting can be retrieved using commands 1 and 9. Therefore, write-protect ($\overline{WP}$) pin provides hardware EEMEM protection feature.

DIGITAL INPUT/OUTPUT CONFIGURATION

All digital inputs are ESD protected high input impedance that can be driven directly from most digital sources. For $\overline{PR}$ and $\overline{WP}$, which are active at logic low, can be tied directly to V_{DD} if they are not being used.

The SDO and RDY pins are open drain digital outputs where pull-up resistors are needed only if using these functions. A resistor value in the range of 1k to 10k ohm optimizes the power and switching speed trade off.

SERIAL DATA INTERFACE

The AD523X family contains a four-wire SPI compatible digital interface (SDI, SDO, $\overline{CS}$, and CLK). Key features of this interface include:

- Independently Programmable Read & Write to all registers
- Direct parallel refresh of all RDAC wiper registers from corresponding internal EEMEM registers
- Increment & Decrement instructions for each RDAC wiper register
- Left & right Bit Shift of all RDAC wiper registers to achieve 6dB level changes
- Nonvolatile storage of the present scratch pad RDAC register values into the corresponding EEMEM register
- Extra bytes of user addressable electrical-erasable memory

The serial interface contains three different word formats to support the single AD5231, dual AD5232, and the quad AD5233 digital potentiometer devices. The AD5232 and AD5233 use a 16-bit serial data word loaded MSB first, while the AD5231 uses a 24-bit serial word loaded MSB first. The format of the SPI compatible word is shown in Table 1 and 2. The Command Bits (Cx) control the operation of the digital potentiometer according to the command instructions shown in Table 3, 4, and 5. The Address Bits (Ax) determine which register is activated. The Data Bits (Dx) are the values that are loaded into the decoded register. The last instruction executed prior to a period of no programming activity should be the No OPeration (NOP) instruction. This will place the internal logic circuitry in a minimum power dissipation state.

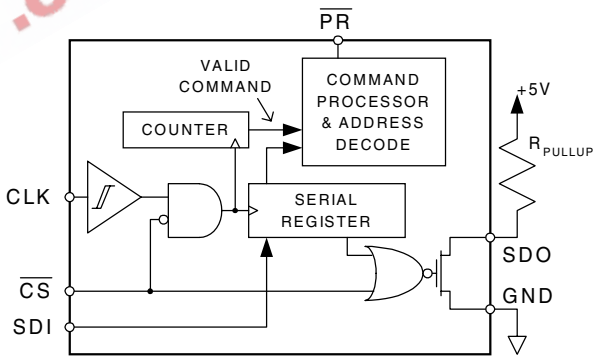


Figure 2. Equivalent Digital Input-Output Logic

The equivalent serial data input and output logic is shown in figure 2. The open drain output SDO is disabled whenever chip select $\overline{CS}$ is logic high. The SPI interface can be used in two slave modes CPHA=1, CPOL=1 and CPHA=0, CPOL=0. CPHA and CPOL refer to the control bits, which dictate SPI timing in the following microprocessors/Micro Converters: ADuC812/824, M68HC11, and MC68HC16R1/916R1.

Table 1. AD5232 & AD5233 16-bit Serial Data Word

	MSB															LSB
AD5232	C3	C2	C1	C0	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
AD5233	C3	C2	C1	C0	A3	A2	A1	A0	X	X	D5	D4	D3	D2	D1	D0

Table 2. AD5231 24-bit Serial Data Word

	MSB																						LSB
AD5231	C3	C2	C1	C0	A3	A2	A1	A0	X	X	X	X	X	X	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Command bits are identified as Cx, address bits are Ax, and data bits are Dx. Command instruction codes are defined in tables 3, 4, & 5.

Table 3. AD5231 Instruction/Operation Truth Table

Inst No.	Instruction Byte 1 B15 •••••••••••••••• B8 C3 C2 C1 C0 A3 A2 A1 A0	Data Byte 1 B15 •••• B8 X ••• D9 D8	Data Byte 0 B7 ••• B0 D7 ••• D0	Operation
0	0 0 0 0 X X X X	X ••• X X	X ••• X	No Operation (NOP): Do nothing
1	0 0 0 1 << ADDR >>	X ••• X X	X ••• X	Write contents of EEMEM(ADDR) to RDAC(ADDR) Register
2	0 0 1 0 << ADDR >>	X ••• X X	X ••• X	SAVE WIPER SETTING: Write contents of RDAC(ADDR) to EEMEM(ADDR)
3	0 0 1 1 << ADDR >>	X ••• D9 D8	D7 ••• D0	Write contents of Serial Register Data Byte 0 & 1 to EEMEM(ADDR)
4	0 1 0 0 << ADDR >>	X ••• X X	X ••• X	Decrement 6dB: Right Shift contents of RDAC(ADDR), stops at all "Zeros".
5	0 1 0 1 X X X X	X ••• X X	X ••• X	Decrement All 6dB: Right Shift contents of all RDAC Registers, stops at all "Zeros".
6	0 1 1 0 << ADDR >>	X ••• X X	X ••• X	Decrement contents of RDAC(ADDR) by "One", stops at all "Zeros".
7	0 1 1 1 X X X X	X ••• X X	X ••• X	Decrement contents of RDAC Register by "One", stops at all "Zeros".
8	1 0 0 0 0 0 0 0	X ••• X X	X ••• X	RESET: Load all RDACs with their corresponding EEMEM previously-saved values
9	1 0 0 1 << ADDR >>	X ••• X X	X ••• X	Write contents of EEMEM(ADDR) to Serial Register Data Byte 0 & 1
10	1 0 1 0 << ADDR >>	X ••• X X	X ••• X	Write contents of RDAC(ADDR) to Serial Register Data Byte 0 & 1
11	1 0 1 1 << ADDR >>	X ••• D9 D8	D7 ••• D0	Write contents of Serial Register Data Byte 0 &1 to RDAC(ADDR)
12	1 1 0 0 << ADDR >>	X ••• X X	X ••• X	Increment 6dB: Left Shift contents of RDAC(ADDR), stops at all "Ones".
13	1 1 0 1 X X X X	X ••• X X	X ••• X	Increment All 6dB: Left Shift contents of all RDAC Registers, stops at all "Ones".
14	1 1 1 0 << ADDR >>	X ••• X X	X ••• X	Increment contents of RDAC(ADDR) by "One", stops at all "Ones".
15	1 1 1 1 X X X X	X ••• X X	X ••• X	Increment contents of RDAC Register by "One", stops at all "Ones".

NOTES:

1. The SDO output shifts-out the last 16-bits of data clocked into the serial register for daisy chain operation. Exception: following Instruction #9 or #10 the selected internal register data will be present in data byte 0 & 1. Instructions following #9 & #10 must be a full 24-bit data word to completely clock out the contents of the serial register.
2. The RDAC register is a volatile scratch pad register that is refreshed at power ON from the corresponding non-volatile EEMEM register.
3. The increment, decrement and shift commands ignore the contents of the shift register Data Byte 0.
4. Execution of the Operation column noted in the table takes place when the $\overline{CS}$ strobe returns to logic high.

Table 4. AD5232 Instruction/Operation Truth Table

Inst No.	Instruction Byte 1 B15 •••••••••••••••• B8 C3 C2 C1 C0 A3 A2 A1 A0	Data Byte 0 B7 •••••••••••••••• B0 D7 D6 D5 D4 D3 D2 D1 D0	Operation
0	0 0 0 0 X X X X	X X X X X X X X	No Operation (NOP): Do nothing
1	0 0 0 1 << ADDR >>	X X X X X X X X	Write contents of EEMEM(ADDR) to RDAC(ADDR) Register
2	0 0 1 0 << ADDR >>	X X X X X X X X	SAVE WIPER SETTING: Write contents of RDAC(ADDR) to EEMEM(ADDR)
3	0 0 1 1 << ADDR >>	D7 D6 D5 D4 D3 D2 D1 D0	Write contents of Serial Register Data Byte 0 to EEMEM(ADDR)
4	0 1 0 0 << ADDR >>	X X X X X X X X	Decrement 6dB: Right Shift contents of RDAC(ADDR) , stops at all "Zeros".
5	0 1 0 1 X X X X	X X X X X X X X	Decrement All 6dB: Right Shift contents of all RDAC Registers, stops at all "Zeros".
6	0 1 1 0 << ADDR >>	X X X X X X X X	Decrement contents of RDAC(ADDR) by "One", stops at all "Zeros".
7	0 1 1 1 X X X X	X X X X X X X X	Decrement contents of all RDAC Registers by "One", stops at all "Zeros".
8	1 0 0 0 0 0 0 0	X X X X X X X X	RESET: Load all RDACs with their corresponding EEMEM previously-saved values
9	1 0 0 1 << ADDR >>	X X X X X X X X	Write contents of EEMEM(ADDR) to Serial Register Data Byte 0
10	1 0 1 0 << ADDR >>	X X X X X X X X	Write contents of RDAC(ADDR) to Serial Register Data Byte 0
11	1 0 1 1 << ADDR >>	D7 D6 D5 D4 D3 D2 D1 D0	Write contents of Serial Register Data Byte 0 to RDAC(ADDR)
12	1 1 0 0 << ADDR >>	X X X X X X X X	Increment 6dB: Left Shift contents of RDAC(ADDR), stops at all "Ones".
13	1 1 0 1 X X X X	X X X X X X X X	Increment All 6dB: Left Shift contents of all RDAC Registers, stops at all "Ones".
14	1 1 1 0 << ADDR >>	X X X X X X X X	Increment contents of RDAC(ADDR) by "One", stops at all "Ones".
15	1 1 1 1 X X X X	X X X X X X X X	Increment contents of all RDAC Registers "One", stops at all "Ones".

NOTES:

1. The SDO output shifts-out the last 8-bits of data clocked into the serial register for daisy chain operation. Exception: following Instruction #9 or #10 the selected internal register data will be present in data byte 0. Instructions following #9 & #10 must be a full 16-bit data word to completely clock out the contents of the serial register.
2. The RDAC register is a volatile scratch pad register that is refreshed at power ON from the corresponding non-volatile EEMEM register.
3. The increment, decrement and shift commands ignore the contents of the shift register Data Byte 0.
4. Execution of the Operation column noted in the table takes place when the $\overline{CS}$ strobe returns to logic high.

Table 5. AD5233 Instruction/Operation Truth Table

Inst No.	Instruction Byte 1 B15 •••••••••••••••• B8 C3 C2 C1 C0 A3 A2 A1 A0	Data Byte 0 B7 •••••••••••••••• B0 D7 D6 D5 D4 D3 D2 D1 D0	Operation
0	0 0 0 0 X X X X	X X X X X X X X	No Operation (NOP): Do nothing
1	0 0 0 1 << ADDR >>	X X X X X X X X	Write contents of EEMEM(ADDR) to RDAC(ADDR) Register
2	0 0 1 0 << ADDR >>	X X X X X X X X	SAVE WIPER SETTING: Write contents of RDAC(ADDR) to EEMEM(ADDR)
3	0 0 1 1 << ADDR >>	D7 D6 D5 D4 D3 D2 D1 D0	Write contents of Serial Register Data Byte 0 to EEMEM(ADDR)
4	0 1 0 0 << ADDR >>	X X X X X X X X	Decrement 6dB: Right Shift contents of RDAC(ADDR), stops at all "Zeros".
5	0 1 0 1 X X X X	X X X X X X X X	Decrement All 6dB: Right Shift contents of all RDAC Registers, stops at all "Zeros".
6	0 1 1 0 << ADDR >>	X X X X X X X X	Decrement contents of RDAC(ADDR) by "One", stops at all "Zeros".
7	0 1 1 1 X X X X	X X X X X X X X	Decrement contents of all RDAC Registers by "One", stops at all "Zeros".
8	1 0 0 0 0 0 0 0	X X X X X X X X	RESET: Load all RDACs with their corresponding EEMEM previously-saved values
9	1 0 0 1 << ADDR >>	X X X X X X X X	Write contents of EEMEM(ADDR) to Serial Register Data Byte 0
10	1 0 1 0 << ADDR >>	X X X X X X X X	Write contents of RDAC(ADDR) to Serial Register Data Byte 0
11	1 0 1 1 << ADDR >>	D7 D6 D5 D4 D3 D2 D1 D0	Write contents of Serial Register Data Byte 0 to RDAC(ADDR)
12	1 1 0 0 << ADDR >>	X X X X X X X X	Increment 6dB: Left Shift contents of RDAC(ADDR), stops at all "Ones".
13	1 1 0 1 X X X X	X X X X X X X X	Increment All 6dB: Left Shift contents of all RDAC Registers, stops at all "Ones".
14	1 1 1 0 << ADDR >>	X X X X X X X X	Increment contents of RDAC(ADDR) by "One", stops at all "Ones".
15	1 1 1 1 X X X X	X X X X X X X X	Increment contents of all RDAC Registers by "One", stops at all "Ones".

NOTES:

1. The SDO output shifts-out the last 8-bits of data clocked into the serial register for daisy chain operation. Exception: following Instruction #9 or #10 the selected internal register data will be present in data byte 0. Instructions following #9 & #10 must be a full 16-bit data word to completely clock out the contents of the serial register. The wiper only has 64 positions that correspond to the lower 6-bits of register data.
2. The RDAC register is a volatile scratch pad register that is refreshed at power ON from the corresponding non-volatile EEMEM register.
3. The increment, decrement and shift commands ignore the contents of the shift register Data Byte 0.
4. Execution of the Operation column noted in the table takes place when the $\overline{CS}$ strobe returns to logic high.

Latched Digital Outputs

A pair of digital outputs, O1 & O2, is available on the AD5231, and the AD5233 parts that provide a nonvolatile logic 0 or logic 1 setting. O1 & O2 are standard CMOS logic outputs shown in figure 2A. These outputs are ideal to replace functions often provided by DIP switches. In addition, they can be used to drive other standard CMOS logic controlled parts that need an occasional setting change.

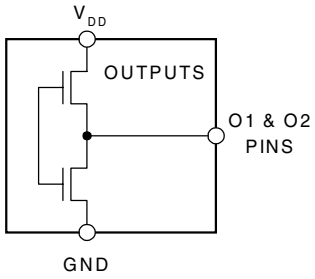


Figure 2A. Logic Outputs O1 & O2.

Using Additional internal Nonvolatile EEMEM

The AD523x family of devices contains additional internal user storage registers (EEMEM) for saving constants and other 8-bit data. Table 6 provides an address map of the internal storage registers shown in the functional block diagrams as EEMEM1, EEMEM2, … EEMEMn, and bytes of USER EEMEM.

Table 6: EEMEM Address Map

EEMEM Address (ADDR)	EEMEM Contents of each device EEMEM(ADDR)		
	AD5231 (16B)	AD5232 (8B)	AD5233 (8B)
0000	RDAC	RDAC1	RDAC1
0001	O1 & O2	RDAC2	RDAC2
0010	USER 1	USER 1	RDAC3
0011	USER 2	USER 2	RDAC4
0100	USER 3	USER 3	O1 & O2
0101	USER 4	USER 4	USER 1
***	***	***	***
1111	USER 14	USER 14	USER 11

NOTES:

1. RDAC data stored in EEMEM locations are transferred to their corresponding RDAC REGISTER at Power ON, or when the following instructions are executed Inst#1 and Inst#8.
2. O1 & O2 data stored in EEMEM locations are transferred to their corresponding DIGITAL REGISTER at Power ON, or when the following instructions are executed Inst#1 and Inst#8.
3. USER data are internal nonvolatile EEMEM registers available to store and retrieve constants using Inst#3 and Inst#9 respectively.
4. AD5231 EEMEM locations are 2 bytes each (16-bits) of data, while the AD5232 & AD5233 are 1 byte each (8-bits).

Detail Programmable Potentiometer Operation

The actual structure of the RDAC is designed to emulate the performance of a mechanical potentiometer. The RDAC contains a string of connected resistor segments, with an array of analog switches that act as the wiper connection to several points along the resistor array. The number of points is the resolution of the device. For example, the AD5232 has 256 connection points allowing it to provide better than 0.5% set-ability resolution. Figure 3 provides an equivalent diagram of the connections between the three terminals that make up one channel of the RDAC. The SW_A and SW_B will always be ON while one of the switches SW(0) to SW(2^N-1) will be ON one at a time depending upon the resistance step decoded from the Data Bits. Note there are two 50 ohm wiper resistances, R_W. The resistance contributed by R_W must be accounted for in the output resistance. At terminals A-to-wiper, R_W is the sum of the resistances of SW_A and SW_X. Similarly, R_W is the sum of the resistances SW_B and SW_X at terminals B-to-Wiper.

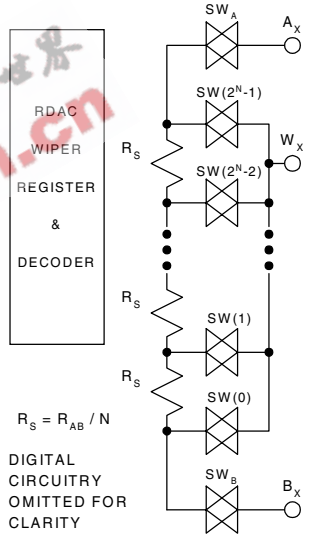


Figure 3. Equivalent RDAC structure

TEST CIRCUITS

Figures X7 to X15 define the test conditions used in the product specification's table.

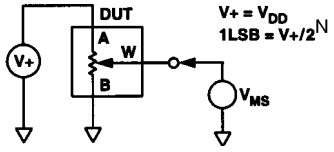


Figure X7. Potentiometer Divider Nonlinearity error test circuit (INL, DNL)

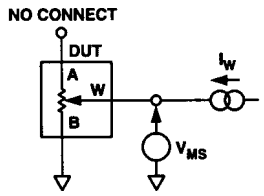


Figure X8. Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)

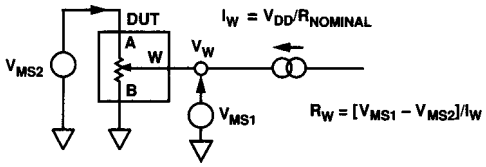


Figure X9. Wiper Resistance test Circuit

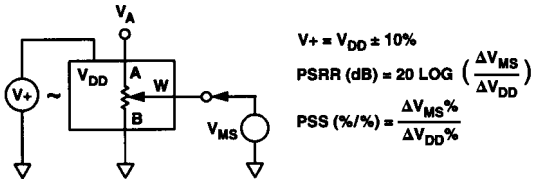


Figure X10. Power supply sensitivity test circuit (PSS, PSSR)

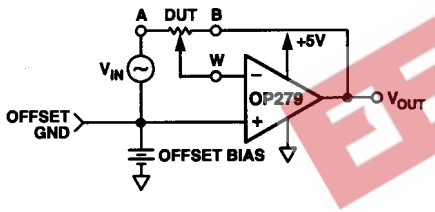


Figure X11. Inverting Gain test Circuit

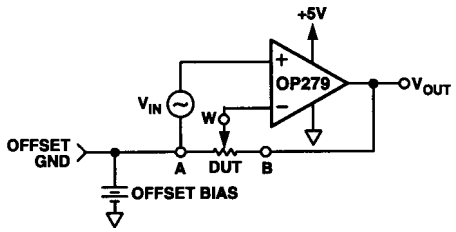


Figure X12. Non-Inverting Gain test circuit

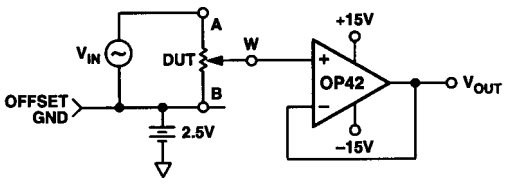


Figure X13. Gain Vs Frequency test circuit

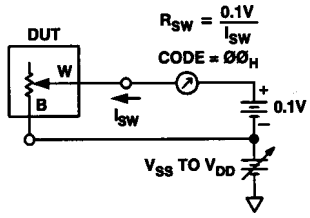


Figure X14. Incremental ON Resistance Test Circuit

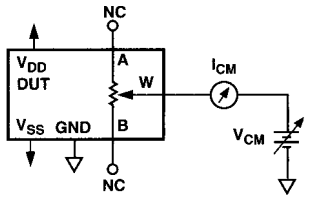


Figure X15. Common Mode Leakage current test circuit

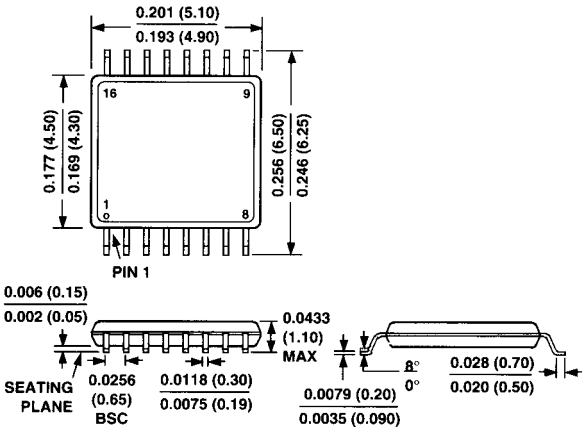
TYPICAL PERFORMANCE GRAPHS

TBD

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm)

16-Lead TSSOP
(RU-16)



24-Lead Thin Surface Mount TSSOP Package (RU-24)