DATEL

# ADC-ET Series
# Monolithic A/D Converters with Three-State Outputs

1

## FEATURES

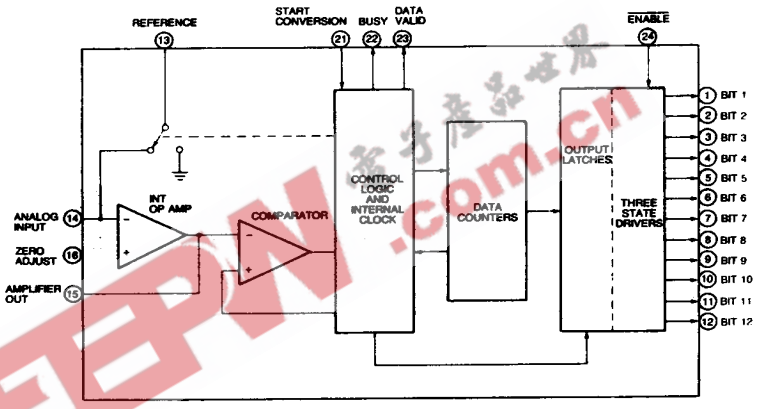
- **Monolithic CMOS**
- **Three-state outputs**
- **12-Bit accuracy**
- **No missing codes**
- **Low cost**
- **Microprocessor-compatible**

## GENERAL DESCRIPTION

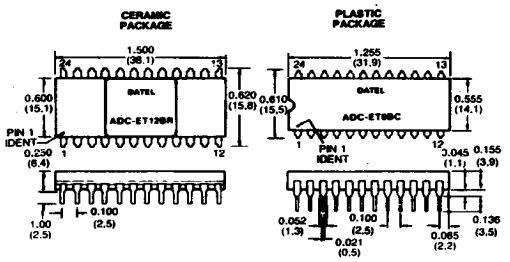
The ADC-ET series devices are low cost integrating A/D converters optimized for high accuracy, linearity and noise immunity. They operate at low power consumption, with sufficient speed to handle most industrial and instrumentation requirements. Discretely controllable three state outputs allow bus organized output connections making these units ideal for microprocessor interfacing.

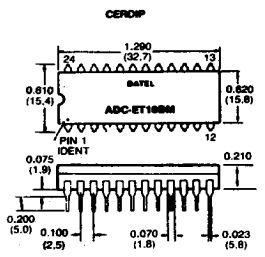
Fabricated with monolithic CMOS techniques, each device is housed in a single 24 pin dual in-line package. The converter consists of an integrating operational amplifier, comparator, current switch, internal clock, two counters, latching output buffers and control logic circuitry. Operation of the circuit requires only a few external passive components and connection to external reference and power supplies. Conversion is accomplished by an incremental charge balancing technique which assures high linearity and noise immunity, along with inherent monotonicity resulting in no missing codes. At the completion of a conversion, the binary coded result appears in parallel form on discretely controlled latched outputs which are CMOS, low power TTL, or low power Schottky TTL compatible. The controllable outputs may be switched to a high impedance or off state by holding the $\overline{\text{ENABLE}}$ high.

Conversion times are 1.8, 6, and 24 milliseconds for the 8-, 10- and 12-bit units respectively. Other typical specifications include linearity to ¼ LSB and a gain tempco of 25 ppm/°C. The analog input voltage range is programmable by means of an external resistor which sets the current into the integrator at 10 μA full scale. Standard operating mode is unipolar but bipolar operation can be implemented by using an external operational amplifier to provide an offset current from the reference. Power requirement is ±5V dc at 2 mA which, for intermittent duty applications, may be reduced to only 200 μA during standby periods without affecting data in the output latches.




## MECHANICAL DIMENSIONS INCHES (MM)




### INPUT/OUTPUT CONNECTIONS

| PIN | FUNCTION | PIN | FUNCTION |
|---|---|---|---|
| 1 | BIT 1 (MSB-12 BITS) | 13 | REFERENCE |
| 2 | BIT 2 | 14 | ANALOG INPUT |
| 3 | BIT 3 (MSB-10 BITS) | 14 | AMPLIFIER OUT |
| 4 | BIT 4 | 16 | ZERO ADJUST |
| 5 | BIT 5 (MSB-8 BITS) | 17 | BIAS |
| 6 | BIT 6 | 18 | −5V POWER |
| 7 | BIT 7 | 19 | +5V POWER |
| 8 | BIT 8 | 20 | GROUND |
| 9 | BIT 9 | 21 | START CONVERT |
| 10 | BIT 10 | 22 | BUSY OUTPUT |
| 11 | BIT 11 | 23 | DATA VALID |
| 12 | BIT 12 (LSB-ALL) | 24 | $\overline{\text{ENABLE}}$ |

**NOTE:** Do not connect unused data output pins on 8- and 10-bit models, they are internally connected to the converter.

DATEL

| ABSOLUTE MAXIMUM RATINGS | |
|---|---|
| $I_{IN}$ | ±10 mA |
| $I_{REF}$ | ±10 mA |
| Digital Input Voltage | −0.3V to $V_{DD}$ +0.3V |
| $V_{DD}$-Vss | 18V |
| Package Dissipation | 500 mW |

## FUNCTIONAL SPECIFICATIONS

**Typical at 25°C, 5V Supplies, $R_{BIAS}$ 100K, unless otherwise noted.**

| ANALOG INPUTS | |
|---|---|
| Type Analog Input | Single-Ended |
| Input Current Range | 0 to +10 μA |
| Reference Current | −20 μA |

| DIGITAL INPUTS | |
|---|---|
| Logical "1" $V_{IH}$ | 3.5V minimum |
| Logical "0" $V_{IN}$ | 1.5V maximum |
| Start Convert Pulse Width | 500 nanoseconds minimum |
| ENABLE Propagation Delay | 500 nanoseconds |

| OUTPUTS | |
|---|---|
| Output Off State Current | 0.1 μA typical, ±10 μA maximum |
| Logic "1" Output Voltage | +4.5V minimum at −10 μA<br>+2.4V minimum at −360 μA[4] |
| Logic "0" Output Voltage | +0.4V maximum at 360 μA[4] |
| Data Valid Output | High for Data Valid, Low When Loading |
| Busy Output | High During Conversion |

| PERFORMANCE | |
|---|---|
| Resolution | 8, 10, 12 Bits |
| Coding, Unipolar | Straight Binary |
| Bipolar | Offset Binary |
| Conversion Times | |
| 8 Bits | 1.8 milliseconds maximum |
| 10 Bits | 6 milliseconds maximum |
| 12 Bits | 24 milliseconds maximum |
| Nonlinearity | ±¼ LSB typical,<br>±½ LSB maximum[1] |
| Differential Nonlinearity | ±¼ LSB typical,<br>±½ LSB maximum |
| Diff. Nonlinearity Tempco | ±2.5 ppm/°C |
| No Missing Codes | Over Operating Temp. Range |
| Initial Gain Error, (Adj. to Zero) | ±5% maximum |
| Gain Temperature Coefficient | ±25 ppm/°C typical, ±75 ppm/°C maximum[2] |
| Initial Zero Error (Adj. to Zero) | ±50 mV maximum |
| Zero Drift Tempco | ±50 μV/°C maximum[2] |
| Power Supply Sensitivity | ±0.05%/% maximum[3] |

| POWER REQUIREMENTS | |
|---|---|
| Voltage, Rated Performance | ±5V dc |
| Voltage Range, Operating | ±3.5V dc to ±7V dc |
| Supply Quiescent Current | |
| C Suffix | ±5.0 mA maximum |
| R Suffix | ±2.5 mA maximum |
| M Suffix | ±3.5 mA maximum |

| PHYSICAL/ENVIRONMENTAL | |
|---|---|
| Operating Temperature Range | |
| C Suffix | 0°C to +70°C |
| R Suffix | −25°C to +85°C |
| M Suffix | −55°C to +125°C |
| Package | |
| C Suffix | 24 Pin Plastic DIP |
| R & M Suffix | 24 Pin Ceramic DIP |

**FOOTNOTES:**
1. Nonlinearity for model ADC-ET12BC only is typically ±¼ LSB, ±1½ LSB maximum.
2. For M suffix units only gain tempco is typically 40 ppm/°C, 80 ppm/°C maximum and zero drift tempco is ±80 μV/°C.
3. $V_{DD}$ ±1V, Vss ±1V.
4. M suffix logic outputs can sink and source 500 μA.

## TECHNICAL NOTES

1. The ADC-ET series are CMOS devices and must be properly handled to prevent damage due to static discharge. Proper anti-static precautions should be taken, including storage and transport in anti-static containers or conductive foam, and grounding of work stations, handling equipment and personnel. Do not connect in circuits under "power on" conditions. The input voltage should be applied after power is on. Do not open the circuitry for the zero adjust, reference or start convert pins while the power is on. It should be noted that the top and bottom of the ceramic package are connected to the positive supply.
2. Nominal values of input, reference and offset resistors are given in the resistor table. Due to the possible ±5% tolerance of the external reference and the +5%, −3% tolerance of the converter scale factor, the actual resistor value can vary by almost ±10%. $R_G$ and $R_T$ in the diagrams are for trimming gain and bipolar offset during calibration. It is recommended that $R_G$ be 1% of $R_{IN}$ (nominal) and that $R_T$ be 1% of $R_{OFF}$ (nominal). They should both be 100 ppm/°C cermet trimming pots. The recommended procedure for selecting $R_{IN}$ and $R_{OFF}$ is set to $R_G$ and $R_T$ to the center of their ranges and choose a 1% metal film resistor which gives the closest fit at the full scale point 1111 . . . . 111 for $R_{IN}$ and one that gives the closest fit to the zero scale point 0000 . . . 000 for $R_T$.
3. The temperature stability of the ADC-ET converters depends directly on the converter itself, $R_{IN}$, $R_{REF}$, $R_{OFF}$ and $V_{REF}$. Since the converter is typically ±25 ppm/°C. It is recommended that a 10 ppm/°C reference be used along with 10 ppm/°C metal film resistors for $R_{IN}$, $R_{REF}$ and $R_{OFF}$ for best performance over temperature.
4. Passive components used with the converter may have tolerances as indicated here: $C_c$ is a ±20% ceramic capacitor; $C_{INT}$ is a ±10% glass or ceramic capacitor; $R_{c1}$, $R_{BIAS}$ and the two zero adjust resistors are ±10% carbon composition type.
5. It is recommended that two 0.1 μF bypass capacitors be used at the power supply pins as shown in the connection diagram. $C_{INT}$ should be connected as close as possible to pins 14 and 15 and as far as possible from any noisy lines.
6. Logic signals should not be routed under these devices or near the input, reference or zero adjust pins.
7. All digital outputs will drive two low power TTL loads or one low power Schottky TTL load. The outputs should not be overloaded as this will affect the performance of the converter.

## TECHNICAL NOTES (Cont'd)

8. It should be noted that there is a propagation delay of approximately 500 nanoseconds between the time ENABLE changes state and the time that the outputs change state.
9. Two's complement coding can be implemented by inverting the MSB signal.
10. $I_{IN}$ and $I_{REF}$, pins 14 and 13 respectively, connect to the summing junction of an operational amplifier which requires a current input. Voltage sources cannot be attached directly to them, but must be buffered by external resistors. Refer to Test Circuit Diagrams. Analog input can be any positive voltage when applied through the proper scaling resistor.
11. Conversion accuracy is directly dependent on $V_{REF}$. In order to avoid degrading accuracy, $V_{REF}$ voltage regulation must be ±0.04% for 8-bit models, ±0.01% for 10-bit models and ±0.0025% for 12-bit models.

## DESCRIPTION OF OPERATION

When the START CONVERT input is strobed with a positive pulse of at least 500 nanoseconds duration, the busy line latches high and a start up cycle of approximately 10 microseconds begins, during which the integrating capacitor is discharged and both counters are reset. Conversion begins at the end of an internal reset pulse.

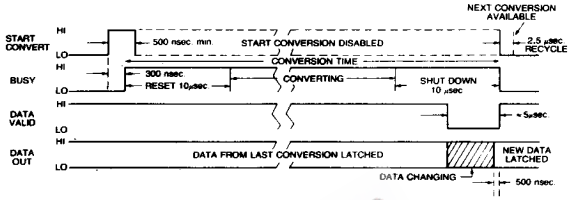
During conversion, the sum of a continuous current, $I_{IN}$ and pulses of an inversely signed reference current $I_{REF}$, is integrated. $I_{IN}$ is proportional to the analog input voltage and $I_{REF}$ is proportional to the reference voltage. A pulse of $I_{REF}$ is applied as required to maintain the summing input of the integrating operational amplifier near zero. The total number of pulses of $I_{REF}$ required to maintain the summing input near zero is counted and the binary coded result is latched into the outputs at the end of conversion.

The end of conversion is signaled by a pulse generated by the clock counter or by the data counter when an overflow condition occurs; this pulse disables further inputs into both counters and begins a 10 microseconds shutdown cycle. During the shutdown cycle, Data Valid goes low for 5 microseconds, while the result of the latest conversion is being transferred to the outputs. Until transfer is complete, the data at the outputs is not valid. At the end of the shutdown cycle, Data Valid goes high indicating that the outputs are latched with the result of the last conversion, and the Busy Output goes low indicating the completion of the conversion cycle and the availability of the converter for the next conversion.

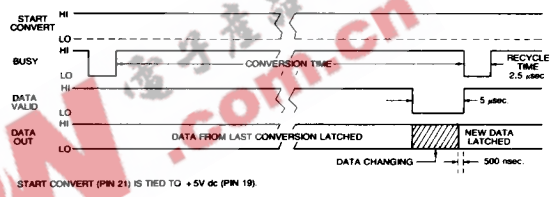
When the converter is employed in a free-running mode, the START CONVERT input is held high (simply connect pin 21 to pin 19), the Busy Output will go low for aproximately 2.5 microseconds to mark the completion and initiation of consecutive conversion cycles. It should be noted that once conversion is initiated, the cycle cannot be interrupted; the START CONVERT pin is disabled when the Busy Output is high, and thus its logic state has no effect until completion of the conversion cycle. After the completion of a conversion, the output data remains valid for as long as power is applied to the circuit, or until Data Valid goes low at the end of a conversion.

## TIMING DIAGRAMS

### CLOCKED OPERATION




### FREE RUNNING OPERATION




START CONVERT (PIN 21) IS TIED TO +5V dc (PIN 19).

## CODING TABLES

**STRAIGHT BINARY**

| | 8 BIT | | 10 BIT | | 12 BIT | |
|---|---|---|---|---|---|---|
| SCALE | 0 TO +10V | CODE | 0 TO +10V | CODE | 0 TO +10V | CODE |
| FS-1 LSB | +9.96V | 1111 1111 | +9.990V | 11 1111 1111 | +9.9976V | 1111 1111 1111 |
| ½ FS | +5.00 | 1000 0000 | +5.000 | 10 0000 0000 | +5.0000 | 1000 0000 0000 |
| 1LSB | +0.04 | 0000 0001 | +0.010 | 00 0000 0001 | +0.0024 | 0000 0000 0001 |
| 0 | 0.00 | 0000 0000 | 0.000 | 00 0000 0000 | 0.0000 | 0000 0000 0000 |

**OFFSET BINARY**

| | 8 BIT | | 10 BIT | | 12 BIT | |
|---|---|---|---|---|---|---|
| SCALE | ±5V | CODE | ±5V | CODE | ±5V | CODE |
| +FS-1 LSB | +4.96V | 1111 1111 | +4.990V | 11 1111 1111 | +4.9976V | 1111 1111 1111 |
| 0 | 0.00 | 1000 0000 | 0.000 | 10 0000 0000 | 0.0000 | 1000 0000 0000 |
| −FS + 1 LSB | −4.96 | 0000 0001 | −4.990 | 00 0000 0001 | −4.9976 | 0000 0000 0001 |
| −FS | −5.00 | 0000 0000 | −5.000 | 00 0000 0000 | −5.0000 | 0000 0000 0000 |

## RESISTOR TABLES

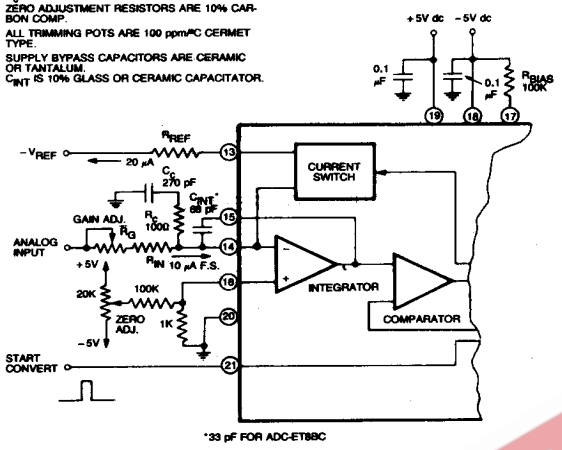
| UNIPOLAR RANGE | BIPOLAR RANGE | $R_{IN}$ (NOMINAL) |
|---|---|---|
| 0 TO +2V | ±1V | 200K |
| 0 TO +5V | ±2.5V | 500K |
| 0 TO +10V | ±5V | 1 MEG |
| 0 TO +20V | ±10V | 2 MEG |

| $V_{REF}$ | $R_{REF}$ (NOMINAL) | $R_{OFF}$ (NOMINAL) |
|---|---|---|
| −1.22V | 61K | 244K |
| −2.5V | 125K | 500K |
| −6.4V | 320K | 1.28 MEG. |

## CONNECTIONS AND CALIBRATION

### CONNECTION FOR UNIPOLAR OPERATION

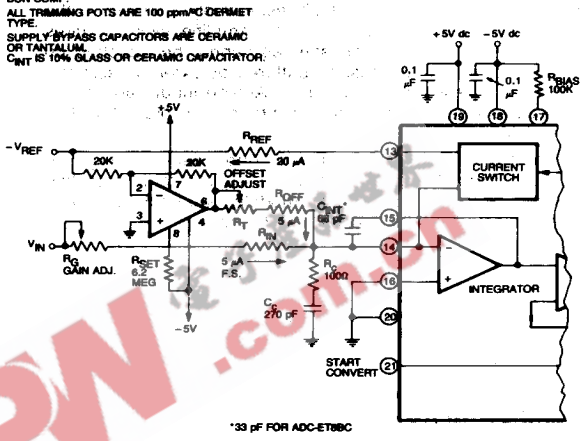
$R_{IN}$, $R_{REF}$ ARE 1% METAL FILM RESISTORS.
$R_{BIAS}$, $R_C$ ARE 10% CARBON COMP RESISTORS.
$C_C$ is 20% CERAMIC CAPACITOR.
ZERO ADJUSTMENT RESISTORS ARE 10% CARBON COMP.
ALL TRIMMING POTS ARE 100 ppm/°C CERMET TYPE.
SUPPLY BYPASS CAPACITORS ARE CERAMIC OR TANTALUM.
$C_{INT}$ IS 10% GLASS OR CERAMIC CAPACITATOR.




*33 pF FOR ADC-ET8BC

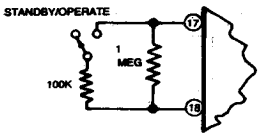
### CONNECTION FOR BIPOLAR OPERATION

$R_{IN}$, $R_{REF}$ ARE 1% METAL FILM RESISTORS.
$R_{BIAS}$, $R_C$ ARE 10% CARBON COMP RESISTORS.
$C_C$ is 20% CERAMIC CAPACITOR.
ZERO ADJUSTMENT RESISTORS ARE 10% CARBON COMP.
ALL TRIMMING POTS ARE 100 ppm/°C CERMET TYPE.
SUPPLY BYPASS CAPACITORS ARE CERAMIC OR TANTALUM.
$C_{INT}$ IS 10% GLASS OR CERAMIC CAPACITATOR.



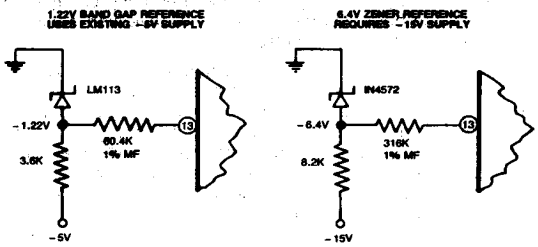

*33 pF FOR ADC-ET8BC

### REDUCTION OF STAND-BY POWER




THIS REDUCES POWER CONSUMPTION TO ABOUT 200 µA DURING STANDBY.

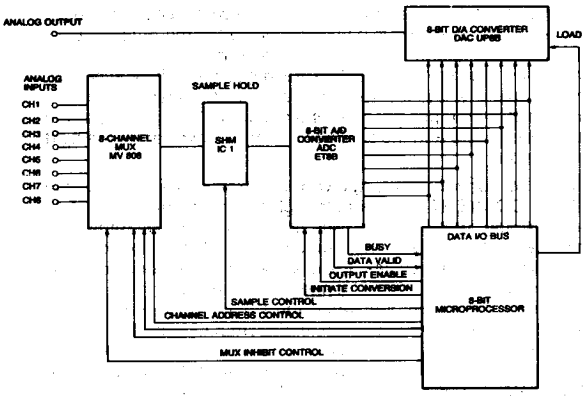
### REFERENCE CIRCUITS




### CALIBRATION PROCEDURE

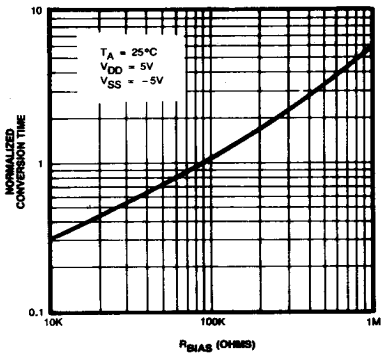
1. Connect the converter as shown in the connection diagrams for either unipolar or bipolar operation. Determine the input voltage range and select the required input resistors. Apply a logic high to the start convert input (pin 21) to give free-running operation.
2. **Zero and Offset Adjustments.** Apply a precision voltage reference source from the analog input resistor to ground. Adjust the reference source to zero + ½ LSB for unipolar operation or −FS + ½ LSB for bipolar operation. Adjust the zero or offset potentiometer so that the output code flickers between 000....000 and 000....001.
3. **Gain Adjustment.** Set the output of the reference source to +FS − 1½ LSB and adjust the gain trimming potentiometer so that the output code just flickers between 111....110 and 111....111.

### LOW COST MICROPROCESSOR A/D, D/A INTERFACE

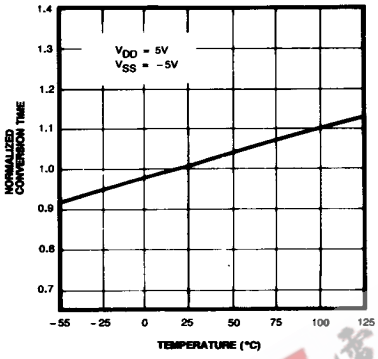


## TYPICAL PERFORMANCE CURVES

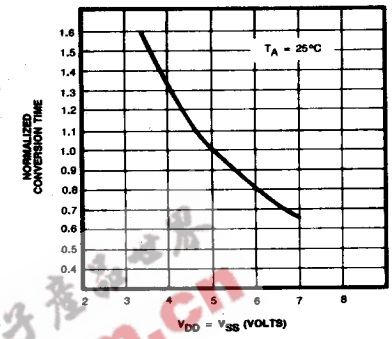
CONVERSION TIME VS. $R_{BIAS}$



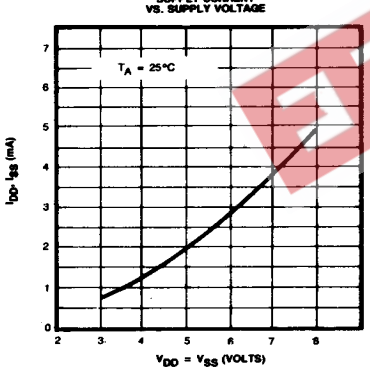

CONVERSION TIME VS. TEMPERATURE



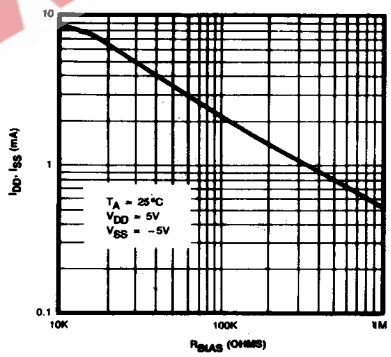

CONVERSION TIME VS. SUPPLY VOLTAGE



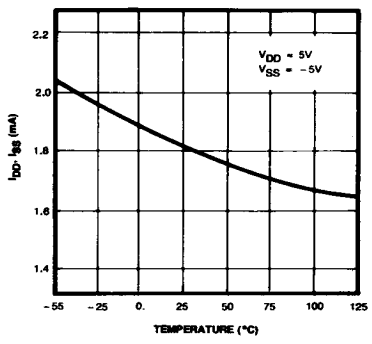

SUPPLY CURRENT VS. SUPPLY VOLTAGE



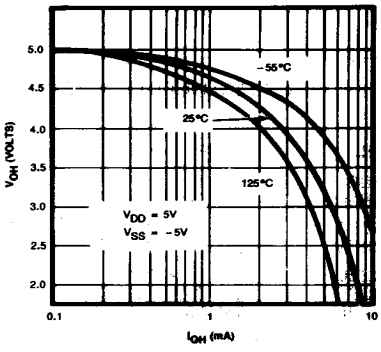

SUPPLY CURRENT VS. $R_{BIAS}$



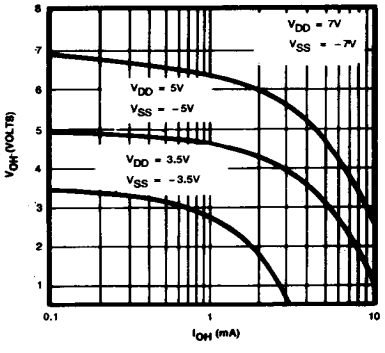

SUPPLY CURRENT VS. TEMPERATURE



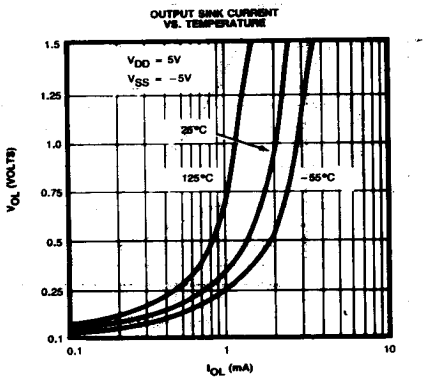

OUTPUT SOURCE CURRENT VS. TEMPERATURE

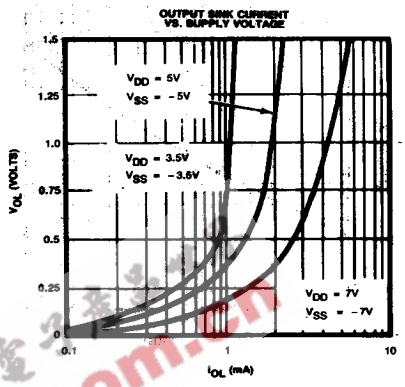


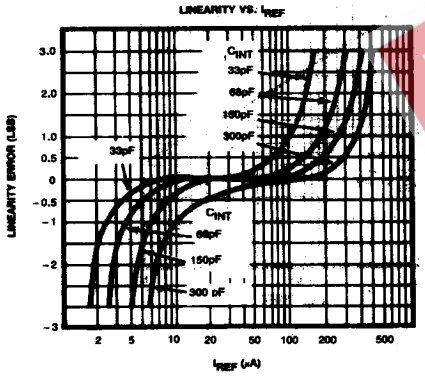

OUTPUT SOURCE CURRENT VS. SUPPLY VOLTAGE

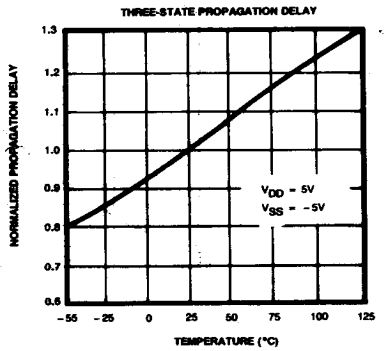


## TYPICAL PERFORMANCE CURVES




### ORDERING INFORMATION

| MODEL | OPERATING TEMP. RANGE | PACKAGE |
|---|---|---|
| ADC-ET8BC | 0°C to +70°C | Plastic |
| ADC-ET8BM | −55°C to +125°C | Cerdip |
| ADC-ET10BC | 0°C to +70°C | Plastic |
| ADC-ET10BM | −55°C to +125°C | Cerdip |
| ADC-ET12BC | 0°C to +70°C | Plastic |
| ADC-ET12BR | −25°C to +85°C | Ceramic |
| ADC-ET12BM | −55°C to +125°C | Ceramic |