# High Precision Shunt Mode Voltage References

# ADR520/ADR525/ADR530/ADR540/ADR550

## FEATURES

**Ultracompact SC70 and SOT-23 packages**
**Temperature coefficient: 40 ppm/°C (max)**
**2× the tempco improvement over the LM4040**
**Pin compatible with LM4040/LM4050**
**Initial accuracy: ±0.2%**
**Low output voltage noise: 14 µV p-p @ 2.5 V output**
**No external capacitor required**
**Operating current range: 50 µA to 10 mA**
**Industrial temperature range: −40°C to +85°C**

## APPLICATIONS

**Portable, battery-powered equipment**
**Automotive**
**Power supplies**
**Data acquisition systems**
**Instrumentation and process control**
**Energy measurement**

Table 1. Selection Guide

| Part | Voltage (V) | Initial Accuracy (%) | Temperature Coeffecient (ppm/°C) |
|---|---|---|---|
| ADR520A | 2.048 | ±0.4 | 70 |
| ADR520B | 2.048 | ±0.2 | 40 |
| ADR525A | 2.5 | ±0.4 | 70 |
| ADR525B | 2.5 | ±0.2 | 40 |
| ADR530A | 3.0 | ±0.4 | 70 |
| ADR530B | 3.0 | ±0.2 | 40 |
| ADR540A | 4.096 | ±0.4 | 70 |
| ADR540B | 4.096 | ±0.2 | 40 |
| ADR550A | 5.0 | ±0.4 | 70 |
| ADR550B | 5.0 | ±0.2 | 40 |

## PIN CONFIGURATION

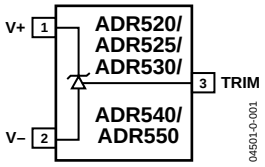


*Figure 1. 3-Lead SC70 (KS) and 3-Lead SOT-23 (RT)*

## GENERAL DESCRIPTION

Designed for space-critical applications, the ADR520/ADR525/ADR530/ADR540/ADR550 are high precision shunt voltage references, housed in ultrasmall SC70 and SOT-23 packages. These references feature low temperature drift of 40 ppm/°C, an initial accuracy of better than 0.2%, and ultralow output noise of 14 µV p-p.

Available in output voltages of 2.048 V, 2.5 V, 3.0 V, 4.096 V, and 5.0 V, the ADR5xx's advanced design eliminates the need for compensation by an external capacitor, yet the references are stable with any capacitive load. The minimum operating current increases from a mere 50 µA to a maximum of 10 mA. This low operating current and ease of use make these references ideally suited for handheld, battery-powered applications.

A TRIM terminal is available on the ADR5xx to allow adjustment of the output voltage over a ±0.5% range, without affecting the temperature coefficient of the device. This feature provides users with the flexibility to trim out any system errors.



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## REVISION HISTORY

11/03—Revision 0: Initial Version

12/03—Data Sheet Changed from REV. 0 to REV. A

Updated Outline Dimensions ..... 13
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# SPECIFICATIONS

**Table 2. ADR520 Electrical Characteristics @ $I_{IN}$ = 50 µA to 10 mA, $T_A$ = 25°C, unless otherwise noted**

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output Voltage | $V_O$ | | | | | |
| Grade A | | | 2.040 | 2.048 | 2.056 | V |
| Grade B | | | 2.044 | 2.048 | 2.052 | V |
| Initial Accuracy | $V_{OERR}$ | | | | | |
| Grade A | | ±0.4% | −8 | | +8 | mV |
| Grade B | | ±0.2% | −4 | | +4 | mV |
| Temperature Coefficient[1] | $TCV_O$ | −40°C < $T_A$ < +85°C | | | | |
| Grade A | | | | 25 | 70 | ppm/°C |
| Grade B | | | | 15 | 40 | ppm/°C |
| Output Voltage Change vs. $I_{IN}$ | $\Delta V_R$ | $I_{IN}$ = 0.1 mA to 10 mA | | | 1 | mV |
| | | −40°C < $T_A$ < +85°C | | | 4 | mV |
| | | $I_{IN}$ = 1 mA to 10 mA | | | | |
| | | −40°C < $T_A$ < +85°C | | | 2 | mV |
| Dynamic Output Impedance | $(\Delta V_R/\Delta I_R)$ | $I_{IN}$ = 0.1 mA to10 mA | | | 0.27 | Ω |
| Minimum Operating Current | $I_{IN}$ | −40°C < $T_A$ < +85°C | 50 | | | µA |
| Voltage Noise | $e_{N\ p\text{-}p}$ | 0.1 Hz to 10 Hz | | 14 | | µV p-p |
| Turn-On Settling Time | $t_R$ | | | 2 | | µs |
| Output Voltage Hysteresis | $\Delta V_{O\_HYS}$ | $I_{IN}$ = 1 mA | | 40 | | ppm |

[1]Guaranteed by design

**Table 3. ADR525 Electrical Characteristics @ $I_{IN}$ = 50 µA to 10 mA, $T_A$ = 25°C, unless otherwise noted**

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output Voltage | $V_O$ | | | | | |
| Grade A | | | 2.490 | 2.500 | 2.510 | V |
| Grade B | | | 2.495 | 2.500 | 2.505 | V |
| Initial Accuracy | $V_{OERR}$ | | | | | |
| Grade A | | ±0.4% | −10 | | +10 | mV |
| Grade B | | ±0.2% | −5 | | +5 | mV |
| Temperature Coefficient[1] | $TCV_O$ | −40°C < $T_A$ < +85°C | | | | |
| Grade A | | | | 25 | 70 | ppm/°C |
| Grade B | | | | 15 | 40 | ppm/°C |
| Output Voltage Change vs. $I_{IN}$ | $\Delta V_R$ | $I_{IN}$ = 0.1 mA to 10 mA | | | 1 | mV |
| | | −40°C < $T_A$ < +85°C | | | 4 | mV |
| | | $I_{IN}$ = 1 mA to 10 mA | | | | |
| | | −40°C < $T_A$ < +85°C | | | 2 | mV |
| Dynamic Output Impedance | $(\Delta V_R/\Delta I_R)$ | $I_{IN}$ = 0.1 mA to 10 mA | | | 0.2 | Ω |
| Minimum Operating Current | $I_{IN}$ | −40°C < $T_A$ < +85°C | 50 | | | µA |
| Voltage Noise | $e_{N\ p\text{-}p}$ | 0.1 Hz to 10 Hz | | 14 | | µV p-p |
| Turn-On Settling Time | $t_R$ | | | 2 | | µs |
| Output Voltage Hysteresis | $\Delta V_{O\_HYS}$ | $I_{IN}$ = 1 mA | | 40 | | ppm |

[1] Guaranteed by design

**Table 4. ADR530 Electrical Characteristics @ $I_{IN}$ = 50 µA to 10 mA, $T_A$ = 25°C, unless otherwise noted**

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output Voltage | $V_O$ | | | | | |
| Grade A | | | 2.988 | 3.000 | 3.012 | V |
| Grade B | | | 2.994 | 3.000 | 3.006 | V |
| Initial Accuracy | $V_{OERR}$ | | | | | |
| Grade A | | ±0.4% | −12 | | +12 | mV |
| Grade B | | ±0.2% | −6 | | +6 | mV |
| Temperature Coefficient[1] | $TCV_O$ | −40°C < $T_A$ < +85°C | | | | |
| Grade A | | | | 25 | 70 | ppm/°C |
| Grade B | | | | 15 | 40 | ppm/°C |
| Output Voltage Change vs. $I_{IN}$ | $\Delta V_R$ | $I_{IN}$ = 0.1 mA to 10 mA | | | 1 | mV |
| | | −40°C < $T_A$ < +85°C | | | 4 | mV |
| | | $I_{IN}$ = 1 mA to 10 mA | | | | |
| | | −40°C < $T_A$ < +85°C | | | 2 | mV |
| Dynamic Output Impedance | $(\Delta V_R/\Delta I_R)$ | $I_{IN}$ = 0.1 mA to 10 mA | | | 0.2 | Ω |
| Minimum Operating Current | $I_{IN}$ | −40°C < $T_A$ < +85°C | 50 | | | µA |
| Voltage Noise | $e_{N\ p\text{-}p}$ | 0.1 Hz to 10 Hz | | 16 | | µV p-p |
| Turn-On Settling Time | $t_R$ | | | 2 | | µs |
| Output Voltage Hysteresis | $\Delta V_{O\_HYS}$ | $I_{IN}$ = 1 mA | | 40 | | ppm |

[1]Guaranteed by design

**Table 5. ADR540 Electrical Characteristics @ $I_{IN}$ = 50 µA to 10 mA, $T_A$ = 25°C, unless otherwise noted**

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output Voltage | $V_O$ | | | | | |
| Grade A | | | 4.08 | 4.096 | 4.112 | V |
| Grade B | | | 4.088 | 4.096 | 4.104 | V |
| Initial Accuracy | $V_{OERR}$ | | | | | |
| Grade A | | ±0.4% | −16 | | +16 | mV |
| Grade B | | ±0.2% | −8 | | +8 | mV |
| Temperature Coefficient[1] | $TCV_O$ | −40°C < $T_A$ < +85°C | | | | |
| Grade A | | | | 25 | 70 | ppm/°C |
| Grade B | | | | 15 | 40 | ppm/°C |
| Output Voltage Change vs. $I_{IN}$ | $\Delta V_R$ | $I_{IN}$ = 0.1 mA to 10 mA | | | 1 | mV |
| | | −40°C < $T_A$ < +85°C | | | 5 | mV |
| | | $I_{IN}$ = 1 mA to 10 mA | | | | |
| | | −40°C < $T_A$ < +85°C | | | 2 | mV |
| Dynamic Output Impedance | $(\Delta V_R/\Delta I_R)$ | $I_{IN}$ = 0.1 mA to 10 mA | | | 0.2 | Ω |
| Minimum Operating Current | $I_{IN}$ | −40°C < $T_A$ < +85°C | 50 | | | µA |
| Voltage Noise | $e_{N\ p\text{-}p}$ | 0.1 Hz to 10 Hz | | 18 | | µV p-p |
| Turn-On Settling Time | $t_R$ | | | 2 | | µs |
| Output Voltage Hysteresis | $\Delta V_{O\_HYS}$ | $I_{IN}$ = 1 mA | | 40 | | ppm |

[1]Guaranteed by design

**Table 6. ADR550 Electrical Characteristics @ $I_{IN}$ = 50 µA to 10 mA, $T_A$ = 25°C, unless otherwise noted**

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output Voltage | $V_O$ | | | | | |
| Grade A | | | 4.980 | 5.000 | 5.020 | V |
| Grade B | | | 4.090 | 5.000 | 5.010 | V |
| Initial Accuracy | $V_{OERR}$ | | | | | |
| Grade A | | ±0.4% | −20 | | +20 | mV |
| Grade B | | ±0.2% | −10 | | +10 | mV |
| Temperature Coefficient[1] | $TCV_O$ | −40°C < $T_A$ < +85°C | | | | |
| Grade A | | | | 25 | 70 | ppm/°C |
| Grade B | | | | 15 | 40 | ppm/°C |
| Output Voltage Change vs. $I_{IN}$ | $\Delta V_R$ | $I_{IN}$ = 0.1 mA to 10 mA | | | 1 | mV |
| | | −40°C < $T_A$ < +85°C | | | 5 | mV |
| | | $I_{IN}$ = 1 mA to 10 mA | | | | |
| | | −40°C < $T_A$ < +85°C | | | 2 | mV |
| Dynamic Output Impedance | $(\Delta V_R/\Delta I_R)$ | $I_{IN}$ = 0.1 mA to 10 mA | | | 0.2 | Ω |
| Minimum Operating Current | $I_{IN}$ | −40°C < $T_A$ < +85°C | 50 | | | µA |
| Voltage Noise | $e_{N\ p\text{-}p}$ | 0.1 Hz to 10 Hz | | 18 | | µV p-p |
| Turn-On Settling Time | $t_R$ | | | 2 | | µs |
| Output Voltage Hysteresis | $\Delta V_{O\_HYS}$ | $I_{IN}$ = 1 mA | | 40 | | ppm |

[1]Guaranteed by design

# ABSOLUTE MAXIMUM RATINGS

Ratings apply at 25°C, unless otherwise noted.

**Table 7.**

| Parameter | Rating |
|---|---|
| Reverse Current | 25 mA |
| Forward Current | 20 mA |
| Storage Temperature Range | –65°C to +150°C |
| Industrial Temperature Range | –40°C to +85°C |
| Junction Temperature Range | –65°C to +150°C |
| Lead Temperature Range (Soldering, 60 sec) | 300°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

| Package Type | $\theta_{JA}$[1] | $\theta_{JC}$ | Unit |
|---|---|---|---|
| 3-Lead SC70 (KS) | 376 | | °C/W |
| 3-Lead SOT-23 (RT) | 230 | 146 | °C/W |

[1] $\theta_{JA}$ is specified for worst-case conditions, i.e., $\theta_{JA}$ is specified for devices soldered on circuit boards for surface-mount packages. Contact factory for latest information on release dates.



## ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

# PARAMETER DEFINITIONS

## TEMPERATURE COEFFICIENT

*Temperature coefficient* is defined as the change in output voltage with respect to operating temperature changes, and is normalized by an output voltage of 25°C. This parameter is expressed in ppm/°C, and is determined by the following equation:

$$TCV_O\left[\frac{ppm}{°C}\right] = \frac{V_O(T_2) - V_O(T_1)}{V_O(25°C) \times (T_2 - T_1)} \times 10^6 \quad (1)$$

where:

$V_O$(25°C) = $V_O$ at 25°C.

$V_O(T_1)$ = $V_O$ at Temperature 1.

$V_O(T_2)$ = $V_O$ at Temperature 2.

## THERMAL HYSTERESIS

*Thermal hysteresis* is defined as the change in output voltage after the device is cycled through temperatures ranging from +25°C to −40°C, then to +85°C, and back to +25°C. The following equation expresses a typical value from a sample of parts put through such a cycle:

$$V_{O\_HYS} = V_O(25°C) - V_{O\_TC}$$
$$V_{O\_HYS}[ppm] = \frac{V_O(25°C) - V_{O\_TC}}{V_O(25°C)} \times 10^6 \quad (2)$$

where:

$V_O$(25°C) = $V_O$ at 25°C.

$V_{O\_TC}$ = $V_O$ at 25°C after a temperature cycle from +25°C to −40°C, then to +85°C, and back to +25°C.

# TYPICAL PERFORMANCE CHARACTERISTICS

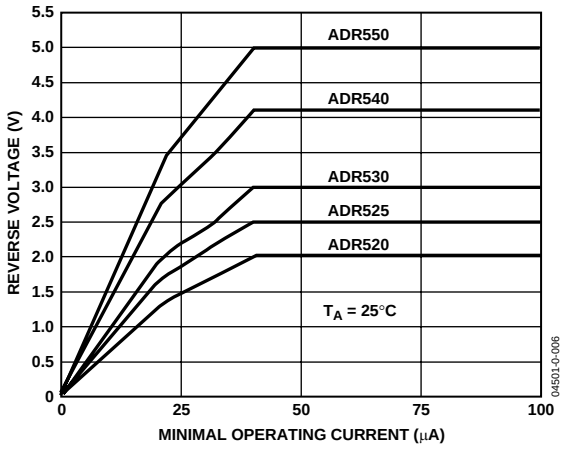


Figure 2. Reverse Characteristics and Minimum Operating Current

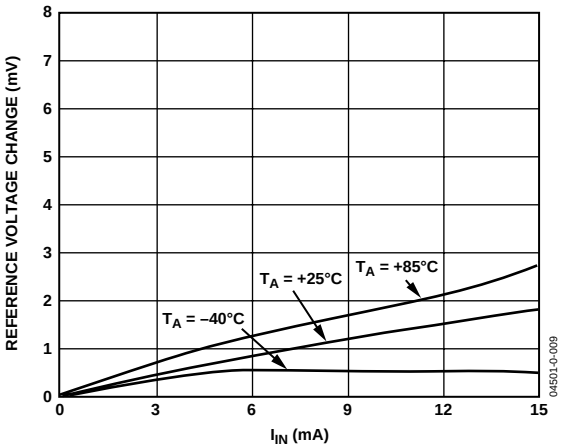


Figure 5. ADR550 Reverse Voltage vs. Operating Current

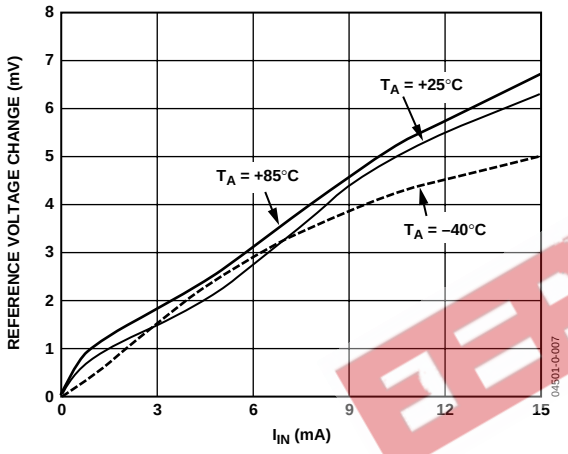


Figure 3. ADR520 Reverse Voltage vs. Operating Current

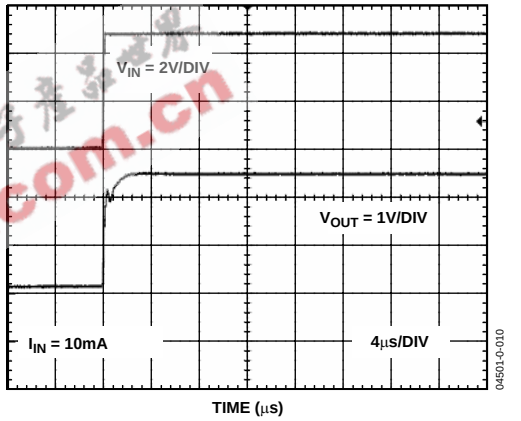


Figure 6. ADR525 Turn-On Response

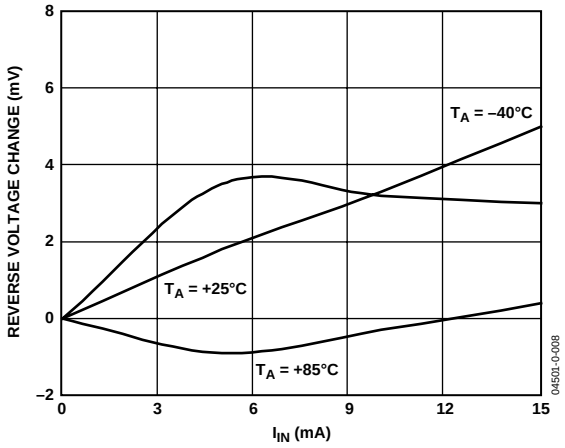


Figure 4. ADR525 Reverse Voltage vs. Operating Current

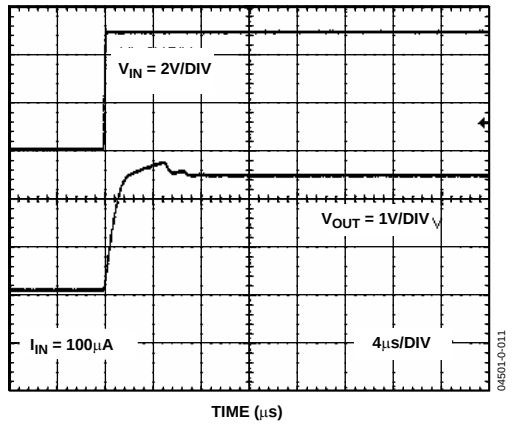


Figure 7. ADR525 Turn-On Response

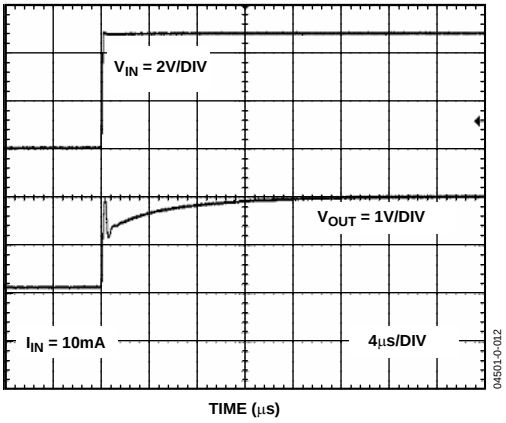


Figure 8. ADR520 Turn-On Response

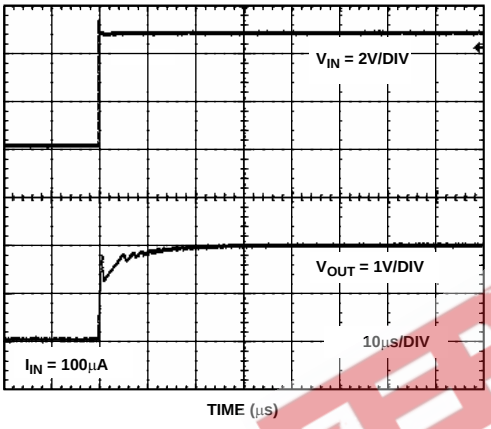


Figure 9. ADR520 Turn-On Response

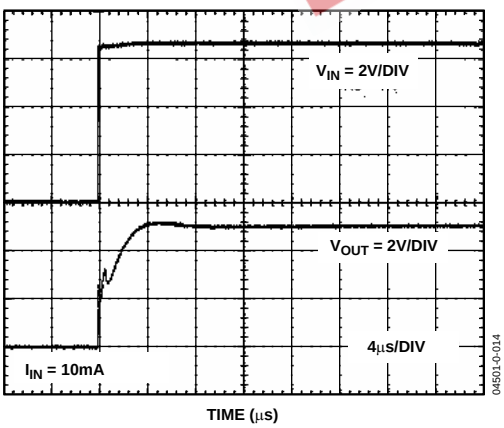


Figure 10. ADR550 Turn-On Response

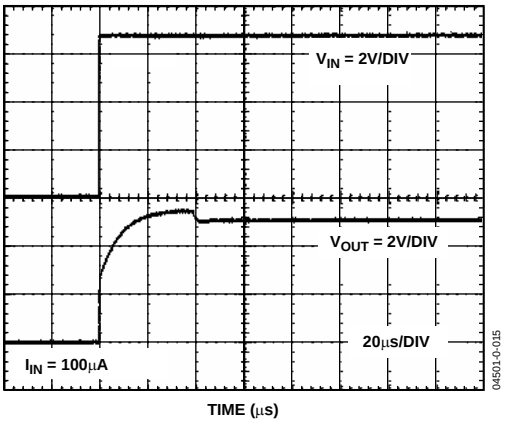


Figure 11. ADR550 Turn-On Response

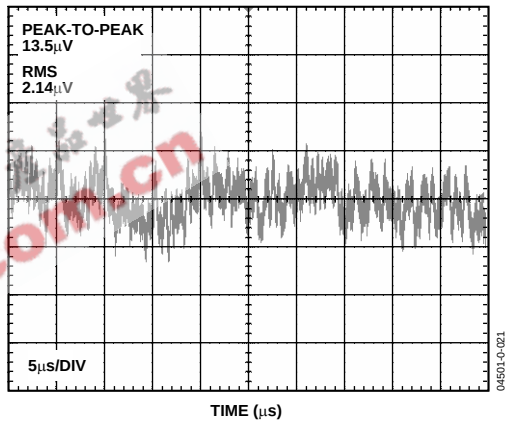


Figure 12. ADR520 Noise Voltage 0.1 Hz to 10 Hz

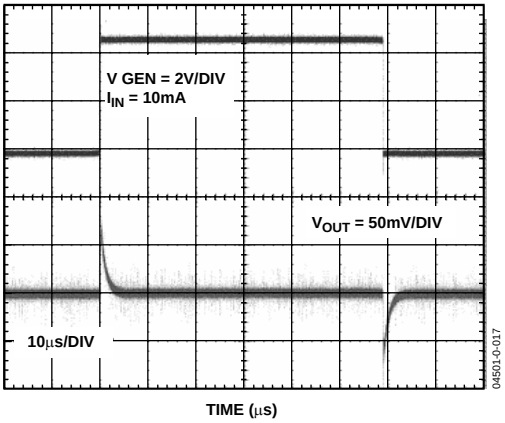


Figure 13. ADR525 Load Transient Response

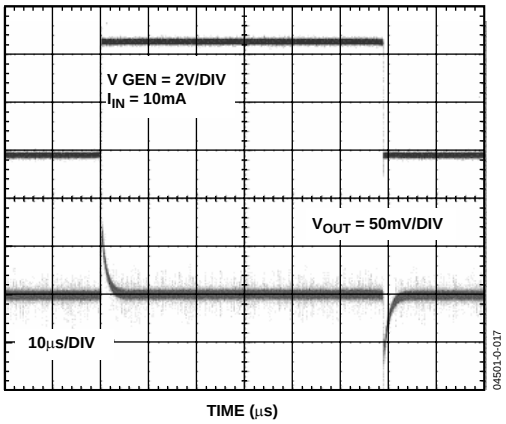


Figure 14. ADR550 Load Transient Response

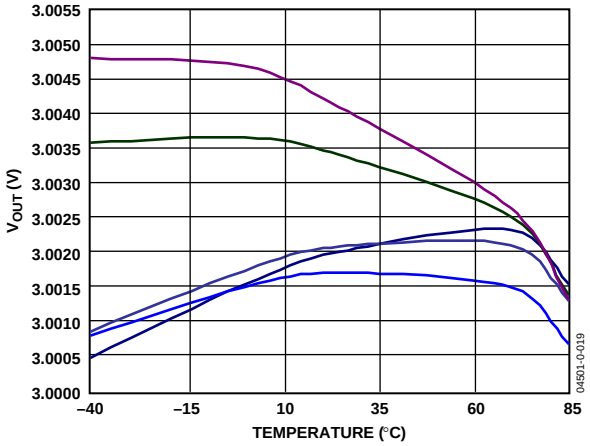


Figure 16. ADR530 $V_{OUT}$ over Temperature

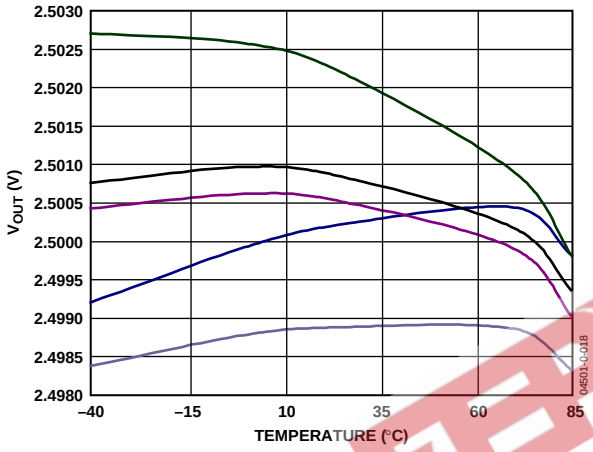


Figure 15. ADR525 $V_{OUT}$ over Temperature

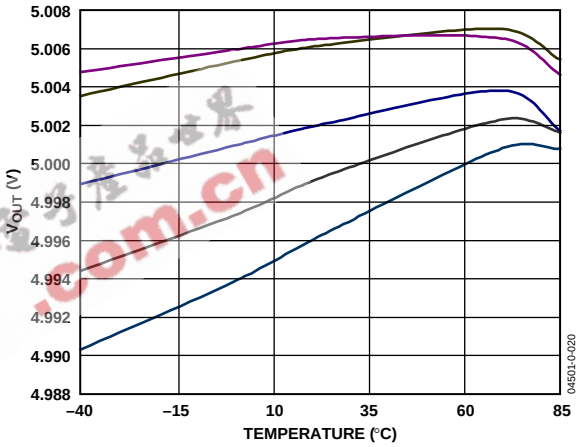


Figure 17. ADR550 $V_{OUT}$ over Temperature

# THEORY OF OPERATION

The ADR520/ADR525/ADR530/ADR540/ADR550 use the band gap concept to produce a stable, low temperature coefficient voltage reference suitable for high accuracy data acquisition components and systems. The devices use the physical nature of a silicon transistor base-emitter voltage in the forward-biased operating region. All such transistors have approximately a –2 mV/°C temperature coefficient (TC), making them unsuitable for direct use as a low temperature coefficient reference. Extrapolation of the temperature characteristic of any one of these devices to absolute zero (with the collector current proportional to the absolute temperature), however, reveals that its $V_{BE}$ approaches approximately the silicon band gap voltage. Thus, if a voltage develops with an opposing temperature coefficient to sum the $V_{BE}$, a zero temperature coefficient reference results. The ADR5xx circuit shown in Figure 18 provides such a compensating voltage (V1) by driving two transistors at different current densities and amplifying the resultant $V_{BE}$ difference ($\Delta V_{BE}$, which has a positive temperature coefficient). The sum of $V_{BE}$ and V1 provides a stable voltage reference over temperature.

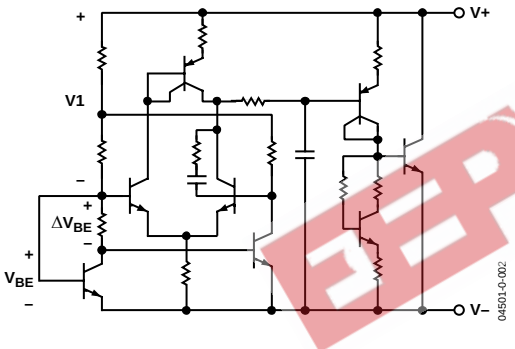


*Figure 18. Circuit Schematic*

## APPLICATIONS

The ADR520/ADR525/ADR530/ADR540/ADR550 are a series of precision shunt voltage references. They are designed to operate without an external capacitor between the positive and negative terminals. If a bypass capacitor is used to filter the supply, the references remains stable.

All shunt voltage references require an external bias resistor ($R_{BIAS}$) between the supply voltage and the reference (see Figure 19). The $R_{BIAS}$ sets the current that flows through the load ($I_L$) and the reference ($I_{IN}$). Because the load and the supply voltage can vary, the $R_{BIAS}$ needs to be chosen based on the following considerations:

- The $R_{BIAS}$ must be small enough to supply the minimum $I_{IN}$ current to the ADR5xx, even when the supply voltage is at its minimum value and the load current is at its maximum value.
- The $R_{BIAS}$ must be large enough so that $I_{IN}$ does not exceed 10 mA when the supply voltage is at its maximum value and the load current is at its minimum value.

Given these conditions, the $R_{BIAS}$ is determined by the supply voltage ($V_{CC}$), the ADR5xx load and operating current ($I_L$ and $I_Q$), and the ADR5xx output voltage ($V_{OUT}$).

$$R_{BIAS} = \frac{V_{CC} - V_{OUT}}{I_L - I_{IN}} \quad (3)$$

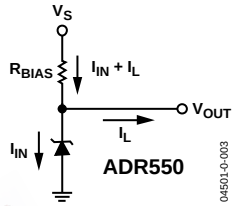


*Figure 19. Shunt Reference*

### Precision Negative Voltage Reference

The ADR5xx is suitable for applications where a precise negative voltage is desired. Figure 20 shows the ADR5xx configured to provide a negative output.

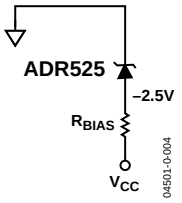


*Figure 20. Negative Precision Reference Configuration*

### Output Voltage Trim

The ADR5xx TRIM terminal can be used to adjust the output voltage over a range of ±0.5%. This allows systems designers to trim system errors by setting the reference to a voltage other than the preset output voltage. An external mechanical or electrical potentiometer can be used for this adjustment. Figure 21 illustrates how the output voltage can be trimmed by using the AD5273, an Analog Devices 10 kΩ potentiometer.

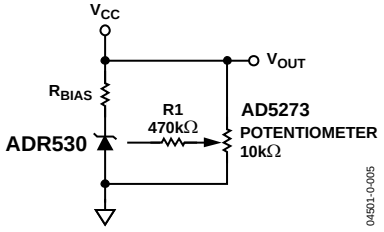


*Figure 21. Output Voltage Trim*

### *Stacking ADR5xx for User-Definable Outputs*

Multiple ADR5xx parts can be stacked together to allow the user to obtain a desired higher voltage. Figure 22a shows three ADR550s configured to give 15 V. The bias resistor, $R_{BIAS}$, is chosen using Equation 3, noting that the same bias current will flow through all the shunt references in series. Figure 22b shows three ADR550s stacked together to give –15 V. $R_{BIAS}$ is calculated in the same manner as before. Parts of different voltages can also be added together, i.e., an ADR525 and an ADR550 can be added together to give an output of +7.5 V or –7.5 V, as desired. Note, however, that the initial accuracy error is now the sum of the errors of all the stacked parts, as are the tempco and output voltage change versus input current.

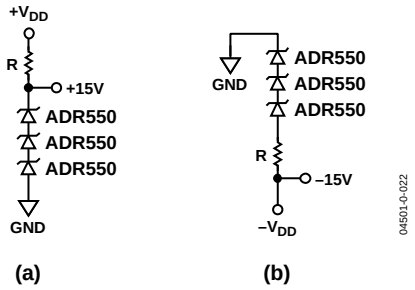


*Figure 22. 15 V Output with Stacked ADR550s*

### *Adjustable Precision Voltage Source*

The ADR5xx, combined with a precision low input bias op amp, such as the AD8610, can be used to output a precise adjustable voltage. Figure 23 illustrates the implementation of this application using the ADR5xx. The output of the op amp, $V_{OUT}$, is determined by the gain of the circuit, which is completely dependant on the resistors, *R1* and *R2*.

$$V_{OUT} = (1 + R2/R1)V_{REF}$$

An additional capacitor, C1, in parallel with R2, can be added to filter out high frequency noise. The value of C1 is dependent on the value of R2.

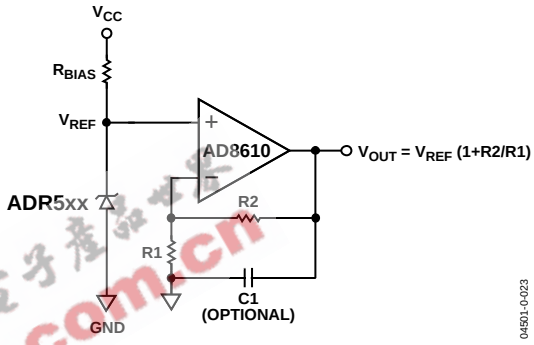


*Figure 23. Adjustable Voltage Source*

# OUTLINE DIMENSIONS

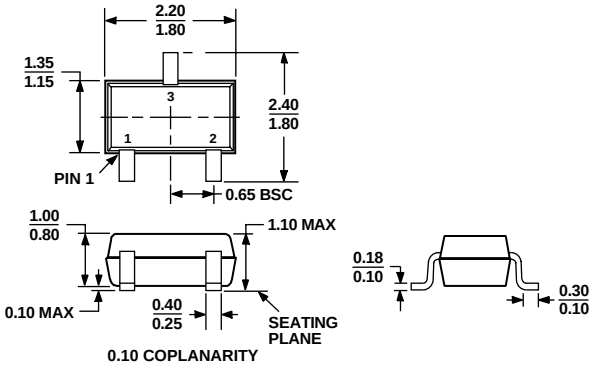


*Figure 24. Surface-Mount Package [SC70]*
*(KS-3)*
*Dimensions shown in millimeters*

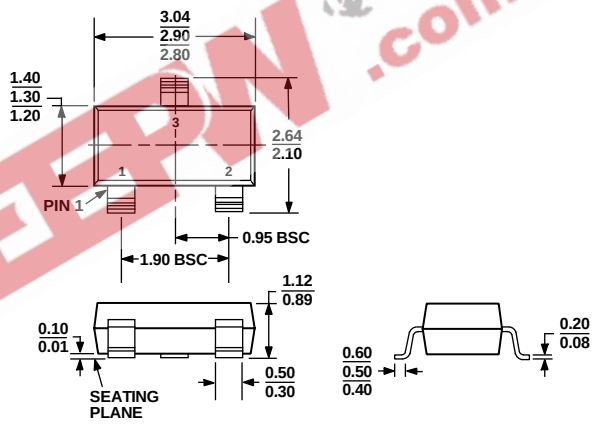


*Figure 25. Surface-Mount Package[SOT-23]*
*(RT-3)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model | Output Voltage (V) | Initial Accuracy (mV) | Tempco Industrial (ppm/°C) | Package Description | Package Option | Branding | Number of Parts per Reel | Temperature Range (°C) |
|---|---|---|---|---|---|---|---|---|
| ADR520ART-REEL7 | 2.048 | 8 | 70 | SOT-23 | RT | RQA | 3,000 | –40 to +85 |
| ADR520ART-R2 | 2.048 | 8 | 70 | SOT-23 | RT | RQA | 250 | –40 to +85 |
| ADR520BRT-REEL7 | 2.048 | 4 | 40 | SOT-23 | RT | RQB | 3,000 | –40 to +85 |
| ADR520BRT-R2 | 2.048 | 4 | 40 | SOT-23 | RT | RQB | 250 | –40 to +85 |
| ADR520BKS-REEL7 | 2.048 | 4 | 40 | SC70 | KS | RQB | 3,000 | –40 to +85 |
| ADR520BKS-R2 | 2.048 | 4 | 40 | SC70 | KS | RQB | 250 | –40 to +85 |
| ADR525ART-REEL7 | 2.500 | 10 | 70 | SOT-23 | RT | RRA | 3,000 | –40 to +85 |
| ADR525ART-R2 | 2.500 | 10 | 70 | SOT-23 | RT | RRA | 250 | –40 to +85 |
| ADR525BRT-REEL7 | 2.500 | 5 | 40 | SOT-23 | RT | RRB | 3,000 | –40 to +85 |
| ADR525BRT-R2 | 2.500 | 5 | 40 | SOT-23 | RT | RRB | 250 | –40 to +85 |
| ADR525BKS-REEL7 | 2.500 | 5 | 40 | SC70 | KS | RRB | 3,000 | –40 to +85 |
| ADR525BKS-R2 | 2.500 | 5 | 40 | SC70 | KS | RRB | 250 | –40 to +85 |
| ADR530ART-REEL7 | 3.0 | 12 | 70 | SOT-23 | RT | RSA | 3,000 | –40 to +85 |
| ADR530ART-R2 | 3.0 | 12 | 70 | SOT-23 | RT | RSA | 250 | –40 to +85 |
| ADR530BRT-REEL7 | 3.0 | 6 | 40 | SOT-23 | RT | RSB | 3,000 | –40 to +85 |
| ADR530BRT-R2 | 3.0 | 6 | 40 | SOT-23 | RT | RSB | 250 | –40 to +85 |
| ADR530BKS-REEL7 | 3.0 | 6 | 40 | SC70 | KS | RSB | 3,000 | –40 to +85 |
| ADR530BKS-R2 | 3.0 | 6 | 40 | SC70 | KS | RSB | 250 | –40 to +85 |
| ADR540ART-REEL7 | 4.096 | 16 | 70 | SOT-23 | RT | RTA | 3,000 | –40 to +85 |
| ADR540ART-R2 | 4.096 | 16 | 70 | SOT-23 | RT | RTA | 250 | –40 to +85 |
| ADR540BRT-REEL7 | 4.096 | 8 | 40 | SOT-23 | RT | RTB | 3,000 | –40 to +85 |
| ADR540BRT-R2 | 4.096 | 8 | 40 | SOT-23 | RT | RTB | 250 | –40 to +85 |
| ADR540BKS-REEL7 | 4.096 | 8 | 40 | SC70 | KS | RTB | 3,000 | –40 to +85 |
| ADR540BKS-R2 | 4.096 | 8 | 40 | SC70 | KS | RTB | 250 | –40 to +85 |
| ADR550ART-REEL7 | 5.0 | 20 | 70 | SOT-23 | RT | RVA | 3,000 | –40 to +85 |
| ADR550ART-R2 | 5.0 | 20 | 70 | SOT-23 | RT | RVA | 250 | –40 to +85 |
| ADR550BRT-REEL7 | 5.0 | 10 | 40 | SOT-23 | RT | RVB | 3,000 | –40 to +85 |
| ADR550BRT-R2 | 5.0 | 10 | 40 | SOT-23 | RT | RVB | 250 | –40 to +85 |
| ADR550BKS-REEL7 | 5.0 | 10 | 40 | SC70 | KS | RVB | 3,000 | –40 to +85 |
| ADR550BKS-R2 | 5.0 | 10 | 40 | SC70 | KS | RVB | 250 | –40 to +85 |

## NOTES

## NOTES


C04501–0–12/03(A)