Quad Voltage Up and Down Sequencer and Monitor with Programmable Timing

ADM1186

FEATURES

- Powered from 2.7 V to 5.5 V on the VCC pin
- Monitors four supplies via 0.8% accurate comparators
- Digital core supports up and down supply sequencing
- Multiple devices can be cascaded (ADM1186-1)
- Four inputs can be programmed to monitor different voltage levels with resistor dividers
- Capacitor programmable supply sequence time delays and a timeout delay to 5% accuracy at 25°C
- Four open-drain enable outputs
- Open-drain power-good output
- Open-drain sequence complete pin and bidirectional open-drain fault pin (ADM1186-1 only)

APPLICATIONS

- Monitor and alarm functions
- Up and down power supply sequencing
- Telecommunication and data communication equipment
- PCs, servers, and notebook PCs

GENERAL DESCRIPTION

The ADM1186-1 and ADM1186-2 are integrated, four-channel voltage monitoring and sequencing devices. A 2.7 V to 5.5 V power supply is required on the VCC pin for power.

Four precision comparators, VIN1 to VIN4, monitor four voltage rails. All four comparators share a 0.6 V reference and have a worst-case accuracy of 0.8%. Resistor networks that are external to the VIN1, VIN2, VIN3, and VIN4 pins set the undervoltage (UV) trip points for the monitored supply rails.

The ADM1186-1 and ADM1186-2 have four open-drain enable outputs, OUT1 to OUT4, that are used to enable power supplies. An open-drain power-good output, PWRGD, indicates whether the four VINx inputs are above their UV thresholds.

A state machine monitors the state of the UP and $\overline{\text{DOWN}}$ pins on the ADM1186-1 or the UP/$\overline{\text{DOWN}}$ pin on the ADM1186-2 to control the supply sequencing direction (see Figure 2). In the WAIT START state, a rising edge transition on the UP or UP/$\overline{\text{DOWN}}$ pin triggers a power-up sequence. A falling edge transition on the $\overline{\text{DOWN}}$ or UP/$\overline{\text{DOWN}}$ pin in the POWER-UP DONE state triggers a power-down sequence.

APPLICATION DIAGRAM

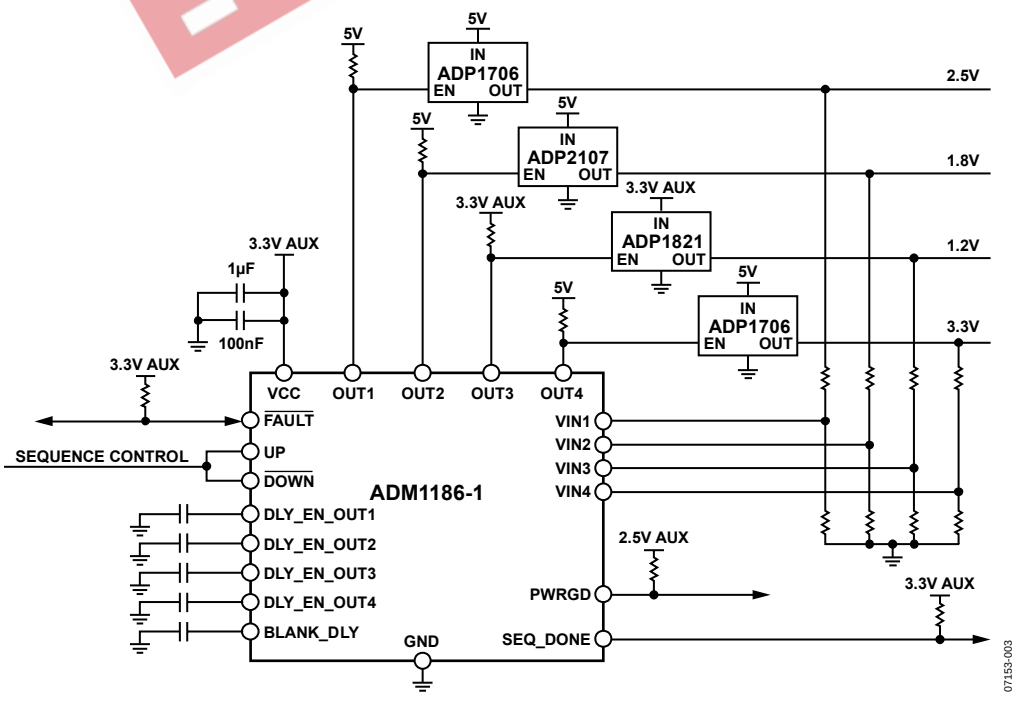

Figure 1.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113

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REVISION HISTORY

5/08—Revision 0: Initial Version

During a power-up sequence, the state machine enables each power supply in turn. The supply output voltage is monitored to determine whether it rises above the UV threshold level within a user defined duration called the blanking time. If a supply rises above the UV threshold, the next enable output in the sequence is turned on. In addition to the blanking time, the user can also define a sequence time delay before each enable output is turned on.

The ADM1186-1 provides an open-drain pin, SEQ_DONE, that is asserted high to provide an indication that a power-up sequence is complete. The SEQ_DONE pin allows multiple cascaded ADM1186-1 devices to perform controlled power-up and power-down sequences.

During a power-down sequence, the enable outputs turn off in reverse order. The same sequence time delays used during the power-up sequence are also used during the power-down sequence as each enable output is turned off; no blanking time is used during a power-down sequence. At the end of a power-down sequence, the SEQ_DONE pin is brought low.

During sequencing and when powered up, the state machine continuously monitors the part for any fault conditions. Faults include a UV condition on any of the inputs or an unexpected control input. Any fault causes the state machine to enter a fault handler, which immediately turns off all enable outputs and then ensures that the device is ready to start a new power-up sequence.

The ADM1186-1 has a bidirectional pin, $\overline{\text{FAULT}}$, that facilitates fault handling when using multiple devices. If an ADM1186-1 experiences a fault condition, the $\overline{\text{FAULT}}$ pin is driven low, causing other connected ADM1186-1 devices to enter their own fault handling states.

The ADM1186-1 is available in a 20-lead QSOP package, and the ADM1186-2 is available in a 16-lead QSOP package.

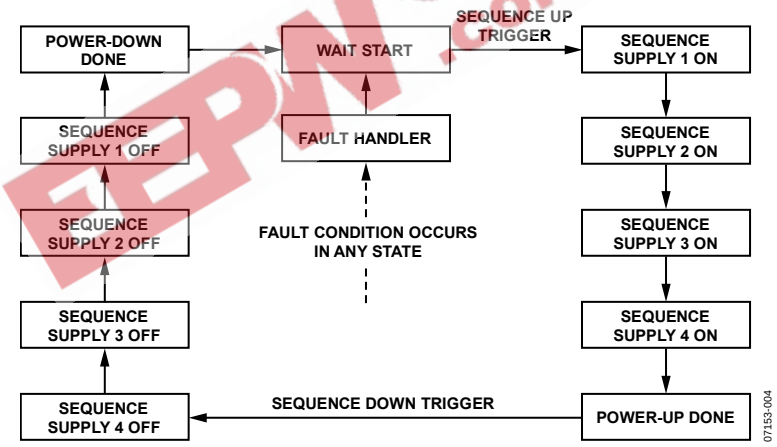


Figure 2. Simplified State Machine Diagram

SPECIFICATIONS

V_{VCC} = 2.7 V to 5.5 V, T_A = −40°C to +85°C; typical values at T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
VCC PIN					
Operating Voltage Range, V_{VCC}	2.7	3.3	5.5	V	
Undervoltage Lockout, V_{UVLO}		2.46		V	V_{VCC} falling
Undervoltage Lockout Hysteresis		50		mV	
Supply Current, I_{VCC}		146	210	µA	Steady state; sequence complete
VIN1 TO VIN4 (VINx) PINS					
Input Current	−25		+25	nA	V_{VINx} = 0 V to 1 V
	−100		+100	nA	V_{VINx} = 0 V to 5.5 V; V_{VINx} can be greater than V_{VCC}
Input Threshold[1]	0.5952	0.6000	0.6048	V	
Input Glitch Immunity					
Positive Glitch Duration	19.9	26.6	33.2	µs	50 mV input overdrive
Negative Glitch Duration	2.75	4.7	6.6	µs	50 mV input overdrive
UP, $\overline{DOWN}$, AND UP/$\overline{DOWN}$ PINS					
Input Current	−100		+100	nA	$V_{UP/\overline{DOWN}}$ = 0 V to 5.5 V; $V_{UP/\overline{DOWN}}$ can be greater than V_{VCC}
Input Threshold[1]	1.372	1.4	1.428	V	
Input Glitch Immunity	3.3	6.8	9.7	µs	100 mV input overdrive
	2.7	4.9	7.9	µs	1 V input overdrive
DLY_EN_OUTx AND BLANK_DLY PINS					
Time Delay Accuracy		5	9	%	External capacitor values of 10 nF to 2.2 µF; excludes external capacitor tolerance
Time Delay Charge Current		14		µA	
Time Delay Threshold		1.4		V	
Time Delay Discharge Resistor		450		Ω	
OUT1 TO OUT4 (OUTx) PINS					
Output Low Voltage, V_{OUTL}			0.4	V	V_{VCC} = 2.7 V, I_{SINK} = 2 mA
Leakage Current			1	µA	OUTx = 5.5 V
V_{VCC} That Guarantees Valid Outputs	1			V	Output is guaranteed to be either low (V_{OUTL} = 0.4 V) or giving a valid output level from V_{VCC} = 1 V, I_{SINK} = 30 µA or V_{VCC} = 1.1 V, I_{SINK} = 100 µA
PWRGD PIN					
Output Low Voltage, V_{PWRGDL}			0.4	V	V_{VCC} = 2.7 V, I_{SINK} = 2 mA
Leakage Current			1	µA	PWRGD = 5.5 V
V_{VCC} That Guarantees Valid Outputs	1			V	Output is guaranteed to be either low (V_{PWRGDL} = 0.4 V) or giving a valid output level from V_{VCC} = 1 V, I_{SINK} = 30 µA or V_{VCC} = 1.1 V, I_{SINK} = 100 µA
$\overline{FAULT}$ PIN					
Input Threshold[1]	1.372	1.4	1.428	V	
Input Glitch Immunity	3.1	5.6	8.1	µs	1 V input overdrive
Output Low Voltage, $V_{\overline{FAULTL}}$			0.4	V	V_{VCC} = 2.7 V, I_{SINK} = 2 mA
Leakage Current			1	µA	$\overline{FAULT}$ = 5.5 V
V_{VCC} That Guarantees Valid Outputs	1			V	Output is guaranteed to be either low ($V_{\overline{FAULTL}}$ = 0.4 V) or giving a valid output level from V_{VCC} = 1 V, I_{SINK} = 30 µA or V_{VCC} = 1.1 V, I_{SINK} = 100 µA

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SEQ_DONE PIN					
Output Low Voltage, V_{SEQ_DONEL}			0.4	V	V_{VCC} = 2.7 V, I_{SINK} = 2 mA
Leakage Current			1	µA	SEQ_DONE = 5.5 V
V_{VCC} That Guarantees Valid Outputs	1			V	Output is guaranteed to be either low (V_{SEQ_DONEL} = 0.4 V) or giving a valid output level from V_{VCC} = 1 V, I_{SINK} = 30 µA or V_{VCC} = 1.1 V, I_{SINK} = 100 µA
RESPONSE TIMING					Includes input glitch filter and all other internal delays
VINx to PWRGD					
VINx Going Low to High	21.9	28.8	35.2	µs	50 mV input overdrive
VINx Going High to Low	5.8	7.3	8.9	µs	50 mV input overdrive
VINx to $\overline{FAULT}$, OUTx Low					
VINx Going High to Low (UV Fault)	6.1	7.5	9.2	µs	50 mV input overdrive
UP, $\overline{DOWN}$, and UP/$\overline{DOWN}$ to $\overline{FAULT}$, OUTx Low, t_{UDOUT}	5.5	8.6	12.1	µs	100 mV input overdrive
	5.8	7.7	10.5	µs	1 V input overdrive
External $\overline{FAULT}$ to OUTx Low			10	µs	1 V input overdrive
Fault Hold Time	35	44	54	µs	UP, UP/$\overline{DOWN}$ held low

[1] Input comparators do not include hysteresis on their inputs. The comparator output passes through a digital glitch filter to remove short transients from the input signal that would otherwise drive the state machine.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Rating
VCC Pin	−0.3 V to +6 V
VINx Pins	−0.3 V to +6 V
UP, $\overline{\text{DOWN}}$, UP/$\overline{\text{DOWN}}$ Pins	−0.3 V to +6 V
DLY_EN_OUTx, BLANK_DLY Pins	−0.3 V to V_{CC} + 0.3 V
PWRGD, SEQ_DONE, OUTx Pins	−0.3 V to +6 V
$\overline{\text{FAULT}}$ Pin	−0.3 V to +6 V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Convection Reflow	
Peak Temperature	260°C
Time at Peak Temperature	≤30 sec
Junction Temperature	125°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Thermal Resistance

Package Type	θ_{JA}	Unit
16-Lead QSOP	149.97	°C/W
20-Lead QSOP	125.80	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

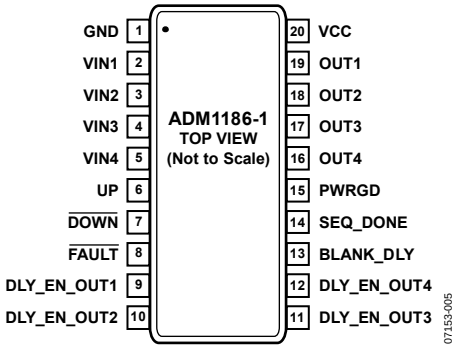


Figure 3. ADM1186-1 Pin Configuration

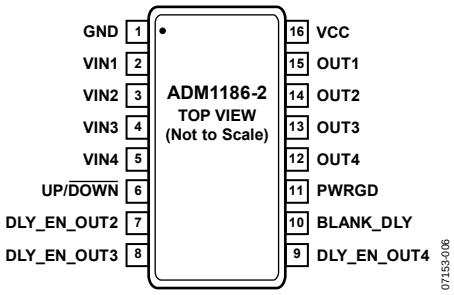


Figure 4. ADM1186-2 Pin Configuration

Table 4. Pin Function Descriptions

Pin No.			
ADM1186-1	**ADM1186-2**	**Mnemonic**	**Description**
1	1	GND	Chip Ground Pin.
2	2	VIN1	Noninverting Comparator Input. The voltage on this pin is compared with a 0.6 V reference. Can be used to monitor a voltage rail via a resistor divider. The output of this comparator is monitored by the state machine.
3	3	VIN2	Noninverting Comparator Input. The voltage on this pin is compared with a 0.6 V reference. Can be used to monitor a voltage rail via a resistor divider. The output of this comparator is monitored by the state machine.
4	4	VIN3	Noninverting Comparator Input. The voltage on this pin is compared with a 0.6 V reference. Can be used to monitor a voltage rail via a resistor divider. The output of this comparator is monitored by the state machine.
5	5	VIN4	Noninverting Comparator Input. The voltage on this pin is compared with a 0.6 V reference. Can be used to monitor a voltage rail via a resistor divider. The output of this comparator is monitored by the state machine.
6		UP	Noninverting Comparator Input. A rising edge on this pin initiates a power-up sequence when the ADM1186-1 is in the WAIT START state.
7		$\overline{\text{DOWN}}$	Noninverting Comparator Input. A falling edge on this pin initiates a power-down sequence when the ADM1186-1 is in the POWER-UP DONE state.
	6	UP/$\overline{\text{DOWN}}$	Noninverting Comparator Input. A rising edge on this pin initiates a power-up sequence when the ADM1186-2 is in the WAIT START state. A falling edge on this pin initiates a power-down sequence when the ADM1186-2 is in the POWER-UP DONE state.
8		$\overline{\text{FAULT}}$	Active Low, Bidirectional, Open-Drain Pin. When an internal fault is detected by the ADM1186-1 state machine, this pin is asserted low and the SET FAULT state is entered. An external device pulling this pin low also causes the ADM1186-1 to enter the SET FAULT state.
9		DLY_EN_OUT1	Timing Input. The capacitor connected to this input sets the time delay between the UP input initiating a power-up sequence and OUT1 being asserted high. During a power-down sequence, this input sets the time delay between OUT1 being asserted low and SEQ_DONE being asserted low.
10	7	DLY_EN_OUT2	Timing Input. The capacitor connected to this input sets the time delay between VIN1 coming into compliance and OUT2 being asserted high during a power-up sequence. During a power-down sequence, this input sets the time delay between OUT2 being asserted low and OUT1 being asserted low.
11	8	DLY_EN_OUT3	Timing Input. The capacitor connected to this input sets the time delay between VIN2 coming into compliance and OUT3 being asserted high during a power-up sequence. During a power-down sequence, this input sets the time delay between OUT3 being asserted low and OUT2 being asserted low.

Pin No.		Mnemonic	Description
ADM1186-1	ADM1186-2		
12	9	DLY_EN_OUT4	Timing Input. The capacitor connected to this input sets the time delay between VIN3 coming into compliance and OUT4 being asserted high during a power-up sequence. During a power-down sequence, this input sets the time delay between OUT4 being asserted low and OUT3 being asserted low.
13	10	BLANK_DLY	Timing Input. The capacitor connected to this input sets the blanking time. This is the time allowed between OUTx being asserted and VINx coming into compliance; otherwise, the SET FAULT state is entered.
14		SEQ_DONE	Active High, Open-Drain Output. This output is pulled low when V_{CC} = 1 V. When the power-up sequence is complete, SEQ_DONE is asserted high. During a power-down sequence, the pin remains asserted until the time delay set by DLY_EN_OUT1 has elapsed. When a fault occurs, this pin is asserted low.
15	11	PWRGD	Active High, Open-Drain Output. This output is pulled low when V_{CC} = 1 V. The output state of this pin is a logical AND function of the UV threshold state of the VINx pins. When the voltage on all VINx inputs exceeds 0.6 V, PWRGD is asserted. This output is driven low if the voltage on any VINx pin is below 0.6 V.
16	12	OUT4	Active High, Open-Drain Output. This output is pulled low when V_{CC} = 1 V. During a power-up sequence, this output is asserted high after the time delay set by the capacitor on DLY_EN_OUT4 has elapsed. The output is asserted low immediately after a power-down sequence has been initiated.
17	13	OUT3	Active High, Open-Drain Output. This output is pulled low when V_{CC} = 1 V. During a power-up sequence, this output is asserted high after the time delay set by the capacitor on DLY_EN_OUT3 has elapsed. During a power-down sequence, the output is asserted low after the time delay set by the capacitor on DLY_EN_OUT4 has elapsed.
18	14	OUT2	Active High, Open-Drain Output. This output is pulled low when V_{CC} = 1 V. During a power-up sequence, this output is asserted high after the time delay set by the capacitor on DLY_EN_OUT2 has elapsed. During a power-down sequence, the output is asserted low after the time delay set by the capacitor on DLY_EN_OUT3 has elapsed.
19	15	OUT1	Active High, Open-Drain Output. This output is pulled low when V_{CC} = 1 V. During a power-up sequence, this output is asserted high after the time delay set by the capacitor on DLY_EN_OUT1 has elapsed (ADM1186-1) or immediately after a rising edge on UP/DOWN (ADM1186-2). During a power-down sequence, the output is asserted low after the time delay set by the capacitor on DLY_EN_OUT2 has elapsed.
20	16	VCC	Positive Supply Input Pin. The operating supply voltage range is 2.7 V to 5.5 V.

TYPICAL PERFORMANCE CHARACTERISTICS

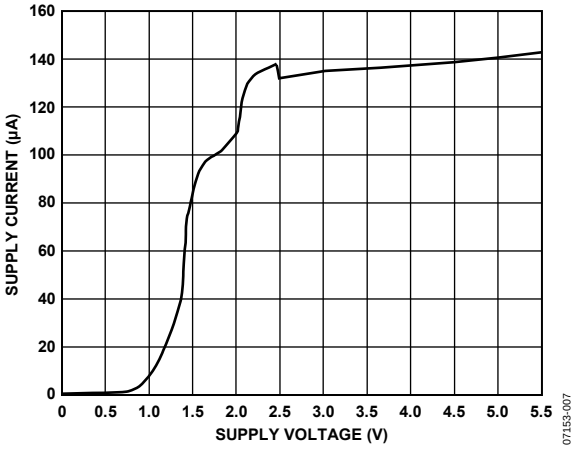


Figure 5. Supply Current vs. Supply Voltage

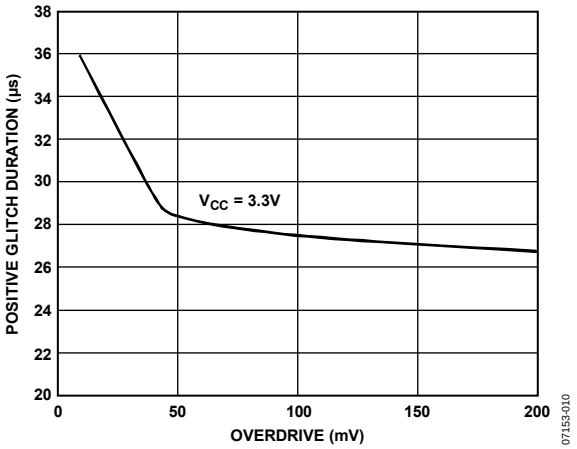


Figure 8. VINx Input Positive Glitch Immunity vs. Input Overdrive

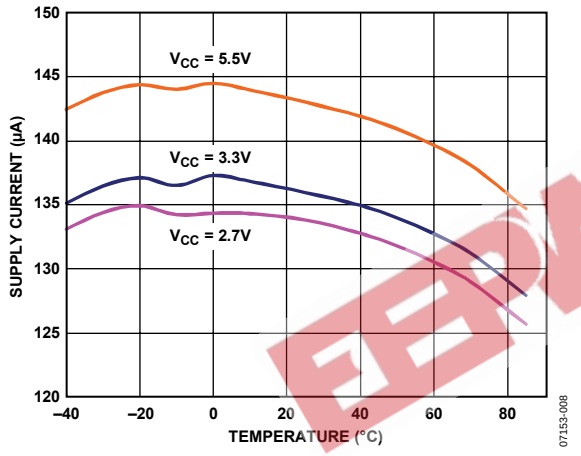


Figure 6. Supply Current vs. Temperature

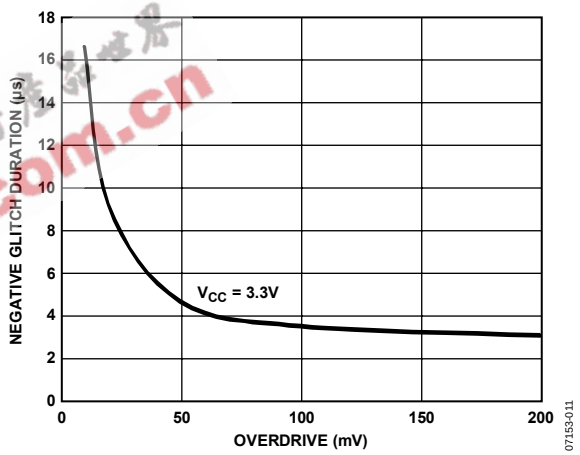


Figure 9. VINx Input Negative Glitch Immunity vs. Input Overdrive

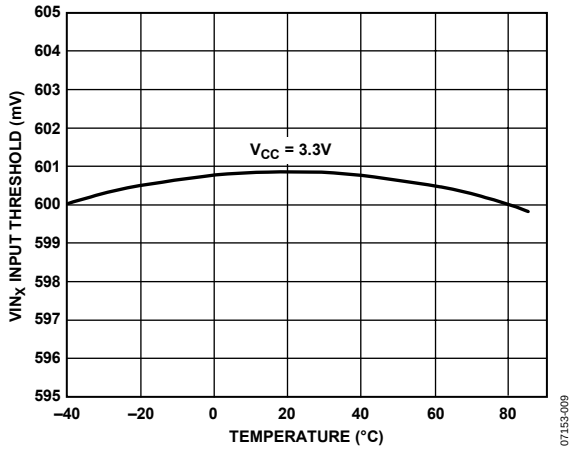


Figure 7. VINx Input Threshold vs. Temperature

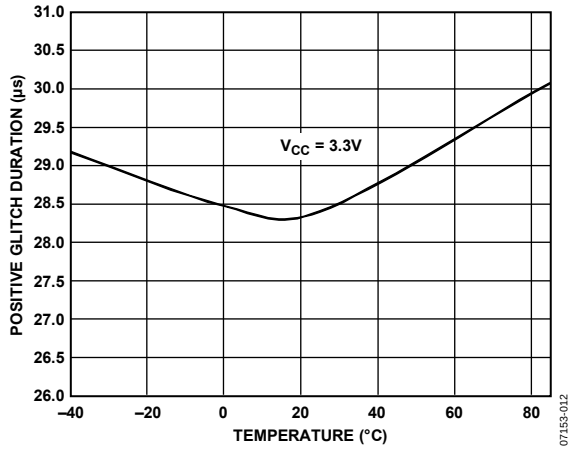


Figure 10. VINx Input Positive Glitch Immunity vs. Temperature

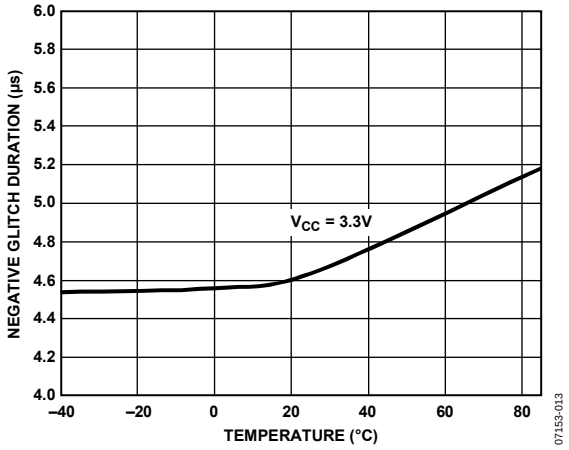


Figure 11. VINx Input Negative Glitch Immunity vs. Temperature

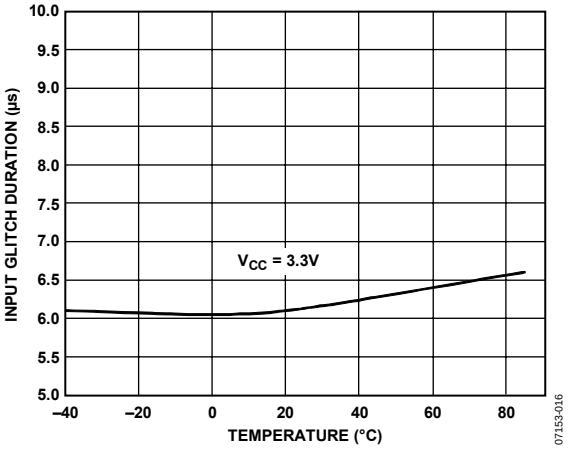


Figure 14. UP, $\overline{DOWN}$, and UP/$\overline{DOWN}$ Input Glitch Immunity vs. Temperature

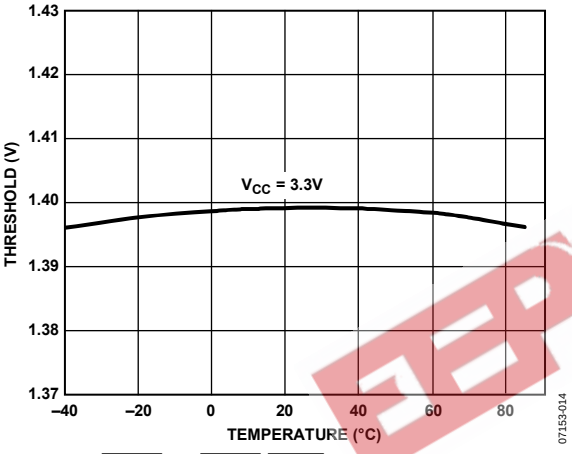


Figure 12. UP, $\overline{DOWN}$, UP/$\overline{DOWN}$, $\overline{FAULT}$, and Time Delay Trip Threshold vs. Temperature

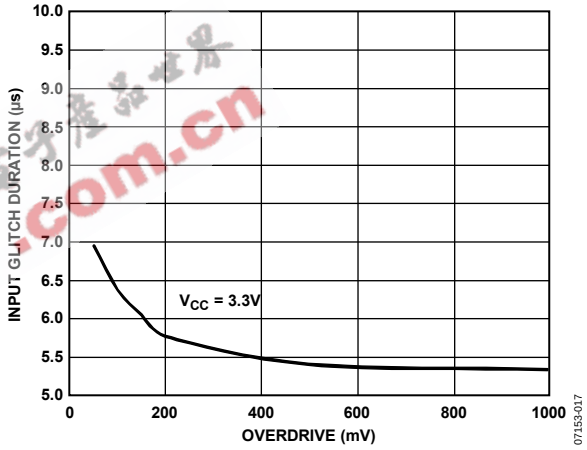


Figure 15. $\overline{FAULT}$ Input Glitch Immunity vs. Input Overdrive

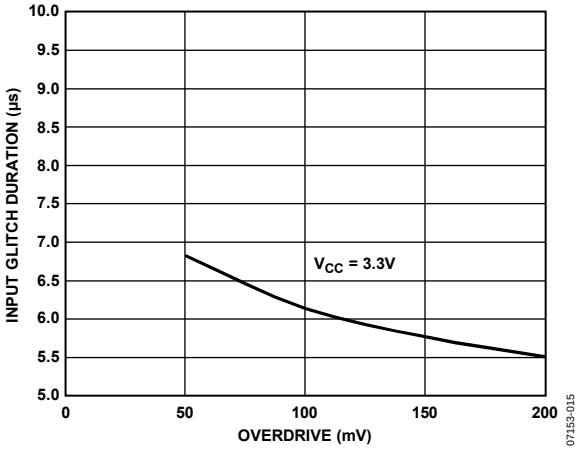


Figure 13. UP, $\overline{DOWN}$, and UP/$\overline{DOWN}$ Input Glitch Immunity vs. Input Overdrive

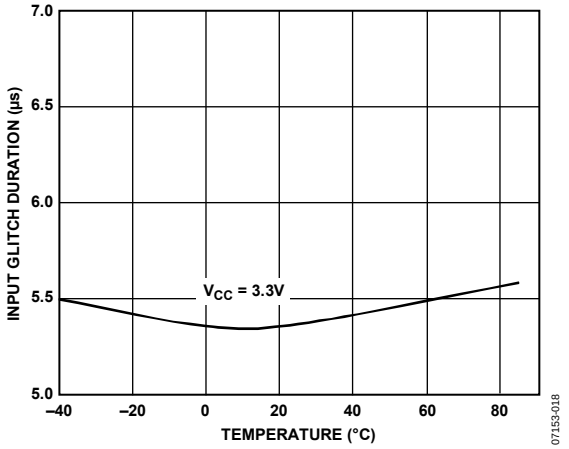


Figure 16. $\overline{FAULT}$ Input Glitch Immunity vs. Temperature

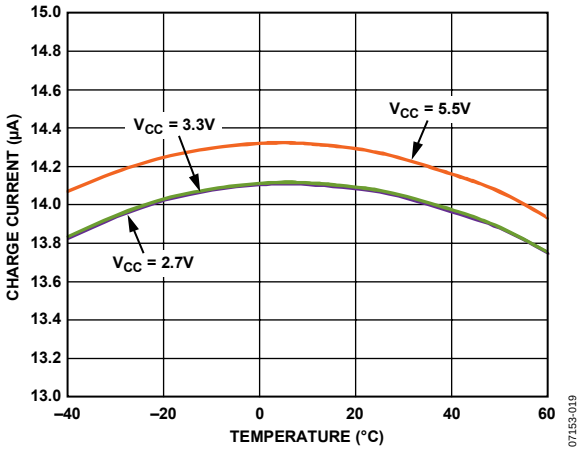


Figure 17. Time Delay Charge Current vs. Temperature

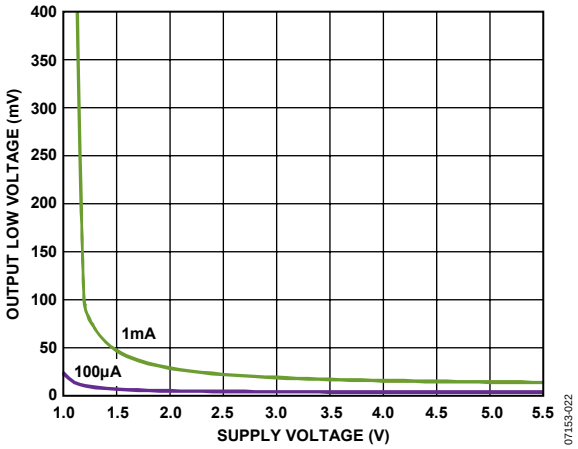


Figure 20. Output Low Voltage vs. Supply Voltage

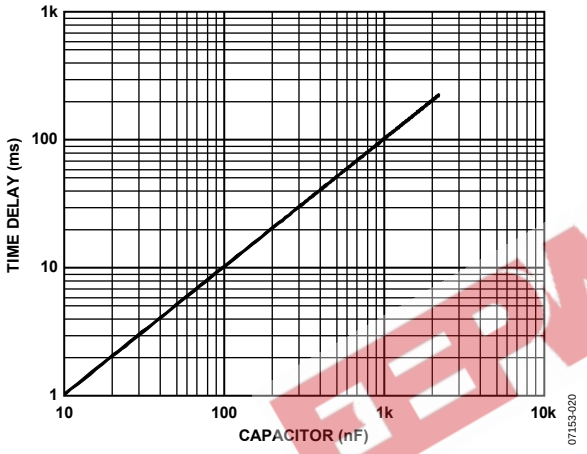


Figure 18. Time Delay vs. Capacitor Value

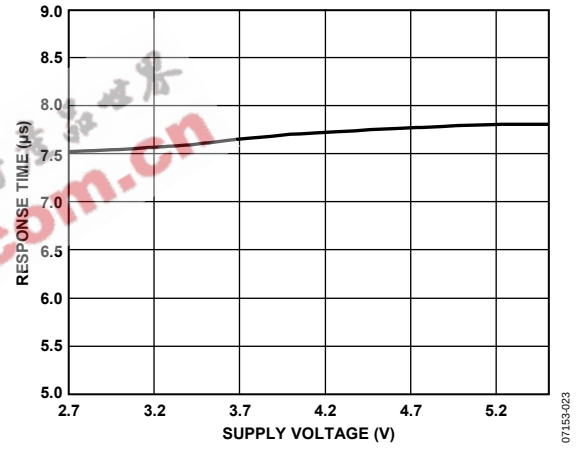


Figure 21. VINx to $\overline{FAULT}$, OUTx Low Response Time vs. Supply Voltage

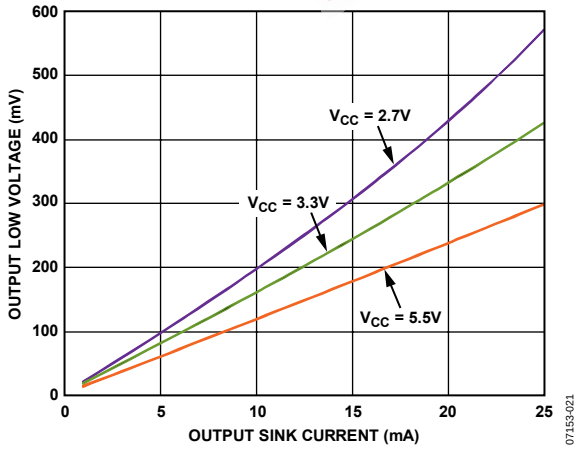


Figure 19. Output Low Voltage vs. Output Sink Current

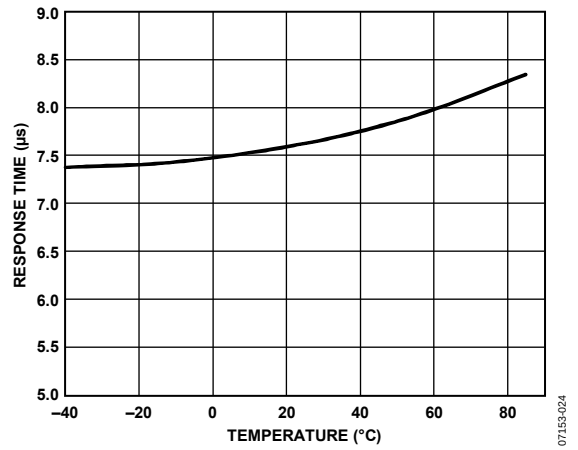


Figure 22. VINx to $\overline{FAULT}$, OUTx Low Response Time vs. Temperature

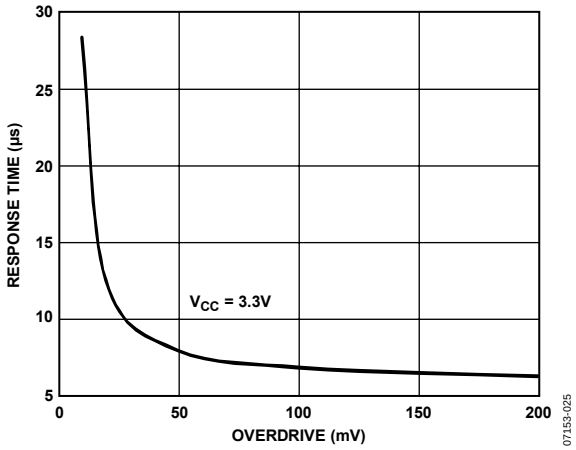


Figure 23. VINx to $\overline{FAULT}$, OUTx Low Response Time vs. Input Overdrive

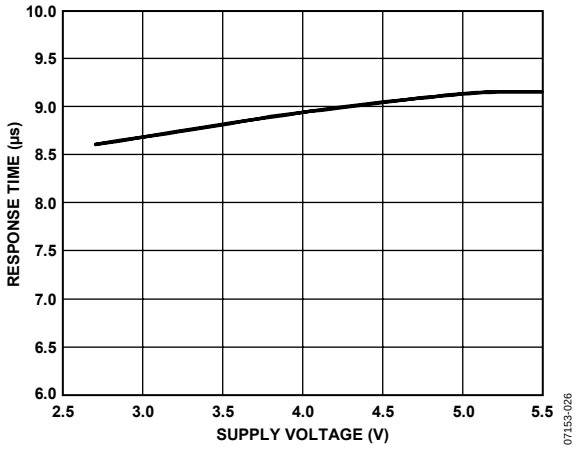


Figure 24. UP, $\overline{DOWN}$, UP/$\overline{DOWN}$ to $\overline{FAULT}$, OUTx Low Response Time vs. Supply Voltage

THEORY OF OPERATION

The operation of the ADM1186 is described in the following sections. Where necessary, differences between the ADM1186-1 and the ADM1186-2 are noted. Figure 28 is a detailed functional block diagram of the ADM1186-1, and Figure 30 is a detailed functional block diagram of the ADM1186-2.

The operation of the ADM1186 is described in the context of a typical voltage monitoring and sequencing application, as shown in Figure 1. This example uses the ADM1186-1, because it is essentially a superset of the functionality of the ADM1186-2. In the example application, the ADM1186-1 turns on four regulators, monitors four separate voltage rails, and generates a power-good signal to turn on a microcontroller when all power supplies are on and above their UV threshold level. Figure 34 shows a typical ADM1186-2 voltage sequencing and monitoring application.

UVLO BEHAVIOR

The ADM1186 is designed to ensure that the outputs are always in a known state for a V_{CC} supply voltage of 1 V or greater; if the V_{CC} supply voltage is below 1 V, the state of the outputs is not guaranteed. Figure 25 shows the behavior of the outputs over the full V_{CC} supply range.

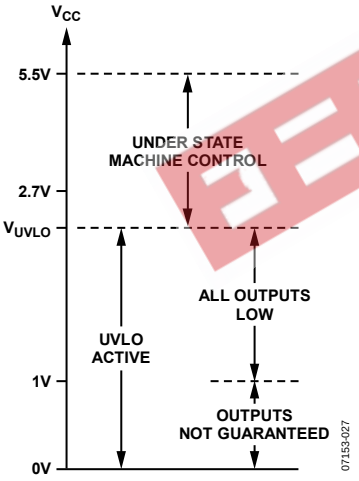


Figure 25. ADM1186 Output Behavior over V_{CC} Supply

As the V_{CC} supply begins to rise, an undervoltage lockout (UVLO) circuit becomes active and begins to pull the outputs of the ADM1186 low. The outputs are not guaranteed to be low until the V_{CC} supply has reached 1 V. State machine operation is also disabled, so it is not possible to initiate a power-up sequence.

This behavior ensures that enable pins on dc-to-dc converters or point-of-load (POL) devices connected to the OUTx pins are held low as the supplies are rising. This prevents the dc-to-dc converters or the POLs from switching on briefly and then switching off as the supply rails stabilize.

When V_{CC} rises above V_{UVLO} and the internal reference is stable, the UVLO circuit enables the state machine. The state machine takes control of the outputs and begins operation from the SET FAULT state.

After the fault hold time elapses, the state machine moves to the CLEAR FAULT state. If the UP (ADM1186-1) or UP/$\overline{\text{DOWN}}$ (ADM1186-2) pin is low, the state machine can exit the CLEAR FAULT state. This change is indicated on the ADM1186-1 by the $\overline{\text{FAULT}}$ pin being asserted high. For the ADM1186-2, there is no external indication that the part is ready to perform sequencing, so 0.5 ms should be allowed after V_{CC} comes up before attempting to start a power-up sequence.

POWER-UP SEQUENCING AND MONITORING

In the example shown in Figure 1, the main supply of 3.3 V powers up the device via the VCC pin. The state machine remains in the WAIT START state until either a rising edge on the UP pin initiates a power-up sequence, or a fault condition occurs. The ADM1186-2 requires a rising edge on the UP/$\overline{\text{DOWN}}$ pin to start a power-up sequence.

If a rising edge on the UP pin is detected, the state machine moves to the DELAY 1 state. The ADM1186-2 does not have a DLY_EN_OUT1 pin, so it omits the DELAY 1 state. Figure 29 shows the ADM1186-1 state machine in detail; Figure 31 shows the ADM1186-2 state machine. The waveforms for a typical power-up and power-down sequence when no faults occur are shown in Figure 32 (ADM1186-1) and Figure 33 (ADM1186-2).

In the DELAY 1 state, a time delay, set by the capacitor connected to the DLY_EN_OUT1 pin, is allowed to elapse. Then, in the ENABLE OUT1 state, the OUT1 pin is asserted high. OUT1 is an open-drain, active high output, and in this application it enables the output of a 2.5 V regulator.

During the ENABLE OUT1 state, the VIN1 pin monitors the 2.5 V supply after a blanking delay, set by the capacitor on the BLANK_DLY pin. The blanking delay, which is the same for all supplies, is set to allow the slowest rising supply sufficient time to switch on.

An external resistor divider scales the supply voltage down for monitoring at the VIN1 pin (see Figure 26). The resistor ratio is selected so that the VIN1 voltage is 0.6 V when the supply voltage rises to the UV level at start-up (a voltage below the nominal 2.5 V level). In Figure 26, R1 is 7.4 kΩ and R2 is 2.5 kΩ, so a voltage level of 2.375 V corresponds to 0.6 V on the noninverting input of the first comparator.

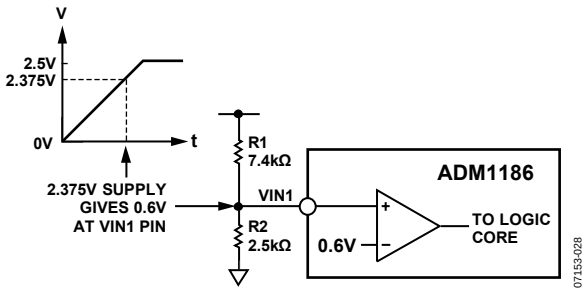


Figure 26. Setting the Undervoltage Threshold with an External Resistor Divider

If the output of the 2.5 V regulator meets the UV level when the blanking time elapses, the state machine continues the power-up sequence, moving into the DELAY 2 state. A time delay, set by the capacitor connected to the DLY_EN_OUT2 pin, elapses before turning on the next enable output, OUT2, in the ENABLE OUT2 state.

If the 1.8 V supply does not rise to the UV level before the blanking time elapses, sequencing immediately stops and the state machine enters the SET FAULT state.

The same scheme is implemented with the other output and input pins. Every supply turned on via an output pin, OUTx, is monitored via an input pin, VINx, to check that the supply has risen above the UV level within the blanking time before the state machine moves on to the next supply.

When a supply is on and operating correctly, the ADM1186 continues to monitor it for the duration of the power-up sequence. If any supply drops below its UV threshold level during a power-up sequence, sequencing stops and the state machine enters the SET FAULT state.

When the state machine is in the WAIT START state, or at any time during a power-up sequence, a falling edge on the $\overline{\text{DOWN}}$ pin (ADM1186-1) or the UP/$\overline{\text{DOWN}}$ pin (ADM1186-2) generates a fault.

The PWRGD pin is asserted high, independently of the state machine, when all four VINx pins are above their UV threshold. The state machine in the ADM1186-1 indicates that the power-up sequence is complete by asserting the SEQ_DONE pin high.

OPERATION IN POWER-UP DONE STATE

When the power-up sequence is complete, the state machine remains in the POWER-UP DONE state until one of the following events occurs:

- A falling edge occurs on the $\overline{\text{DOWN}}$ (ADM1186-1) or UP/$\overline{\text{DOWN}}$ (ADM1186-2) pin, initiating a power-down sequence.
- An undervoltage condition occurs on one or more of VIN1 to VIN4, generating a fault.
- A rising edge occurs on the UP pin, generating a fault (ADM1186-1 only).
- An external device brings the $\overline{\text{FAULT}}$ pin low, causing a fault (ADM1186-1 only).

POWER-DOWN SEQUENCING AND MONITORING

When the ADM1186 is in the POWER-UP DONE state, a falling edge on the $\overline{\text{DOWN}}$ or UP/$\overline{\text{DOWN}}$ pin initiates a power-down sequence (see Figure 29 or Figure 31).

The state machine moves to the DISABLE OUT4 state, bringing the OUT4 pin low and switching off the 3.3 V regulator. A time delay, set by the capacitor on the DLY_EN_OUT4 pin, elapses before the state machine moves to the DISABLE OUT3 state.

This sequence of steps is repeated until all four regulators are switched off and the device is in the WAIT START state. Because the ADM1186-2 does not have a DLY_EN_OUT1 pin, there is no delay between the OUT1 pin being brought low and the state machine returning to the WAIT START state. When the device is in the WAIT START state, the SEQ_DONE pin is brought low.

During a power-down sequence, the state machine monitors the supplies that are still on. If a supply drops below its UV threshold before it is turned off, the power-down sequence immediately stops and the state machine enters the SET FAULT state.

A rising edge on the UP or UP/$\overline{\text{DOWN}}$ pin during a power-down sequence generates a fault.

The PWRGD pin is asserted low, independently of the state machine power-down sequence, when one or more of the VINx pins drops below 0.6 V.

INPUT GLITCH FILTERING

The VINx, UP, $\overline{\text{DOWN}}$, and $\overline{\text{FAULT}}$ inputs on the ADM1186-1 and the VINx and UP/$\overline{\text{DOWN}}$ inputs on the ADM1186-2 use a time-based glitch filter to prevent false triggering. The glitch filter avoids the need to use some of the operating supply range to provide hysteresis on an input. This helps to maximize the available operating supply range for a system, which is especially important in systems where low supply voltages are being used.

The VINx inputs use a positive glitch filter that is approximately five times longer than the negative glitch filter. This provides additional glitch immunity during the power-up sequence as a supply is rising, but still allows for a quick response in the event of an undervoltage event on an input.

FAULT CONDITIONS AND FAULT HANDLING

During supply sequencing and operation in the POWER-UP DONE state, the ADM1186 continuously monitors the VINx, UP, $\overline{\text{DOWN}}$, and UP/$\overline{\text{DOWN}}$ pins for fault conditions. The $\overline{\text{FAULT}}$ pin on the ADM1186-1 is monitored to detect external faults generated by other devices, which is important during cascade operation.

The following faults are internally generated:

- A supply fails to reach the UV threshold within the time defined by the BLANK_DLY capacitor during a power-up sequence.
- A UV condition occurs on VINx after the blanking time has elapsed during a power-up sequence.
- A UV condition occurs on VINx before the supply is disabled during a power-down sequence.
- A falling edge occurs on the $\overline{\text{DOWN}}$ or UP/$\overline{\text{DOWN}}$ pin during a power-up sequence or in the WAIT START state.
- A rising edge occurs on the UP or UP/$\overline{\text{DOWN}}$ pin during a power-down sequence or in the POWER-UP DONE state.

The action taken by the ADM1186 state machine is the same for an internal or external fault. The state machine enters the SET FAULT state, asserts the SEQ_DONE and $\overline{\text{FAULT}}$ pins low (ADM1186-1 only), and asserts all four OUTx enable pins low.

The ADM1186 remains in the SET FAULT state for the fault hold time before moving into the CLEAR FAULT state. If the UP or UP/$\overline{\text{DOWN}}$ pin is low for a time of $t \geq t_{UDOUT}$ before the state machine enters the CLEAR FAULT state, the state machine can move immediately into the WAIT ALL OK state.

The length of time from entering the SET FAULT state to reaching the WAIT ALL OK state, with the UP or UP/$\overline{\text{DOWN}}$ pin held low, is the fault hold time. The fault hold time is the minimum amount of time that the $\overline{\text{FAULT}}$ pin is held low. If the UP or UP/$\overline{\text{DOWN}}$ pin is high when the state machine enters the CLEAR FAULT state, the time that the $\overline{\text{FAULT}}$ pin is held low is extended.

When the ADM1186-1 is in the CLEAR FAULT state and the UP pin is low, the WAIT ALL OK state is entered and the $\overline{\text{FAULT}}$ pin is deasserted. If an external device is driving the $\overline{\text{FAULT}}$ pin low, the state machine remains in the WAIT ALL OK state until the $\overline{\text{FAULT}}$ pin returns high. The state machine then transitions into the WAIT START state, ready for the next power-up sequence.

DEFINING TIME DELAYS

The ADM1186 allows the user to define sequence and blanking time delays using capacitors. The ADM1186-1 has four DLY_EN_OUTx pins, and the ADM1186-2 has three DLY_EN_OUTx pins. Capacitors connected to these pins control the time delay between supplies turning on or off during the power-up and power-down sequences. Both devices provide one pin (BLANK_DLY) to set the blanking time delay.

The ADM1186-1 has a pin called DLY_EN_OUT1 that the ADM1186-2 does not have. The capacitor on this pin sets the time delay used before enabling OUT1 during a power-up sequence, as well as the time delay between disabling OUT1 and returning to the WAIT START state during a power-down sequence. Although this time delay is not essential when a single ADM1186-1 device is used, the time delay is essential when multiple devices are cascaded (see the Cascading Multiple Devices section).

When ADM1186-1 devices are used in cascade, the capacitor on the DLY_EN_OUT1 pin of Device N + 1 sets the sequence time delay between the last supply of Device N and the first supply of Device N + 1 being turned on and off.

During the power-up sequence, the capacitors connected to the DLY_EN_OUTx pins set the time from the end of the blanking period to the next enable output being asserted high. During the power-down sequence, the capacitors set the time between consecutive enable outputs being asserted low.

The blanking time is controlled by the capacitor on the BLANK_DLY pin. This capacitor sets the time allowed between an enable output being asserted, turning on a supply, and the output of the supply rising above its defined UV threshold.

A constant current source is connected to a capacitor through a switch that is under the control of the state machine. This current source charges a capacitor until the threshold voltage is reached. For all capacitors, the duration of the time delay is defined by the following formula:

$$t_{DELAY} = C_{DELAY} \times 0.1$$

where:
t_{DELAY} is the time delay in seconds.
C_{DELAY} is the capacitor value in microfarads (μF).

For capacitor values from 10 nF to 2.2 μF, the time delay is in the range of 1 ms to 220 ms. If a capacitor is not connected to a timing pin, the time delay is minimal, in the order of several microseconds.

When a capacitor is not being charged by the current source, it is connected via a resistor to ground. Each capacitor has a dedicated resistor with a typical value of 450 Ω. To ensure accurate time delays, time must be allowed for a capacitor to discharge after it has been used. Typically, allowing five RC time constants is sufficient for the capacitor to discharge to less than 1% of the threshold voltage.

If the capacitors are not sufficiently discharged after use, the time delays will be smaller than expected. This can happen if very small capacitor values are used or if a power-up or power-down sequence is performed immediately after another sequence has been completed. Examples of when this behavior can occur include, but are not limited to, the following:

- A power-down sequence is initiated immediately after entering the POWER-UP DONE state.
- A fault occurs in the ENABLE OUT1 state when the DLY_EN_OUT1 capacitor is charged and a power-up sequence is started very quickly after the fault has been handled.
- The DLY_EN_OUTx time delay is very short and is insufficient to allow the BLANK_DLY capacitor to fully discharge.

To achieve the best timing accuracy over the operational temperature range, the choice of capacitor is critical. Capacitors are typically specified with a value tolerance of ±5%, ±10%, or ±20%, but in addition to the value tolerance, there is also a variation in capacitance over temperature.

Where high accuracy timing is important, the use of capacitors that use a C0G, sometimes called NPO, dielectric results in a capacitance variation of only ±0.3% over the full temperature range. This capacitance variation contrasts with typical variations of ±15% for X5R and X7R dielectrics and ±22% for X7S capacitor dielectrics.

SEQUENCE CONTROL USING A SUPPLY RAIL

The UP and $\overline{\text{DOWN}}$ inputs on the ADM1186-1 and the UP/$\overline{\text{DOWN}}$ input on the ADM1186-2 are used to initiate power-up and power-down sequences. These inputs are designed for use with digital or analog signals, such as power supply rails. Using a power supply rail to control the up and down sequencing allows the ADM1186 to perform sequencing and monitoring functions for five supply rails.

When using a supply rail to control an ADM1186-1 (with the UP and $\overline{\text{DOWN}}$ pins connected) or an ADM1186-2, some hysteresis is required. The hysteresis is added on the joined UP and $\overline{\text{DOWN}}$ pins of the ADM1186-1 or on the UP/$\overline{\text{DOWN}}$ pin of the ADM1186-2 to ensure that a slowly ramping supply rail does not cause spurious rising or falling edges that would otherwise cause state machine faults.

To provide the necessary hysteresis, a single additional resistor (RH in Figure 27) is connected between the joined UP and $\overline{\text{DOWN}}$ pins of the ADM1186-1 and the OUT1 pin of the device, or between the UP/$\overline{\text{DOWN}}$ pin of the ADM1186-2 and the OUT1 pin of the device.

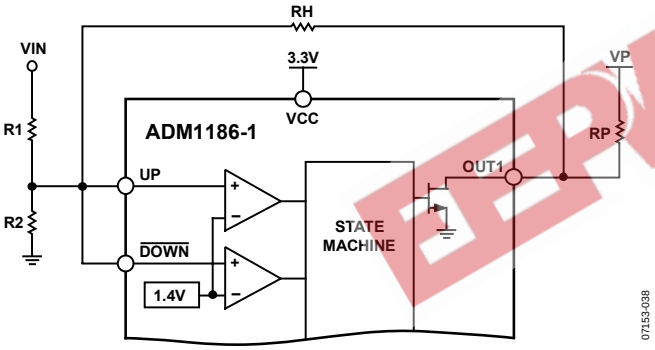


Figure 27. Using a Supply Rail to Control Sequencing with Hysteresis

When OUT1 is low, the resistor RH sinks current from the node at the midpoint of R1 and R2, slightly increasing the VIN voltage needed to start a power-up sequence, referred to as V_H. When OUT1 is high, RH sources current into the midpoint of R1 and R2, decreasing the VIN voltage necessary to start a power-down sequence, referred to as V_L.

The hysteresis at the VIN node is simply $V_H - V_L$. As the R1 and R2 resistors scale VIN down, the hysteresis on VIN is also scaled down. The scaled hysteresis, V_{SHYS}, at the inputs to the UP and $\overline{\text{DOWN}}$ pins (ADM1186-1) or the UP/$\overline{\text{DOWN}}$ pin (ADM1186-2) must be at least 75 mV. The value of RH is selected to ensure that this is the case.

$$V_H = 1.4 \times \left[1 + \left(R1 \times \frac{R2 + RH}{R2 \times RH}\right)\right]$$

$$V_L = 1.4 + \left[R1 \times \left(\frac{1.4}{R2} - \frac{VP - 1.4}{RH + RP}\right)\right]$$

$$V_{SHYS} = (V_H - V_L) \times \left(\frac{R2}{R1 + R2}\right)$$

In the example application shown in Figure 27, the following values could be used:

RP = 10 kΩ

VP = 5 V

VIN = 3.3 V

The values of the R1 and R2 resistors determine the midpoint of the hysteresis, V_{MID}, about which V_H and V_L set the levels at which power-up and power-down sequences are initiated. For a 3.3 V supply, a threshold just below 3 V could be used, making R1 = 11 kΩ and R2 = 10 kΩ and giving a midpoint of 2.94 V.

$$V_{MID} = \frac{VIN \times R2}{R1 + R2} = \frac{3.3 \times 10\,\text{k}}{11\,\text{k} + 10\,\text{k}}$$

V_{MID} = 2.94 V

As a general rule, the value for RH is approximately 60 times the value of R1 in parallel with R2. In this example, R1 in parallel with R2 is 5.24 kΩ, so RH would be approximately 314 kΩ. Taking a value of 300 kΩ for RH and using this value in the previous equations for V_H, V_L, and V_{SHYS}, the following values are obtained:

$$V_H = 1.4 \times \left[1 + \left(11\,\text{k} \times \frac{10\,\text{k} + 300\,\text{k}}{10\,\text{k} \times 300\,\text{k}}\right)\right]$$

V_H = 2.991 V

$$V_L = 1.4 + \left[11\,\text{k} \times \left(\frac{1.4}{10\,\text{k}} - \frac{5 - 1.4}{300\,\text{k} + 10\,\text{k}}\right)\right]$$

V_L = 2.812 V

$$V_{SHYS} = (2.991 - 2.812) \times \left(\frac{10\,\text{k}}{11\,\text{k} + 10\,\text{k}}\right)$$

V_{SHYS} = 0.085 V

Because the value of V_{SHYS} is greater than the 75 mV of scaled hysteresis required, the RH resistor value selected is sufficient. If the value of V_{SHYS} obtained is too small, the value of RH can be reduced, increasing the scaled hysteresis provided.

It should be noted that it is not possible to directly connect the V_{CC} supply to the UP pin (ADM1186-1) or to the UP/$\overline{\text{DOWN}}$ pin (ADM1186-2) to start a sequence as the V_{CC} comes up. When the UVLO circuit enables the state machine, it begins in the fault handler states. To reach the WAIT START state so that sequencing can begin, the UP pin (ADM1186-1) or the UP/$\overline{\text{DOWN}}$ pin (ADM1186-2) must be held low after the state machine is enabled.

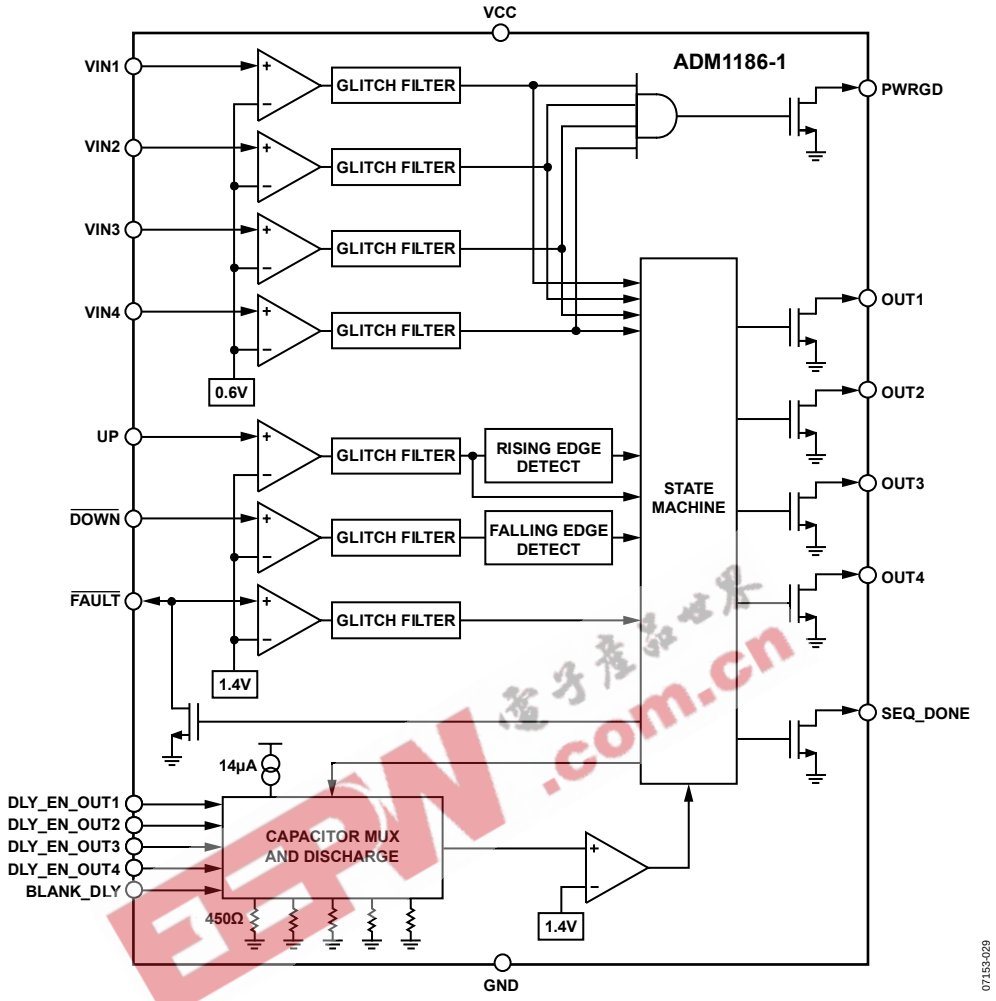


Figure 28. Functional Block Diagram of the ADM1186-1

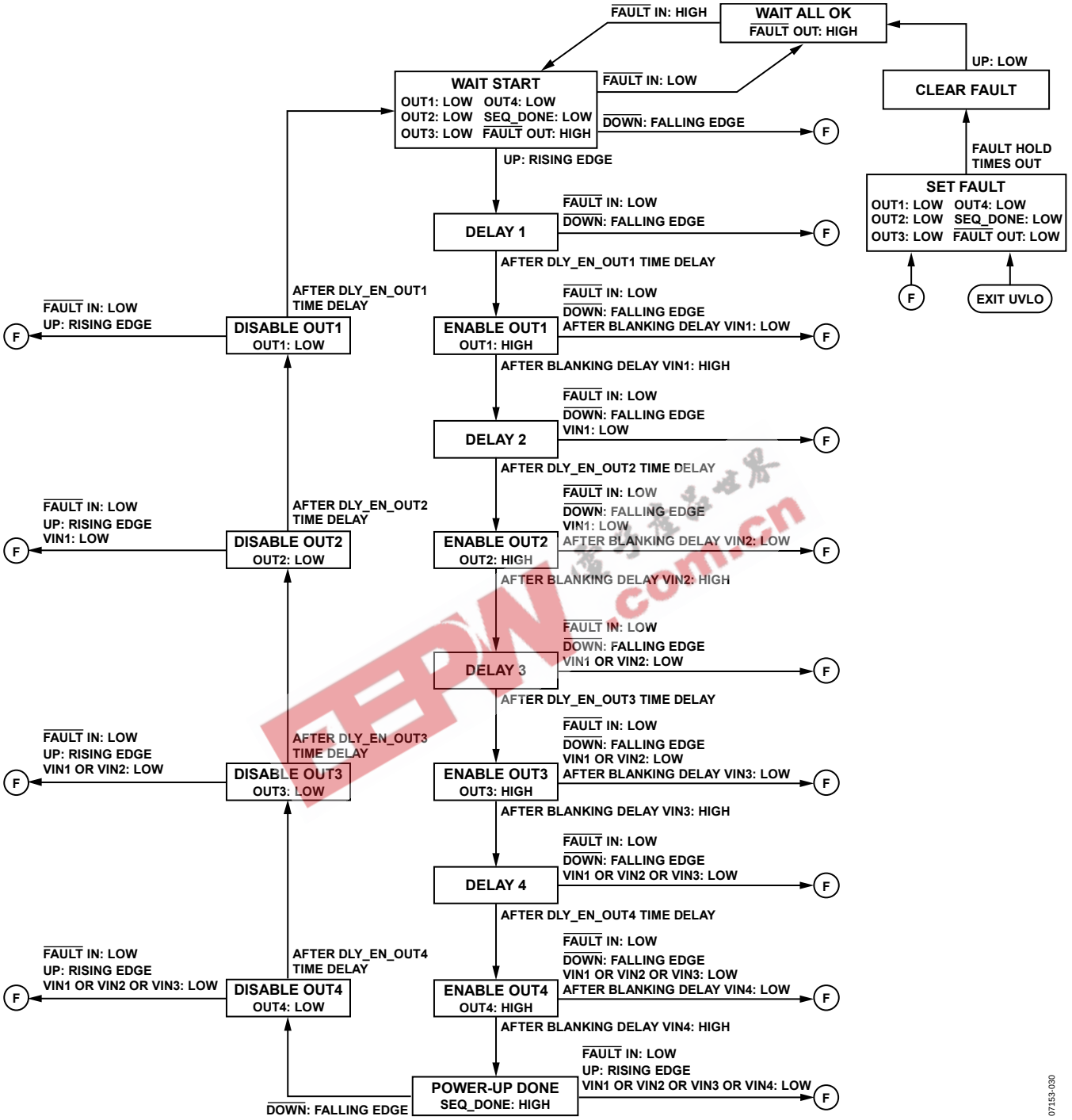


Figure 29. ADM1186-1 State Machine Operation

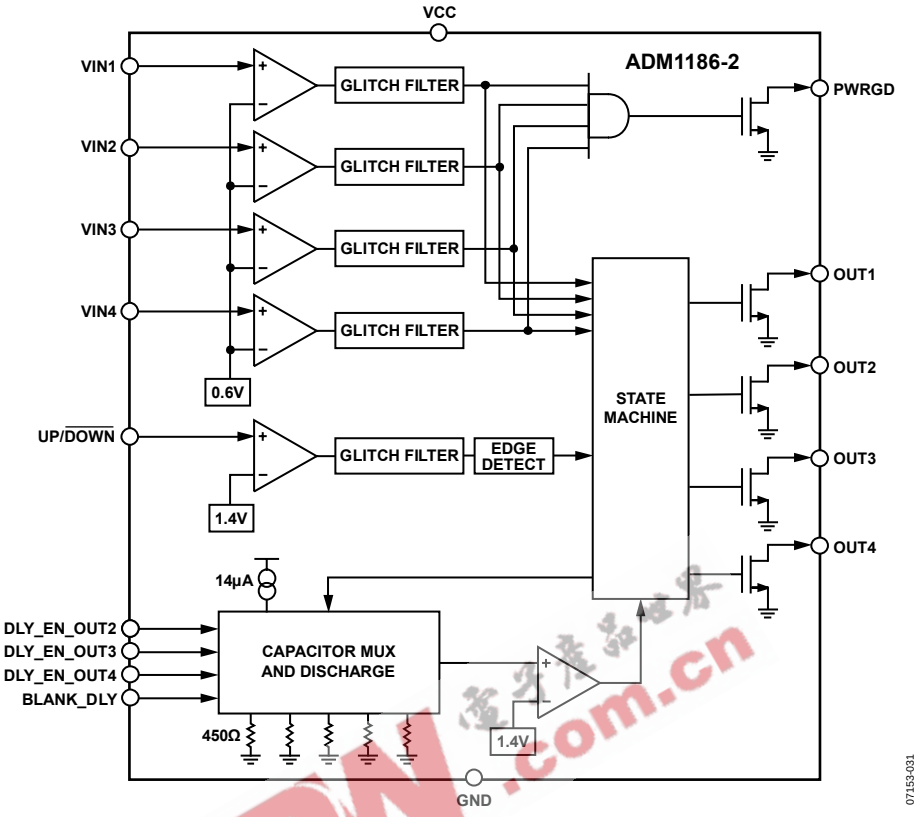


Figure 30. Functional Block Diagram of the ADM1186-2

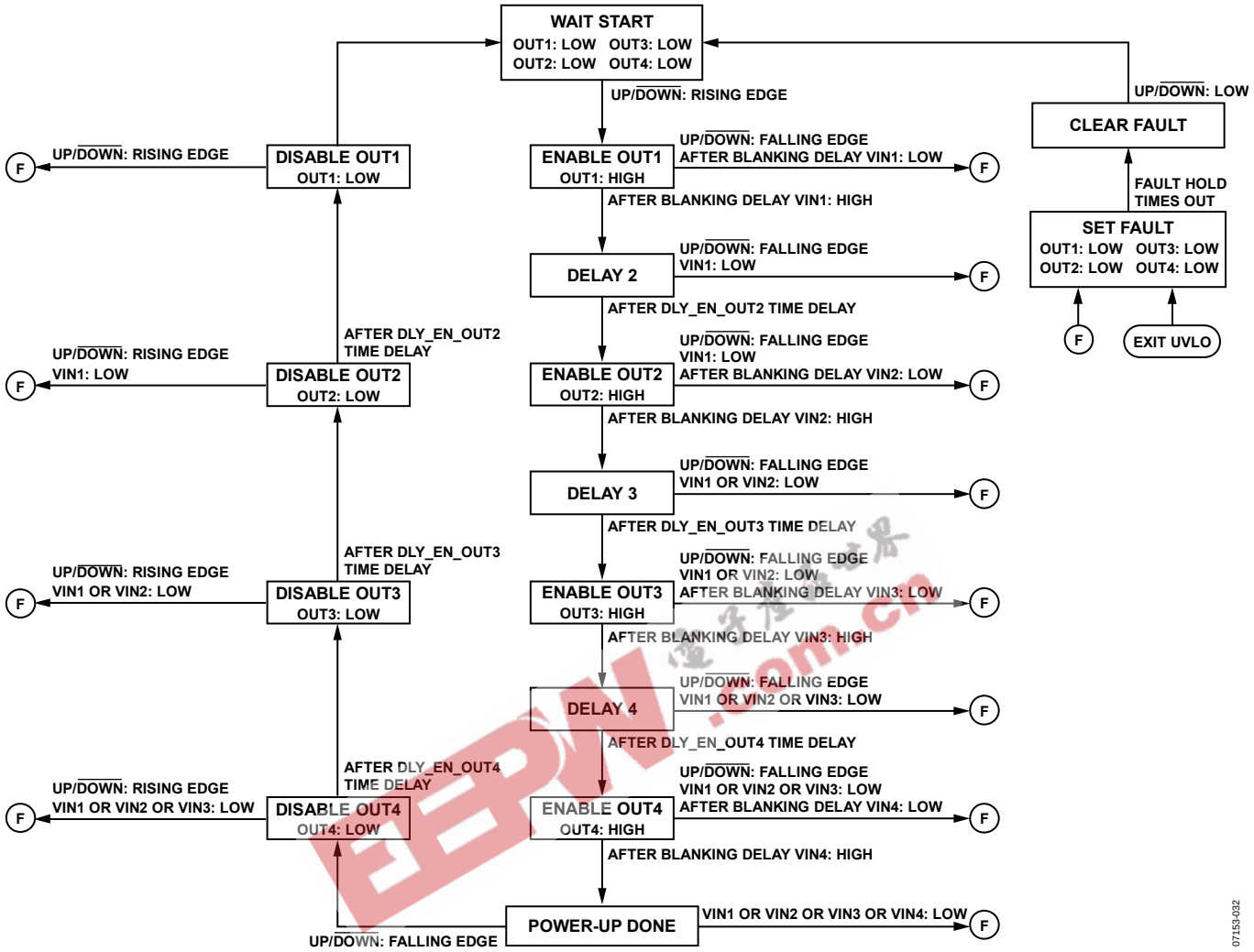


Figure 31. ADM1186-2 State Machine Operation

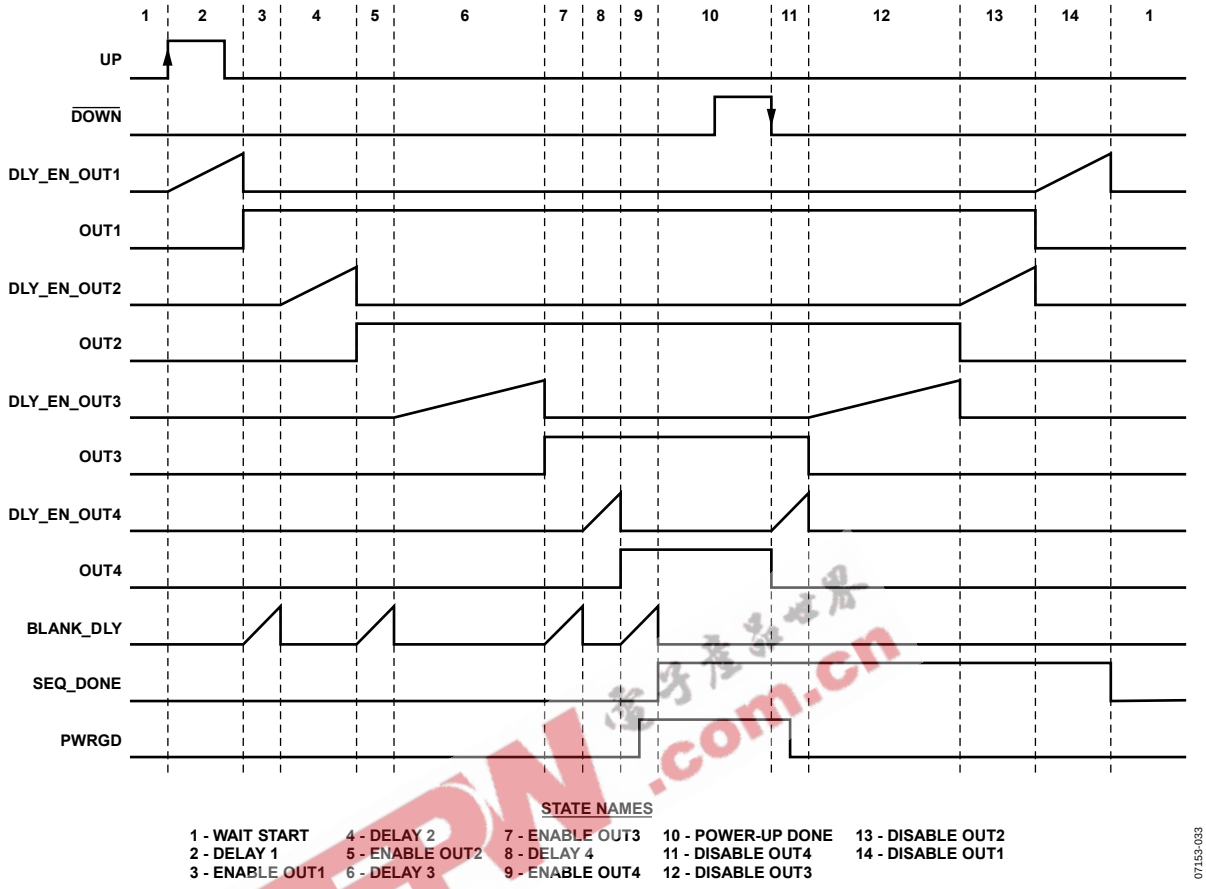


Figure 32. ADM1186-1 Typical Power-Up and Power-Down Sequence Waveforms with Corresponding State Names

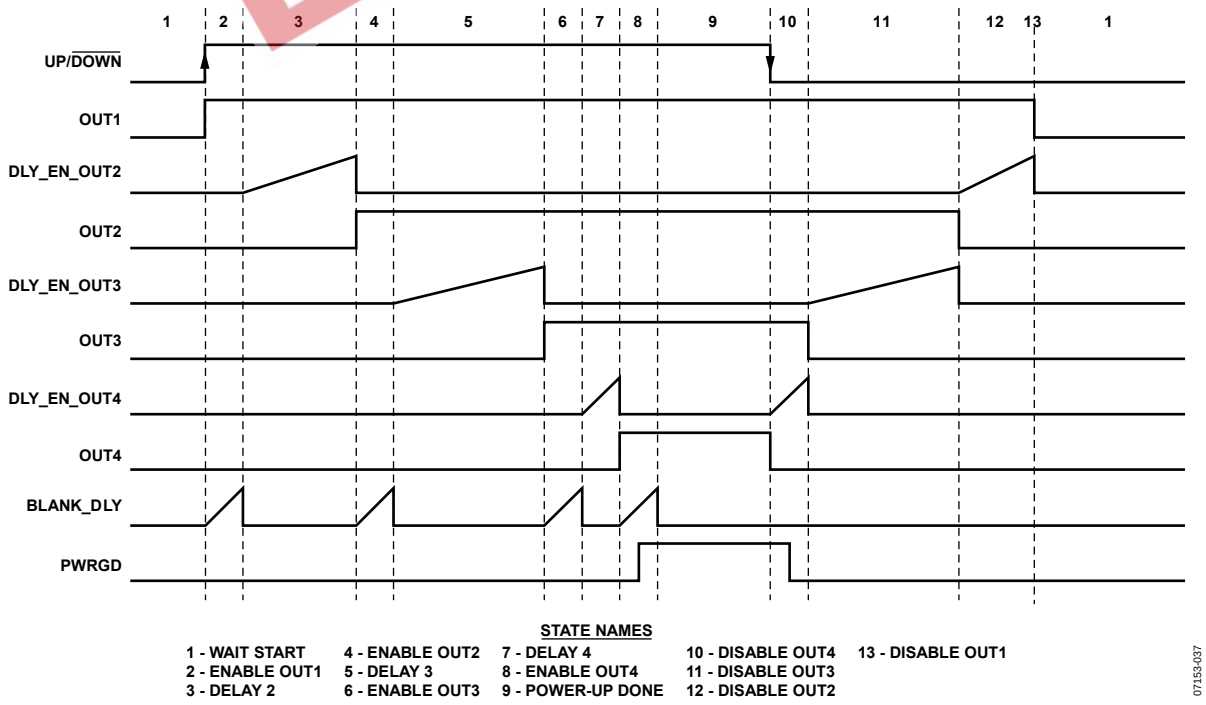


Figure 33. ADM1186-2 Typical Power-Up and Power-Down Sequence Waveforms with Corresponding State Names

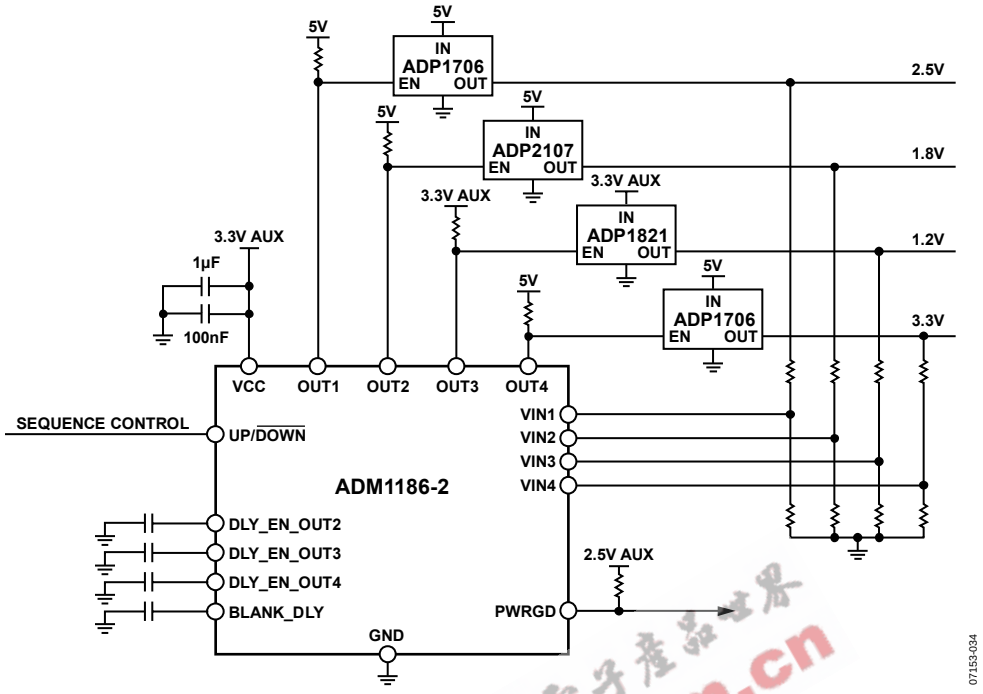


Figure 34. ADM1186-2 Typical Application

CASCADING MULTIPLE DEVICES

Multiple ADM1186-1 devices can be cascaded in applications that require more than four supplies to be sequenced and monitored. When ADM1186-1 devices are cascaded, the controlled power-up and power-down of all the cascaded supplies is maintained using only three pins on each device.

There are several configurations for interconnecting these devices. The most suitable configuration depends on the application. Figure 35 and Figure 36 show two methods for cascading multiple ADM1186-1 devices.

Figure 35 shows a single sequence of 12 supplies. The capacitors used for timing are not shown in the figure for clarity. To ensure controlled power-up and power-down sequencing of all 12 supplies, the following connections are made:

- The UP pin of the first device and the $\overline{\text{DOWN}}$ pin of the last device in the cascade chain are connected.
- The SEQ_DONE pin of Device N is connected to the UP pin of Device N + 1.
- The SEQ_DONE pin of Device N is connected to the $\overline{\text{DOWN}}$ pin of Device N − 1.

When the SEQUENCE CONTROL line goes high, Device A begins the power-up sequence, turning on each enable output in turn, with the associated delays, according to the state machine. When Device A completes its power-up sequence, the SEQ_DONE pin goes from low to high, initiating a power-up sequence on Device B. When Device B completes its power-up sequence, the Device B SEQ_DONE pin goes high, initiating a power-up sequence on Device C. When Device C completes its power-up sequence and all supplies are above the UV threshold, the system POWER GOOD signal goes high.

If the SEQUENCE CONTROL line goes low, Device C starts a power-down sequence, turning off its enable outputs. When all Device C enable outputs are off, the SEQ_DONE pin on Device C goes low, causing a high-to-low transition on the $\overline{\text{DOWN}}$ pin of Device B. This transition initiates a power-down sequence on Device B, which takes all its OUTx pins low, causing SEQ_DONE to be taken low. This high-to-low transition is seen by Device A, which starts its power-down sequence, thus completing the ordered shutdown of the 12 supplies.

Note that the capacitor on the DLY_EN_OUT1 pin of Device B (not shown in Figure 35) sets the sequence time delay between the last supply of Device A and the first supply of Device B being turned on and off.

Figure 36 shows two independent sequences of four supplies, each with common status outputs. In this example, both devices share the same sequence control signal, so they start their power-up and power-down sequences at the same time. Both devices must complete their power-up sequences before the POWER GOOD signal goes high.

The $\overline{\text{FAULT}}$ pins of all devices in a cascade should be connected. Connecting the $\overline{\text{FAULT}}$ pins ensures that an undervoltage fault on one device, or an unexpected event such as a rising or falling edge on the UP or $\overline{\text{DOWN}}$ pin, generates a fault condition on all the other devices.

When an internal fault condition occurs on a device, it pulls its $\overline{\text{FAULT}}$ pin low. This in turns causes the other ADM1186-1 devices to enter the SET FAULT state and pull their $\overline{\text{FAULT}}$ pins low. Each device waits for the fault hold time to elapse and then moves to the CLEAR FAULT state.

If the V_{CC} supply for an ADM1186-1 drops below V_{UVLO}, the UVLO circuit becomes active, and the $\overline{\text{FAULT}}$ pin is pulled low. This generates a fault condition on all other connected devices.

A device in the CLEAR FAULT state holds its $\overline{\text{FAULT}}$ pin low until its UP input pin is low. The device then moves into the WAIT ALL OK state and releases the $\overline{\text{FAULT}}$ pin.

If, for example, a UV fault occurs on a VINx pin during a power-up sequence, the UP pin will be high on the first device in the cascade. The first device in the cascade holds the $\overline{\text{FAULT}}$ line low until the UP pin is brought low. All other devices will have released their $\overline{\text{FAULT}}$ pins and will be in the WAIT ALL OK state.

When the UP pin goes low, the first device releases its $\overline{\text{FAULT}}$ pin so the $\overline{\text{FAULT}}$ line returns high, which allows all devices to move together from the WAIT ALL OK state back into the WAIT START state, ready for the next power-up sequence.

An external device such as a microcontroller, field programmable gate array (FPGA), or an overtemperature sensor can cause a fault condition by briefly bringing $\overline{\text{FAULT}}$ low. In this case, the ADM1186-1 behaves as described. If the external device continues to hold the $\overline{\text{FAULT}}$ line low, all the ADM1186-1 devices remain in the WAIT ALL OK state, effectively preventing a power-up sequence from starting.

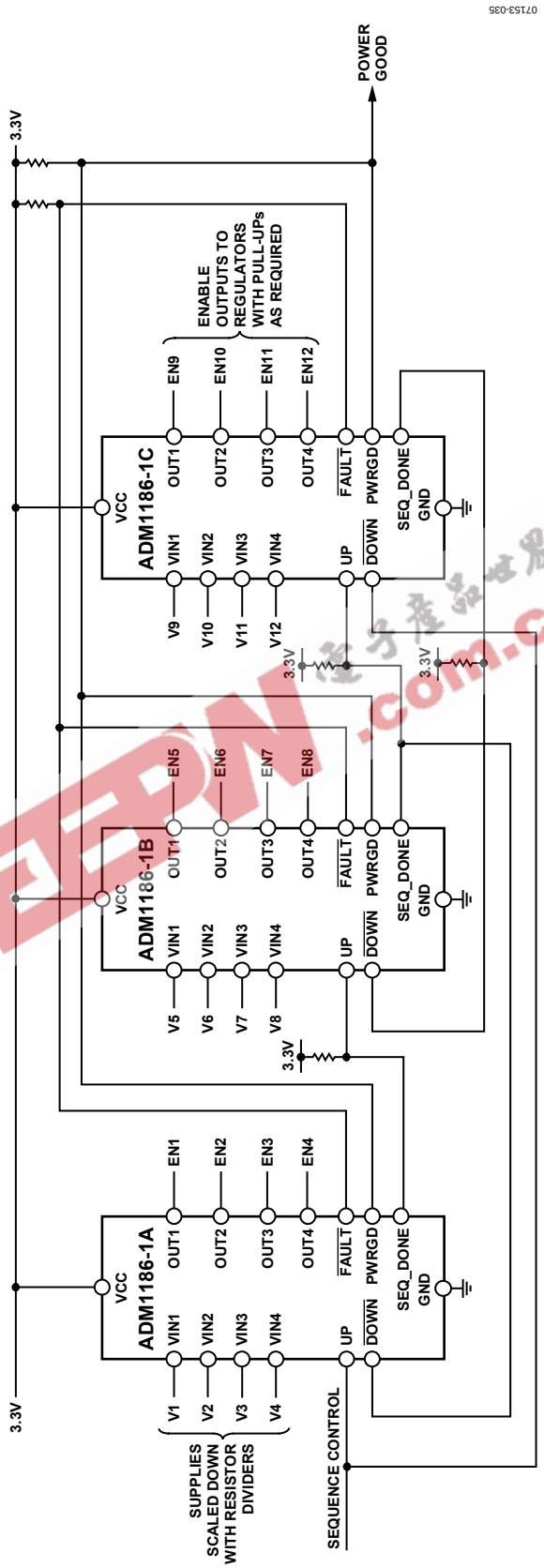


Figure 35. Cascading Multiple ADM1186-1 Devices, Option 1

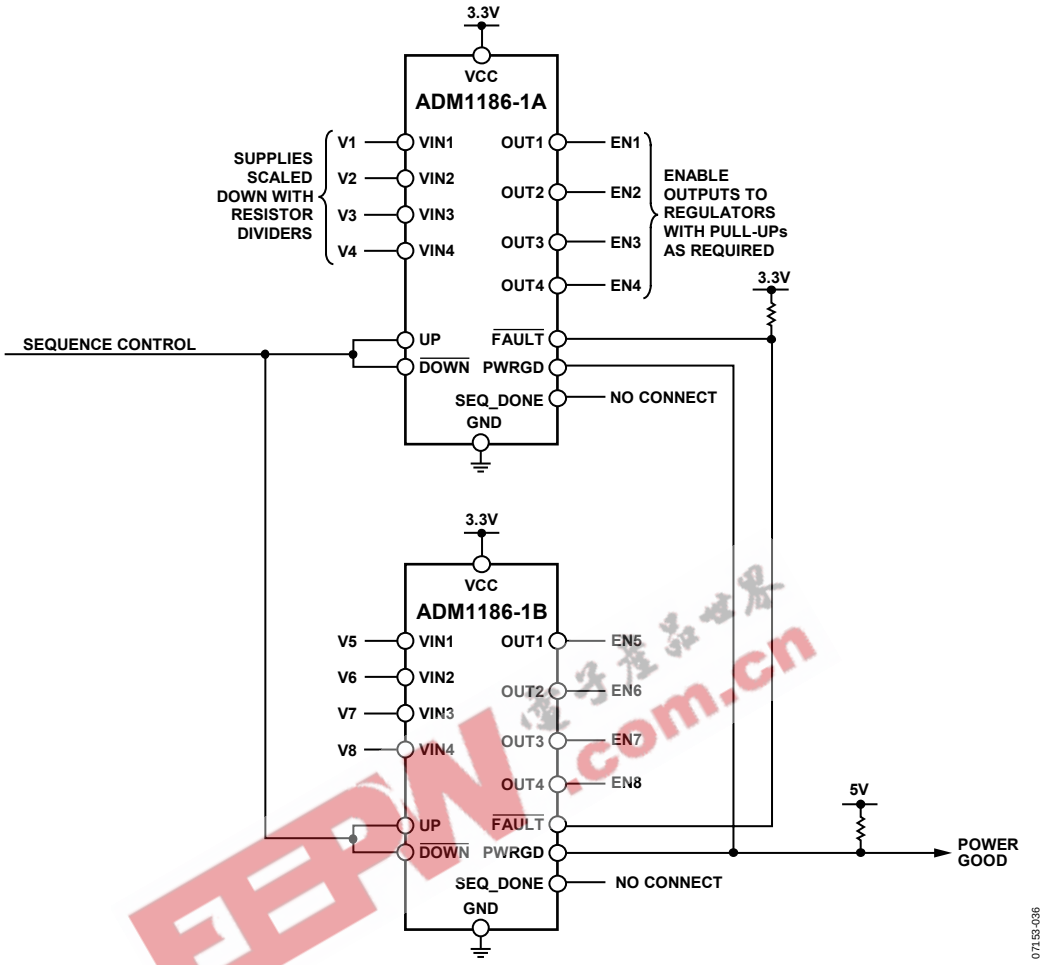
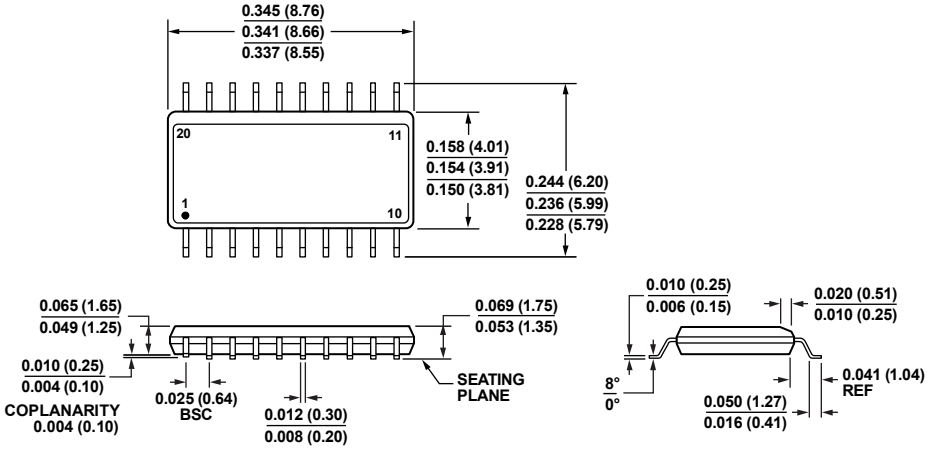


Figure 36. Cascading Multiple ADM1186-1 Devices, Option 2

OUTLINE DIMENSIONS

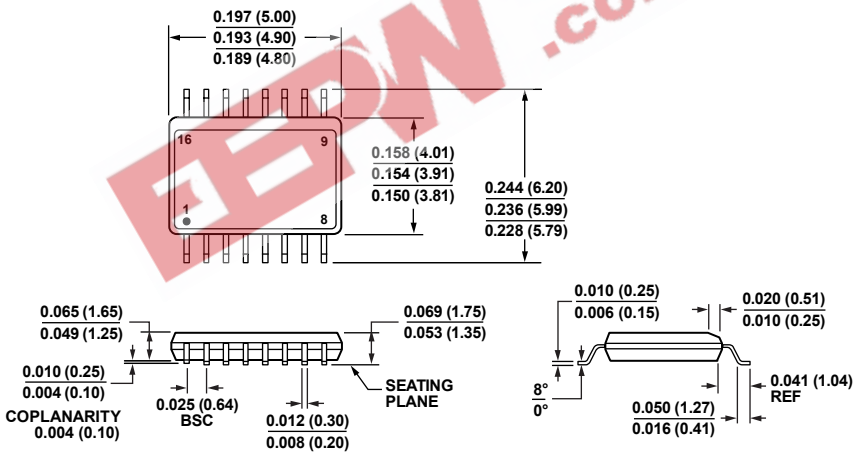


COMPLIANT TO JEDEC STANDARDS MO-137-AD

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETERS DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012808-A

Figure 37. 20-Lead Shrink Small Outline Package [QSOP] (RQ-20)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MO-137-AB

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETERS DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012808-A

Figure 38. 16-Lead Shrink Small Outline Package [QSOP] (RQ-16)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADM1186-1ARQZ[1]	−40°C to +85°C	20-Lead Shrink Small Outline Package [QSOP]	RQ-20
ADM1186-1ARQZ-REEL[1]	−40°C to +85°C	20-Lead Shrink Small Outline Package [QSOP]	RQ-20
ADM1186-2ARQZ[1]	−40°C to +85°C	16-Lead Shrink Small Outline Package [QSOP]	RQ-16
ADM1186-2ARQZ-REEL[1]	−40°C to +85°C	16-Lead Shrink Small Outline Package [QSOP]	RQ-16
EVAL-ADM1186-1EBZ[1]		Evaluation Kit	
EVAL-ADM1186-1MBZ[1]		Micro-Evaluation Kit	
EVAL-ADM1186-2EBZ[1]		Evaluation Kit	
EVAL-ADM1186-2MBZ[1]		Micro-Evaluation Kit	

[1] Z = RoHS Compliant Part.

NOTES

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