

101536

# Am25LS2519

Am25LS2519

Quad Register with Two Independently Controlled Three-State Outputs

### DISTINCTIVE CHARACTERISTICS

- Two sets of fully buffered three-state outputs
- Four D-type flip-flops
- Polarity control on W outputs
- Buffered common clock enable
- Buffered common asynchronous clear
- Separate buffered common output enable for each set of outputs

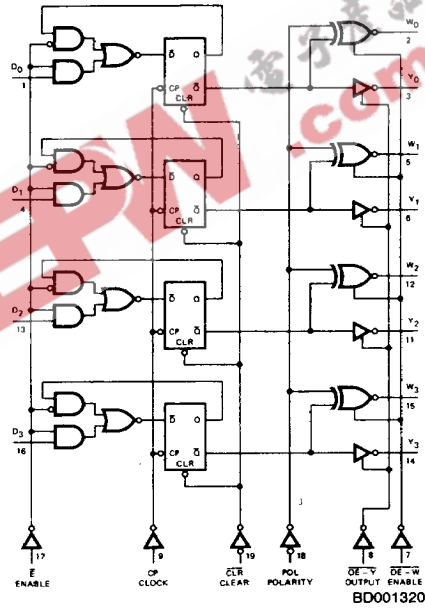
### GENERAL DESCRIPTION

The Am25LS2519 consists of four D-type flip-flops with a buffered common clock enable. Information meeting the set-up and hold time requirements on the D inputs is transferred to the flip-flop outputs on the LOW-to-HIGH transition of the clock. Data on the Q outputs of the flip-flops is enabled when the output control ( $\overline{OE}$ ) input is LOW. When the appropriate  $\overline{OE}$  input is HIGH, the outputs are in the high impedance state. Two independent sets of outputs – W and Y – are provided such

that the register can simultaneously and independently drive two buses. One set of outputs contains a polarity control such that the outputs can either be inverting or non-inverting.

The device also features an active LOW asynchronous clear. When the clear input is LOW, the Q output of the internal flip-flops are forced LOW independent of the other inputs. The Am25LS2519 is packaged in a space saving (0.3-inch row spacing) 20-pin package.

### BLOCK DIAGRAM



### RELATED PRODUCTS

Part No.	Description
Am25S18, Am2918	Quad D Register
Am25LS2518	Quad D Register

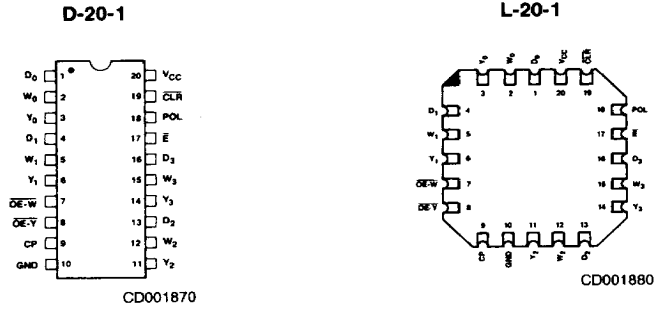
9

03660B

9-95

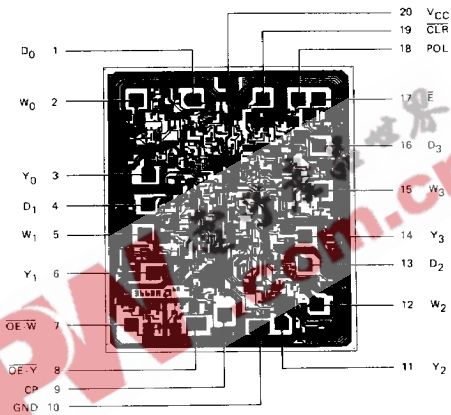
Refer to Page 13-1 for Essential Information on Military Devices

### CONNECTION DIAGRAM Top View



Note: Pin 1 is marked for orientation

### METALLIZATION AND PAD LAYOUT



DIE SIZE 0.083" x 0.099"

### ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am25LS2519

D

C

B

- Screening Option
  - Blank - Standard processing
  - B - Burn-in
- Temperature (See Operating Range)
  - C - Commercial (0°C to +70°C)
  - M - Military (-55°C to +125°C)

Package

- D - 20-pin Cerdip
- F - 20-pin flatpak
- L - 20-pin leadless chip carrier
- P - 20-pin plastic DIP
- X - Dice

Device type  
Quad D Register

#### Valid Combinations

Am25LS2519	PC
	DC, DM
	FM
	LC, LM
	XC, XM

#### Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

## PIN DESCRIPTION

Pin No.	Name	I/O	Description
	D <sub>i</sub>	I	Any of the four D flip-flop data lines.
17	E	I	Clock Enable. When LOW, the data is entered into the register on the next clock LOW-to-HIGH transition. When HIGH, the data in the register remains unchanged, regardless of the data in.
9	CP	I	Clock Pulse. Data is entered into the register on the LOW-to-HIGH transition.
7, 8	OE-W, OE-Y	O	Output Enable. When OE is LOW, the register is enable to the output. When HIGH, the output is in the high-impedance state. The OE-W controls the W set of outputs, and OE-Y controls the Y set.
	Y <sub>i</sub>	O	Any of the four non-inverting three-state output lines.
	W <sub>i</sub>	O	Any of the four three-state outputs with polarity control.
18	POL	O	Polarity Control. The W <sub>i</sub> outputs will be non-inverting when POL is LOW, and when it is HIGH, the outputs are inverting.
19	CLR	I	Asynchronous Clear. When CLR is LOW, the internal Q flip-flops are reset to LOW.

## FUNCTION TABLE

FUNCTION	INPUTS								INTERNAL	OUTPUTS	
	CP	D <sub>i</sub>	E	CLR	POL	OE-W	OE-Y	Q	W <sub>i</sub>	Y <sub>i</sub>	
Output Three-State Control	X	X	X	X	X	H	L	NC	Z	Enabled	
	X	X	X	X	X	L	H	NC	Z	Enabled	
	X	X	X	X	X	H	H	NC	Z	Enabled	
	X	X	X	X	X	L	L	NC	Z	Enabled	
W <sub>i</sub> Polarity	X	X	X	X	L	L	L	NC	Non-Inverting	Non-Inverting	
	X	X	X	X	H	L	L	NC	Inverting	Non-Inverting	
Asynchronous Clear	X	X	X	L	H	L	L	L	L	L	
	X	X	X	L	H	L	L	L	H	L	
Clock Enabled	↑	X	H	H	X	X	X	NC	NC	NC	
	↑	L	L	H	L	L	L	L	L	L	
	↑	L	L	H	L	L	L	L	H	L	
	↑	H	L	H	L	L	L	H	H	H	

L = LOW

H = HIGH

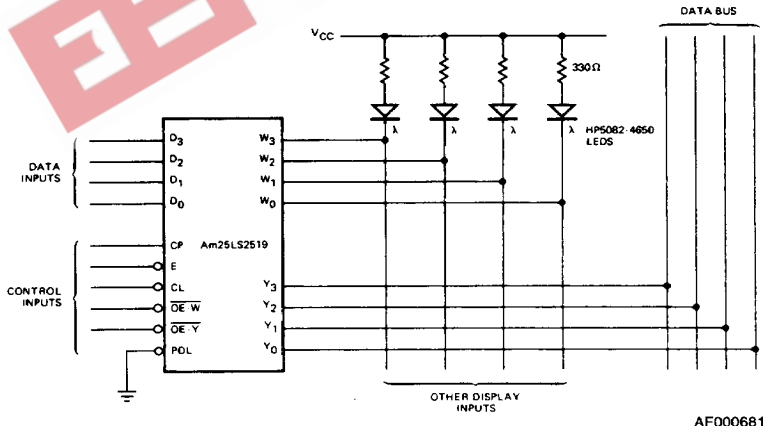
Z = High-Impedance

X = Don't Care

NC = No Change

↑ = LOW to HIGH Transition

## APPLICATION



Convenient Register Content Monitor or Test Point

**ABSOLUTE MAXIMUM RATINGS**

Storage Temperature .....	-65°C to +150°C
Ambient Temperature Under Bias .....	-55°C to +125°C
Supply Voltage to Ground Potential	
Continuous .....	-0.5V to +7.0V
DC Voltage Applied to Outputs For	
High Output State .....	-0.5V to +V <sub>CC</sub> max
DC Input Voltage .....	-0.5V to +7.0V
DC Output Current, Into Outputs .....	30mA
DC Input Current .....	-30mA to +5.0mA

Stresses above those listed under **ABSOLUTE MAXIMUM RATINGS** may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

**OPERATING RANGES**

Commercial (C) Devices	
Temperature .....	0°C to +70°C
Supply Voltage .....	+4.75V to +5.25V

Military (M) Devices	
Temperature .....	-55°C to +125°C
Supply Voltage .....	+4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

**DC CHARACTERISTICS** over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)		Min	Typ (Note 1)	Max	Units
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = MIN V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	MIL, I <sub>OH</sub> = -1.0mA COM'L, I <sub>OH</sub> = -2.6mA	2.4	3.4		Volts
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = MIN V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 4.0 mA I <sub>OL</sub> = 8.0mA I <sub>OL</sub> = 12mA			0.4 0.45 0.5	Volts
V <sub>IH</sub>	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V <sub>IL</sub>	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.7 0.8	Volts
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18mA				-1.5	Volts
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4V				-0.36	mA
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7V				20	μA
I <sub>I</sub>	Input HIGH Current	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0V				0.1	mA
I <sub>OZ</sub>	Off-State (High-Impedance) Output Current	V <sub>CC</sub> = MAX	V <sub>O</sub> = 0.4V V <sub>O</sub> = 2.4V			-20 20	μA
I <sub>SC</sub>	Output Short Circuit Current (Note 3)	V <sub>CC</sub> = MAX		-15		-85	mA
I <sub>CC</sub>	Power Supply Current (Note 4)	V <sub>CC</sub> = MAX	MIL COM'L		24 24	36 39	mA

- Notes: 1. Typical limits are at V<sub>CC</sub> = 5.0V, 25°C ambient and maximum loading.  
 2. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.  
 3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.  
 4. Inputs grounded; outputs open.

SWITCHING CHARACTERISTICS ( $T_A = +25^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V}$ )

Parameters	Description	Test Conditions	Min	Typ	Max	Units
$t_{PHL}$	Clock to $Y_i$	$C_L = 15\text{pF}$ $R_L = 2.0\text{k}\Omega$		22	33	ns
$t_{PLH}$				20	30	
$t_{PLH}$	Clock to $W_i$ (Either Polarity)			24	36	ns
$t_{PHL}$				24	36	
$t_{PHL}$	Clear to $Y_i$			29	43	ns
$t_{PLH}$				25	37	
$t_{PHL}$	Clear to $W_i$			30	45	ns
$t_{PLH}$				23	34	
$t_{PHL}$	Polarity to $W_i$			25	37	ns
$t_{PLH}$				18		
$t_{pw}$	Clear			15		ns
$t_{pw}$			Clock Pulse Width	LOW	18	
				HIGH		
$t_s$	Data			15		ns
$t_h$	Data		5		ns	
$t_s$	Data Enable		20		ns	
$t_h$	Data Enable		0		ns	
$t_s$	Set-up Time, Clear Recovery (Inactive) to clock		20	15	ns	
$t_{ZH}$	Output Enable to W or Y			11	17	ns
$t_{ZL}$				13	20	
$t_{HZ}$	Output Enable to W or Y	$C_L = 5.0\text{pF}$ $R_L = 2.0\text{k}\Omega$		13	20	ns
$t_{LZ}$				11	17	
$f_{max}$	Maximum Clock Frequency (Note 1)	$C_L = 15\text{pF}$ $R_L = 2.0\text{k}\Omega$	35	45		MHz

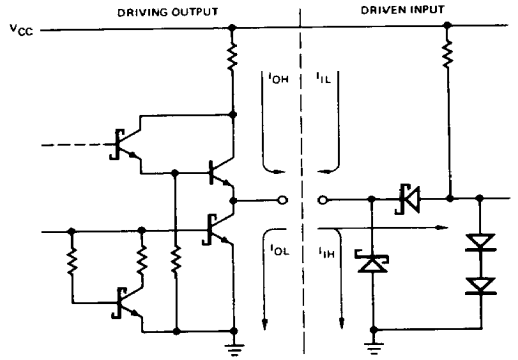
Note 1. Per industry convention,  $f_{max}$  is the worst case value of the maximum device operating frequency with no constraints on  $t_r$ ,  $t_f$ , pulse width or duty cycle.

## SWITCHING CHARACTERISTICS over operating range unless otherwise specified\*

Parameters	Description	Test Conditions	COMMERCIAL		MILITARY		Units
			Am25LS2519		Am25LS2519		
			Min	Max	Min	Max	
$t_{PLH}$	Clock to $Y_i$	$C_L = 50\text{pF}$ $R_L = 2.0\text{k}\Omega$		39		42	ns
$t_{PHL}$				39		45	
$t_{PLH}$	Clock to $W_i$ (Either Polarity)			41		43	ns
$t_{PHL}$				44		48	
$t_{PHL}$	Clear to $Y_i$			52		58	ns
$t_{PLH}$				42		43	
$t_{PHL}$	Clear to $W_i$			51		53	ns
$t_{PLH}$				41		45	
$t_{PHL}$	Polarity to $W_i$			42		44	ns
$t_{PLH}$				20		20	
$t_{pw}$	Clear			20		20	ns
$t_{pw}$			Clock	LOW	20		
				HIGH	20		20
$t_s$	Data			15		15	ns
$t_h$	Data		10		10	ns	
$t_s$	Data Enable		25		25	ns	
$t_h$	Data Enable		0		0	ns	
$t_s$	Set-up Time, Clear Recovery (Inactive) to Clock		23		24	ns	
$t_{ZH}$	Output Enable to $W_i$ or $Y_i$			24		27	ns
$t_{ZL}$				29		35	
$t_{HZ}$	Output Enable to $W_i$ or $Y_i$	$C_L = 5.0\text{pF}$ $R_L = 2.0\text{k}\Omega$		33		45	ns
$t_{LZ}$				22		26	
$f_{max}$	Maximum Clock Frequency (Note 1)	$C_L = 5.0\text{pF}$ $R_L = 2.0\text{k}\Omega$	30		25		MHz

\*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

### Am25LS2519 LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



IC000090

Note: Actual current flow direction shown.

EEPW.com.cn 电子产品世界