



# AM26C32

## QUADRUPLE DIFFERENTIAL LINE RECEIVER

SLLS104I – DECEMBER 1990 – REVISED SEPTEMBER 2004

### description/ordering information (continued)

#### ORDERING INFORMATION

T <sub>A</sub>	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP (N)	Tube of 25	AM26C32CN	AM26C32CN
	SOIC (D)	Tube of 40	AM26C32CD	AM26C32C
		Reel of 2500	AM26C32CDR	
	SOP (NS)	Reel of 2000	AM26C32CNSR	26C32
-40°C to 85°C	PDIP (N)	Tube of 25	AM26C32IN	AM26C32IN
	SOIC (D)	Tube of 40	AM26C32ID	AM26C32I
		Reel of 2500	AM26C32IDR	
	SOP (NS)	Reel of 2000	AM26C32INSR	26C32I
TSSOP (PW)	Tube of 90	AM26C32IPW	26C32I	
-40°C to 125°C	SOIC (D)	Tube of 40	AM26C32QD	AM26C32QD
-55°C to 125°C	CDIP (J)	Tube of 25	AM26C32MJ	AM26C32MJ
	CFP (W)	Tube of 150	AM26C32MW	AM26C32MW
	LCCC (FK)	Tube of 55	AM26C32MFK	AM26C32MFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

#### FUNCTION TABLE (each receiver)

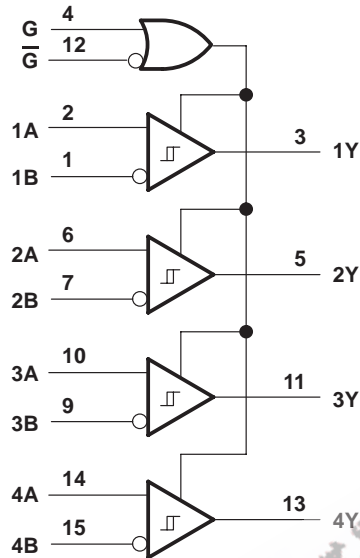
DIFFERENTIAL INPUT	ENABLES		OUTPUT Y
	G	$\bar{G}$	
$V_{ID} \geq V_{IT+}$	H	X	H
	X	L	H
$V_{IT-} < V_{ID} < V_{IT+}$	H	X	?
	X	L	?
$V_{ID} \leq V_{IT-}$	H	X	L
	X	L	L
X	L	H	Z

H = high level, L = low level, X = irrelevant  
Z = high impedance (off), ? = indeterminate

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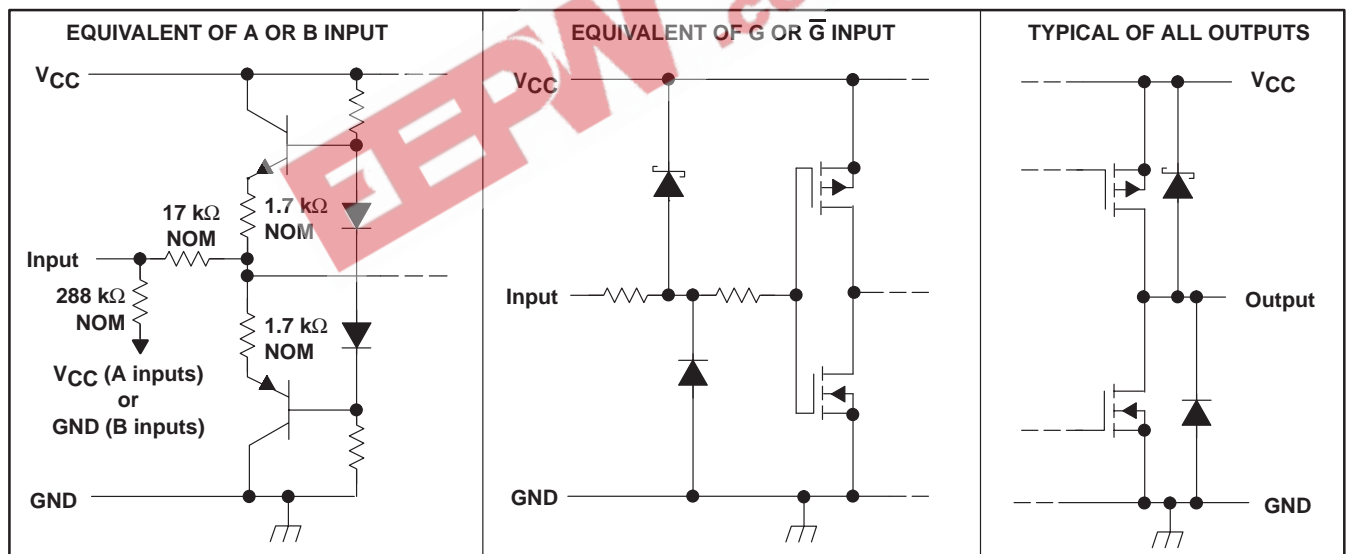
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## logic diagram (positive logic)



Pin numbers shown are for the D, J, N, NS, PW, and W packages.

## schematics





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electrical characteristics over recommended ranges of  $V_{CC}$ ,  $V_{IC}$ , and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{IT+}$	Differential input high-threshold voltage	$V_O = V_{OH(min)}$ , $I_{OH} = -440 \mu A$	$V_{IC} = -7 V$ to $7 V$			0.2	V
			$V_{IC} = 0$ to $5.5 V$			0.1	
$V_{IT-}$	Differential input low-threshold voltage	$V_O = 0.45 V$ , $I_{OL} = 8 mA$	$V_{IC} = -7 V$ to $7 V$			$-0.2\ddagger$	V
			$V_{IC} = 0$ to $5.5 V$			$-0.1\ddagger$	
$V_{hys}$	Hysteresis voltage ( $V_{IT+} - V_{IT-}$ )				60		mV
$V_{IK}$	Enable input clamp voltage	$V_{CC} = 4.5 V$ ,	$I_I = -18 mA$			-1.5	V
$V_{OH}$	High-level output voltage	$V_{ID} = 200 mV$ ,	$I_{OH} = -6 mA$	3.8			V
$V_{OL}$	Low-level output voltage	$V_{ID} = -200 mV$ ,	$I_{OL} = 6 mA$		0.2	0.3	V
$I_{OZ}$	Off-state (high-impedance state) output current	$V_O = V_{CC}$ or GND			$\pm 0.5$	$\pm 5$	$\mu A$
$I_I$	Line input current	$V_I = 10 V$ ,	Other input at $0 V$			1.5	mA
		$V_I = -10 V$ ,	Other input at $0 V$			-2.5	
$I_{IH}$	High-level enable current	$V_I = 2.7 V$				20	$\mu A$
$I_{IL}$	Low-level enable current	$V_I = 0.4 V$				-100	$\mu A$
$r_i$	Input resistance	One input to ground		12	17		k $\Omega$
$I_{CC}$	Supply current	$V_{CC} = 5.5 V$			10	15	mA

† All typical values are at  $V_{CC} = 5 V$ ,  $V_{IC} = 0$ , and  $T_A = 25^\circ C$ .

‡ The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage.

switching characteristics over recommended ranges of operation conditions,  $C_L = 50 pF$  (unless otherwise noted)

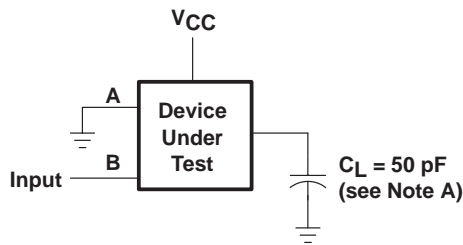
PARAMETER	TEST CONDITIONS	AM26C32C AM26C32I			AM26C32Q AM26C32M			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
$t_{PLH}$	Propagation delay time, low- to high-level output	9	17	27	9	17	27	ns
$t_{PHL}$	Propagation delay time, high- to low-level output							
$t_{TLH}$	Output transition time, low- to high-level output	4	4	9	4	4	10	ns
$t_{THL}$	Output transition time, high- to low-level output							
$t_{PZH}$	Output enable time to high level	13	13	22	13	13	22	ns
$t_{PZL}$	Output enable time to low level							
$t_{PHZ}$	Output disable time from high level	13	13	22	13	13	26	ns
$t_{PLZ}$	Output disable time from low level							

† All typical values are at  $V_{CC} = 5 V$ ,  $T_A = 25^\circ C$ .

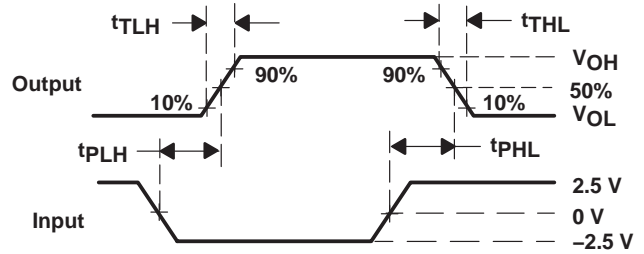
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## PARAMETER MEASUREMENT INFORMATION



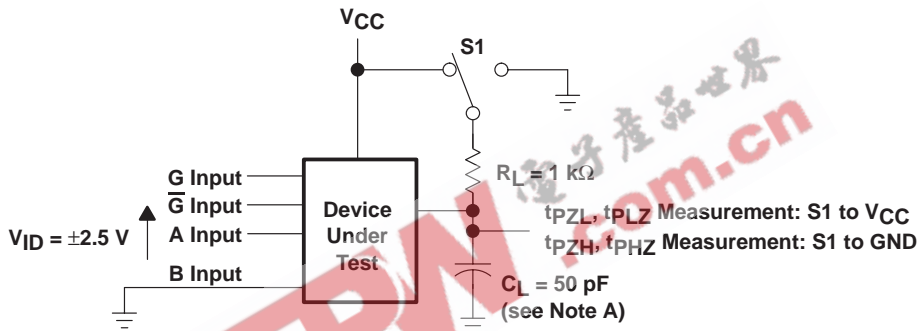
TEST CIRCUIT



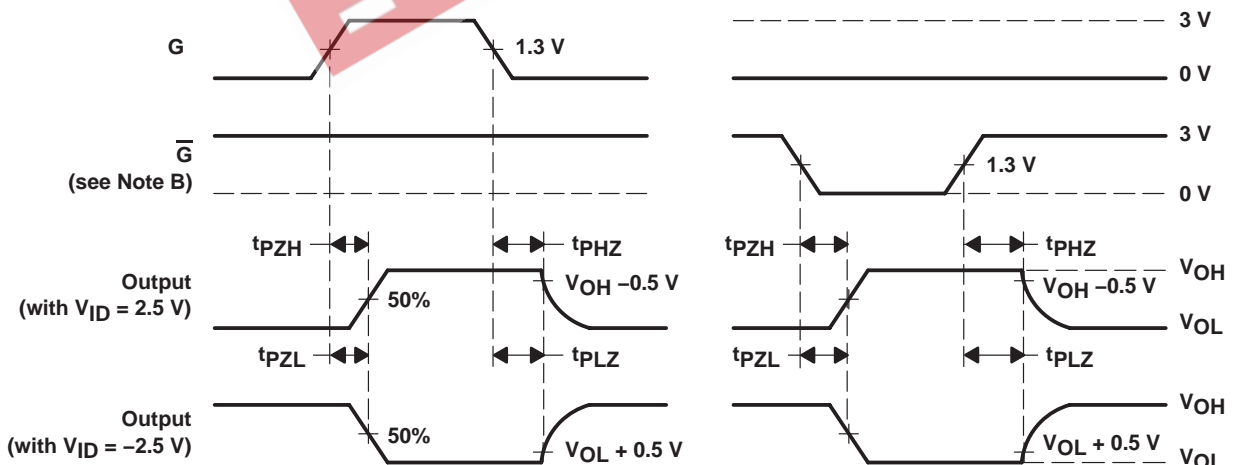
VOLTAGE WAVEFORMS

NOTE A:  $C_L$  includes probe and jig capacitance.

Figure 1. Switching Test Circuit and Voltage Waveforms



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A.  $C_L$  includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle  $\leq 50\%$ ,  $t_r = t_f = 6 ns$ .

Figure 2. Enable/Disable Time Test Circuit and Output Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
5962-9164001Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-9164001QEA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
5962-9164001QFA	ACTIVE	CFP	W	16	1	TBD	A42 SNPB	N / A for Pkg Type
AM26C32CD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26C32CDBLE	OBSOLETE	SSOP	DB	16		TBD	Call TI	Call TI
AM26C32CDE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26C32CDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26C32CDRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26C32CN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
AM26C32CNE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
AM26C32CNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26C32CNSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26C32ID	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26C32IDBLE	OBSOLETE	SSOP	DB	16		TBD	Call TI	Call TI
AM26C32IDE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26C32IDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26C32IDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26C32IDRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26C32IDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26C32IN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
AM26C32INE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
AM26C32INSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26C32INSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26C32IPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26C32IPWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26C32IPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26C32IPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
AM26C32MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
AM26C32MJB	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
AM26C32MWB	ACTIVE	CFP	W	16	1	TBD	A42 SNPB	N / A for Pkg Type
AM26C32QD	ACTIVE	SOIC	D	16	40	TBD	CU NIPDAU	Level-1-220C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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J (R-GDIP-T\*\*)  
14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



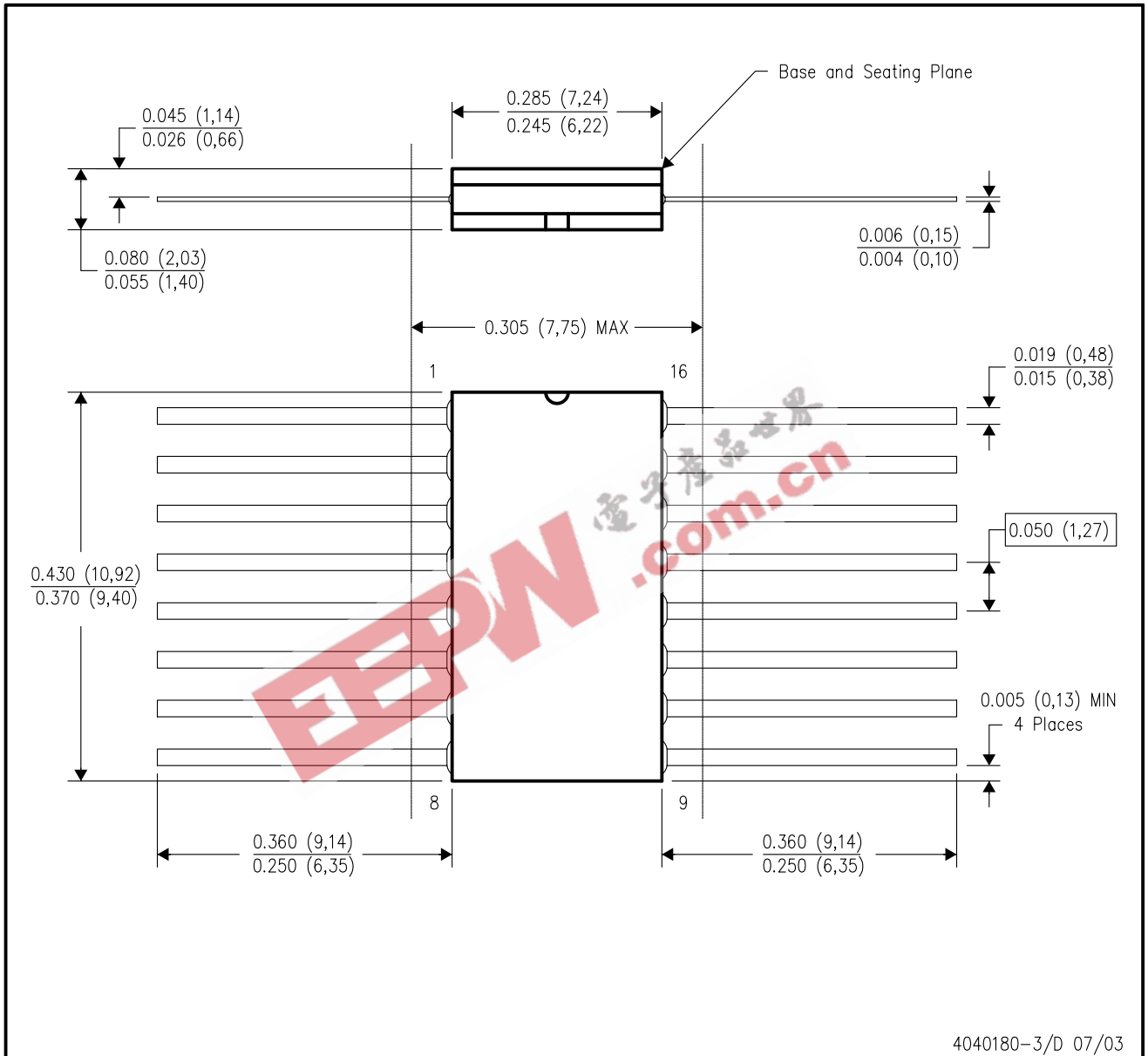
4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

# MECHANICAL DATA

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK

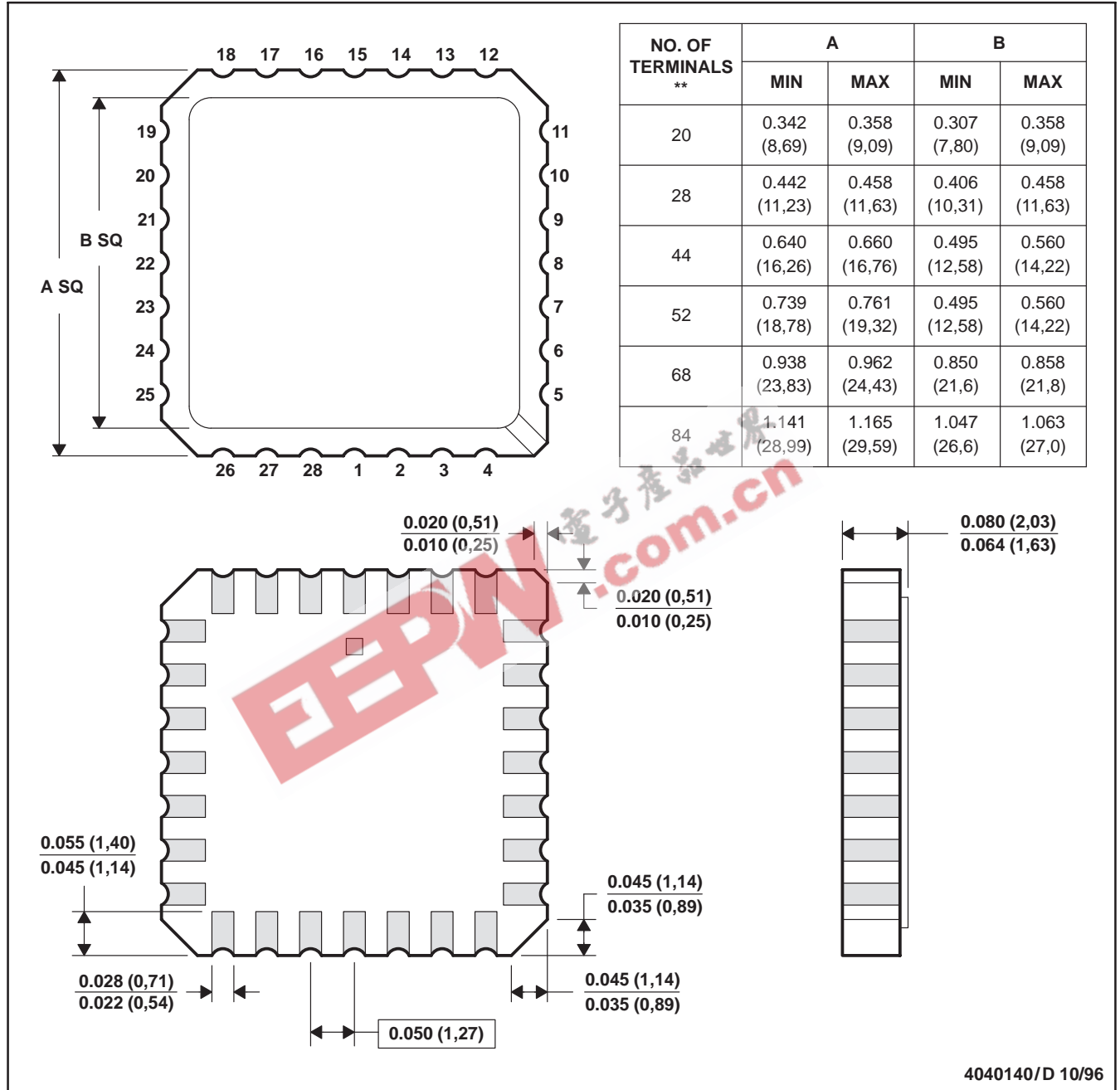


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



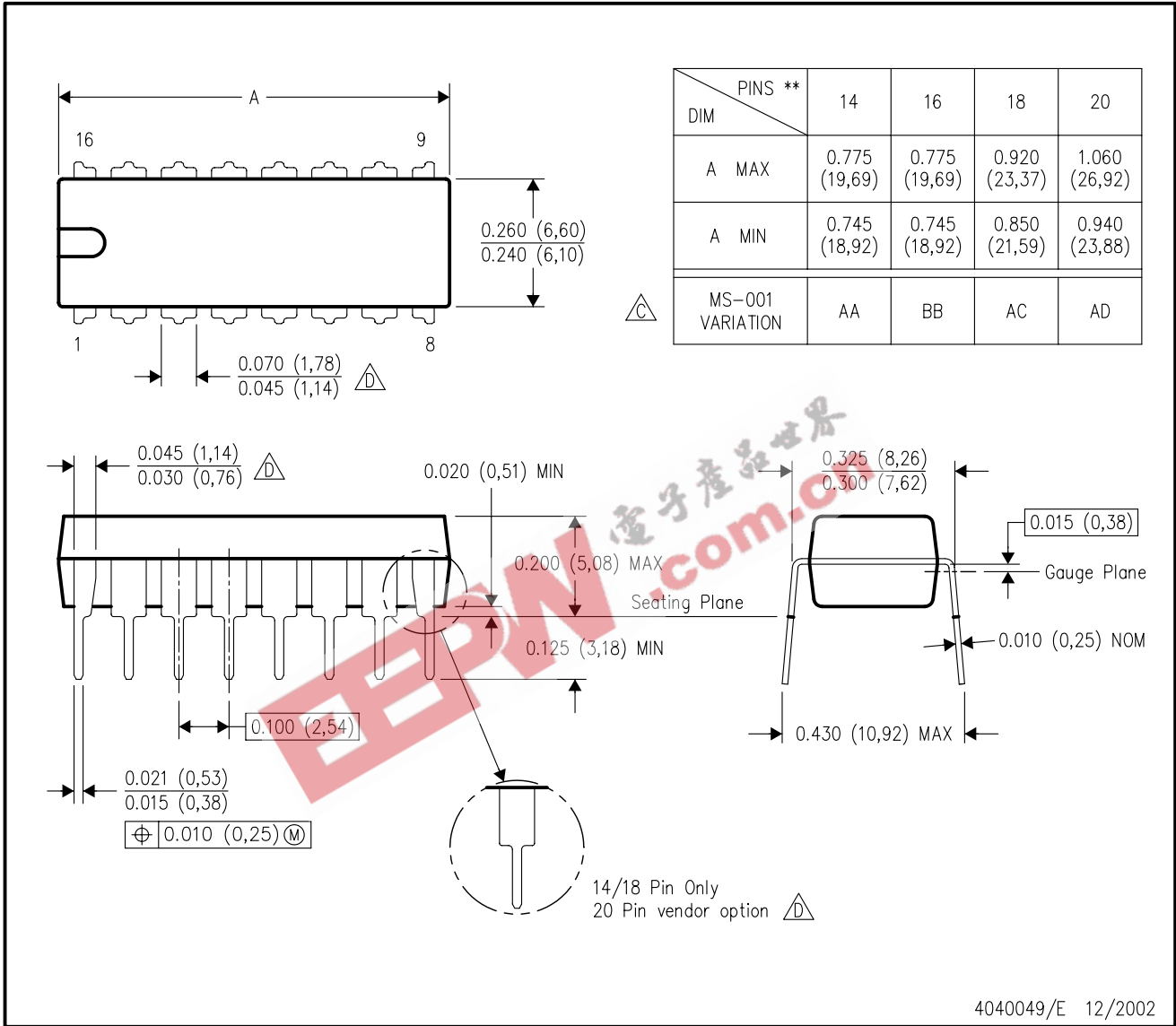
- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a metal lid.
  - D. The terminals are gold plated.
  - E. Falls within JEDEC MS-004

# MECHANICAL DATA

## N (R-PDIP-T\*\*)

## PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

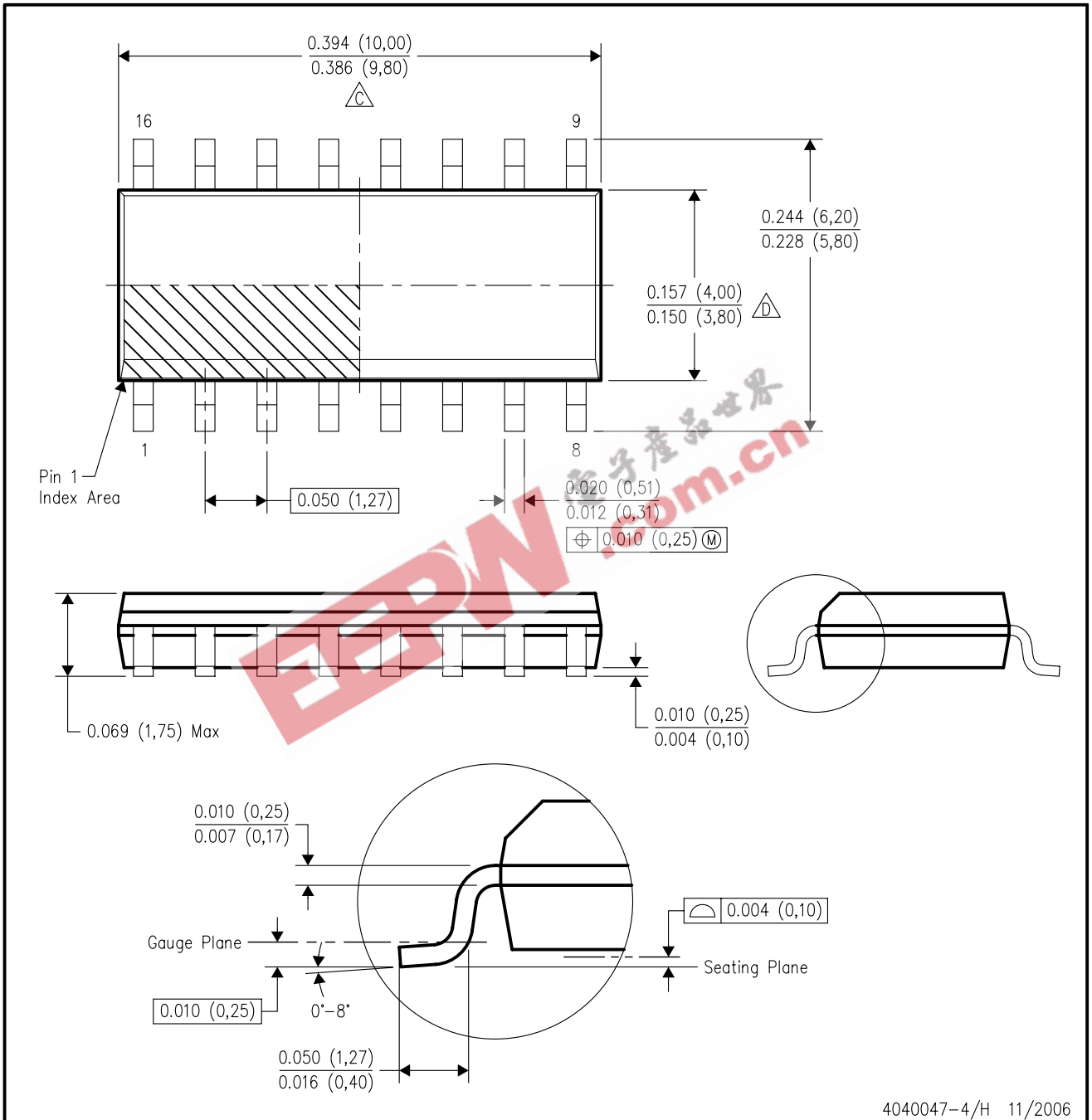


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

# MECHANICAL DATA

## D (R-PDSO-G16)

## PLASTIC SMALL-OUTLINE PACKAGE



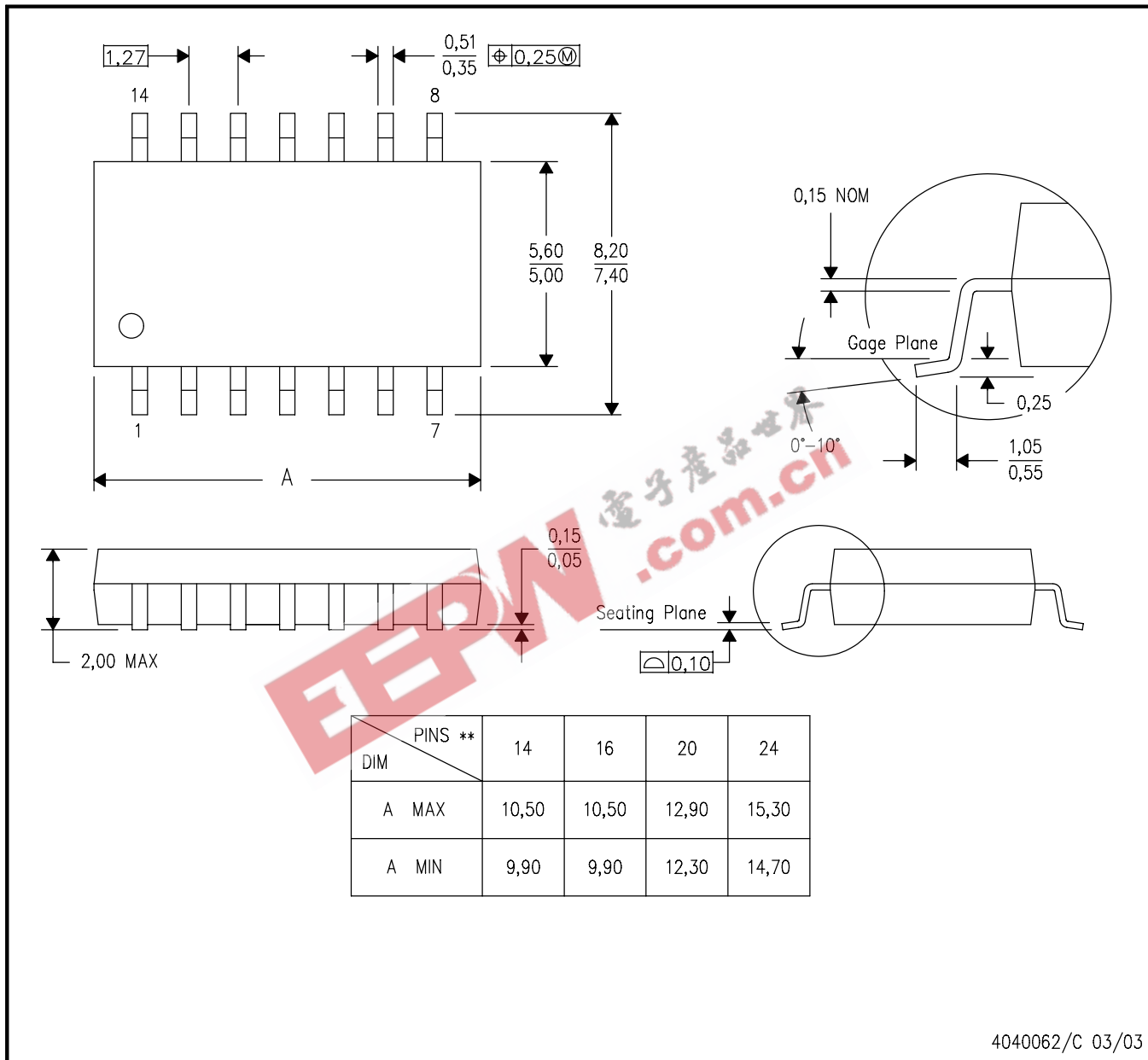
- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
  - E. Reference JEDEC MS-012 variation AC.

## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

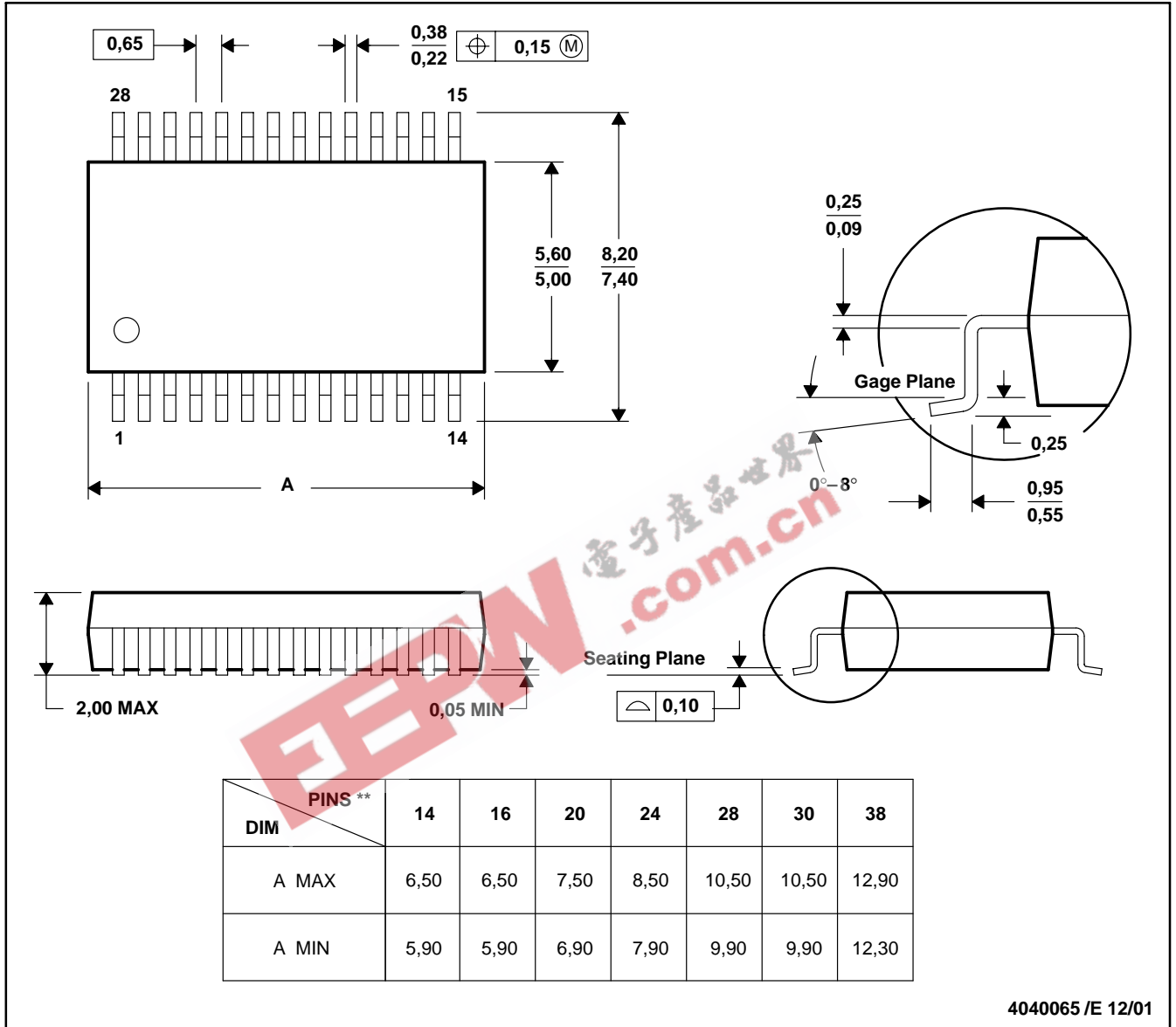
# MECHANICAL DATA

MSS0002E – JANUARY 1995 – REVISED DECEMBER 2001

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

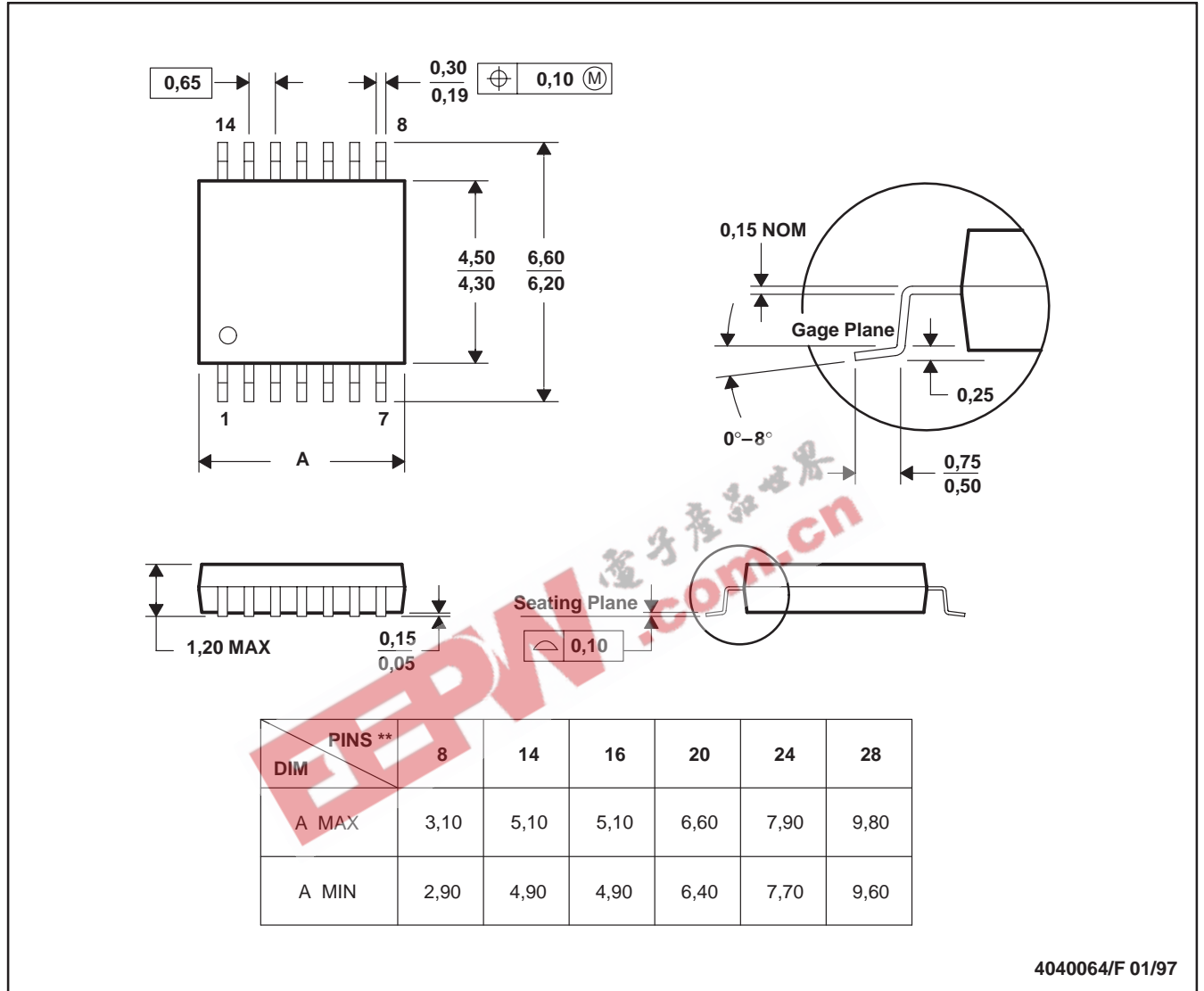
# MECHANICAL DATA

MTSS001C – JANUARY 1995 – REVISED FEBRUARY 1999

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153



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DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>	Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>	Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>	Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
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