2048-bits Serial Electrically Erasable PROM

AM93LC56

■ Features

- State-of-the-art architecture
  - Non-volatile data storage
  - Standard voltage and low voltage operation
    Vcc: 2.7V ~ 5.5V
  - Full TTL compatible inputs and outputs
  - Auto increment read for efficient data dump
- Hardware and software write protection
  - Defaults to write-disabled state at power up
  - Software instructions for write-enable/disable
  - VCC level verification before self-timed programming cycle
- Advanced low voltage CMOS EEPROM technology
- Versatile, easy-to-use interface
  - Self-timed programming cycle
  - Automatic erase-before-write
  - Programming status indicator
  - Word and chip erasable
  - Stop SK anytime for power savings
- Durability and reliability
  - 40 years data retention
  - Minimum of 1M write cycles per word
  - Unlimited read cycles
  - ESD protection

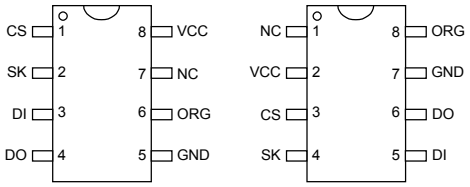
■ General Description

The AM93LC56 is the 2048-bit non-volatile serial EEPROM. It is manufactured by using ATC's advanced CMOS EEPROM technology. The AM93LC56 provides efficient non-volatile read/write memory arranged as 128 words of 16 bits each when the ORG Pin is connected to VCC and 256 words of 8 bits each when it is tied to ground. The instruction set includes read, write, and write enable/disable functions. The data out pin (DO) indicates the status of the device during the self-timed non-volatile programming cycle.

The self-timed write cycle includes an automatic erase-before-write capability. Only when the chip is in the WRITE ENABLE state and proper VCC operation range is the WRITE instruction accepted and thus to protect against inadvertent writes. Data is written in 16 bits per write instruction into the selected register. If Chip Select (CS) is brought HIGH after initiation of the write cycle, the Data Output (DO) pin will indicate the READY/BUSY status of the chip.

The AM93LC56 is available in space-saving 8-lead PDIP, 8-lead SOP and rotated 8-lead SOP package.

■ Connection Diagram



PDIP-8L / SOP-8L　　Rotated SOP-8L

■ Pin Assignments

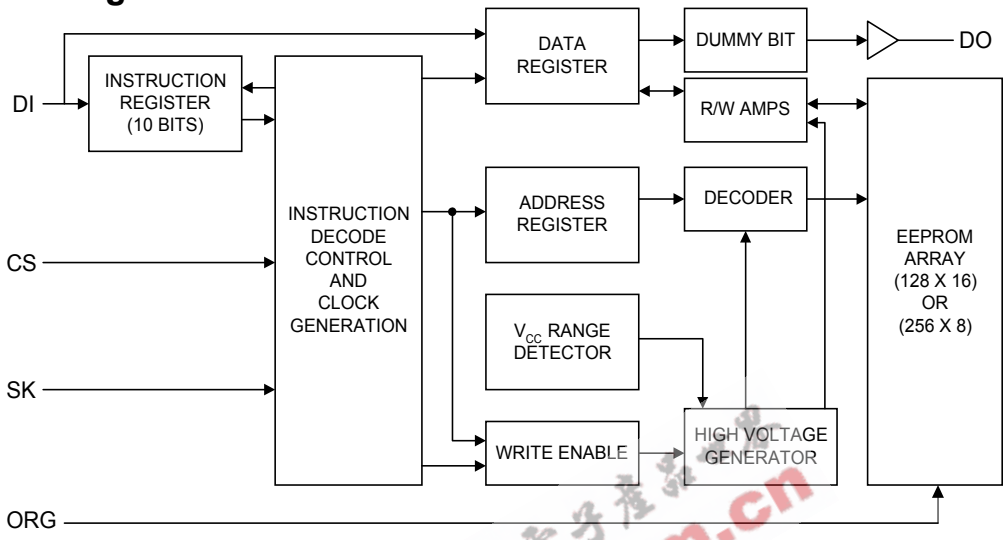
Name	Description
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
VCC	Power Supply
NC	No Connection
ORG	Internal Organization

■ Ordering Information

AM 93 L C 56 X XX X

Operating Voltage	Type	Temp. grade	Package	Packing
LC : 2.7~5.5V,CMOS	56: 2K	Blank : 0°C ~ +70°C I : −40°C ~ +85°C V : −40°C ~ +125°C	S : SOP-8L GS8: SOP-8L,G type N : PDIP-8L	Blank : Tube A : Taping

■ Block Diagrams



■ Absolute Maximum Ratings

Characteristics	Symbol	Values	Unit
Storage Temperature	T_S	-65 to + 125	°C
Voltage with Respect to Ground		-0.3 to + 6.5	V

NOTE: These are STRESS rating only. Appropriate conditions for operating these devices given elsewhere may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

■ Operating Conditions

Temperature under bias	Values	Unit
AM93LC56	0 to + 70	°C
AM93LC56I	-40 to + 85	°C
AM93LC56V	-40 to +125	°C

■ DC Electrical Characteristics (Vcc =2.7~5.5V, Ta = 25°C , unless otherwise noted)

Parameter	Symbol	Conditions	Min	Max	Units
Operating current**	I_{CC}	CS=V_{IH}, SK=1MHz CMOS input levels		3	mA
Standby current	I_{SB}	CS=DI=SK=0V		10	µA
Input leakage	I_{IL}	V_{IN} = 0V to $V_{CC(CS,SK,DI)}$	-1	1	µA
Output leakage	I_{OL}	V_{OUT} = 0V to V_{CC}, CS=0V	-1	1	µA
Input low voltage**	V_{IL}	V_{CC} = 3V ± 10%	-0.1	0.15 V_{CC}	V
		V_{CC} = 5V ± 10%	-0.1	0.8	
Input high voltage**	V_{IH}	V_{CC} = 3V ± 10%	0.8 V_{CC}	V_{CC} +0.2	V
		V_{CC} = 5V ± 10%	2	V_{CC} +0.2	
Output low voltage	V_{OL1}	I_{OL} = 2.1mA TTL, V_{CC}=5V ± 10%		0.4	V
Output high voltage	V_{OH1}	I_{OH} = -400uA TTL, V_{CC}=5V ± 10%	2.4		V
Output low voltage	V_{OL2}	I_{OL} = 10uA CMOS		0.2	V
Output high voltage		I_{OH} = -10uA CMOS	V_{CC} -0.2		V

Note **: I_{CC} , V_{IL} min and V_{IH} max are for reference only and are not tested

■ AC Electrical Characteristics (Vcc = 2.7V ~ 5.5V, Ta = 25°C , unless otherwise noted)

Parameter	Symbol	Conditions	AM93LC56		Units
			Min	Max	
SK Clock Frequency	F_{SK}		0	1	MHz
SK High Time	T_{SKH}		250		ns
SK Low Time	T_{SKL}		250		ns
Minimum CS Low Time	T_{CS}		250		ns
CS Setup Time	T_{CSS}	Relative to SK	50		ns
DI Setup Time	T_{DIS}	Relative to SK	100		ns
CS Hold Time	T_{cSH}	Relative to SK	0		ns
DI Hold Time	T_{DIH}	Relative to SK	100		ns
Output Delay to "1"	T_{pD1}	AC Test		500	ns
Output Delay to "0"	T_{pD0}	AC Test		500	ns
CS to Status Valid	T_{SV}	AC Test CL = 100pF		500	ns
CS to DO in 3-state	T_{dF}	CS = VIL		100	ns
Write Cycle Time	T_{wP}			10	ms
5V, 25°C, Page Mode	Endurance**		1M		write cycles

Note : The parameter is characterized and isn't 100% tested.

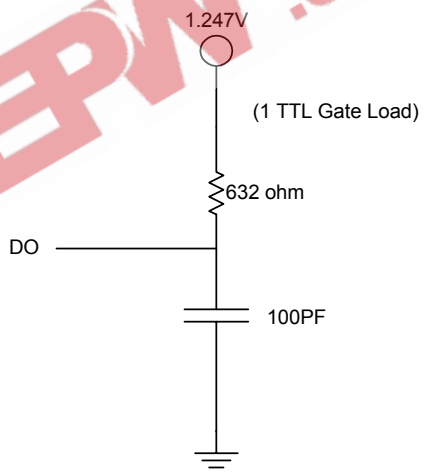


FIGURE 1. AC TEST CONDITIONS

■ Instruction Set

Instruction	Start Bit	OP Code	Address		Input Data	
			x 8	x 16	x 8	x 16
READ	1	10	A_7 - A_0	A_6 - A_0		
WEN (Write Enable)	1	00	11 XXXXXX	11XXXXX		
WRITE	1	01	A_7 - A_0	A_6 - A_0	D_7 – D_0	D_{15} - D_0
WRALL (Write All Registers)	1	00	01XXXXXX	01XXXXX	D_7 – D_0	D_{15} - D_0
WDS (Write Disable)	1	00	00 XXXXXX	00XXXXX		
ERASE	1	11	A_7 - A_0	A_6 - A_0		
ERAL (Erase All Registers)	1	00	10 XXXXXX	10XXXXX		

■ Pin Capacitance ** (Ta=25°C , f=1MHz)

Symbol	Parameter	Max	Units
C_{OUT}	Output capacitance	5	pF
C_{IN}	Input capacitance	5	pF

Note ** : The parameter is characterized and isn't 100% tested.

■ Functional Descriptions

Applications
The AM93LC56 is ideal for high volume applications requiring low power and low density storage. This device uses a low cost, space saving 8-pin package. Typical applications include robotics, alarm devices, electronic locks, meters and instrumentation settings such as LAN cards, monitors and MODEM.

Endurance and Data Retention
The AM93LC56 is designed for applications requiring up to 1M programming cycles (WRITE, WRALL, EARSE and ERALL). It provides 40 years of secure data retention.

Device Operation
The AM93LC56 is controlled by seven 10-bit instructions. Instructions are clocked in (serially) on the DI pin. Each instruction begins with a logical "1" (the start bit). This is followed by the opcode (2 bits), the address field (7 bits), and data, if appropriate. The clock signal (SK) may be halted at any time and the AM93LC56 will remain in its last state. This allows full static flexibility and maximum power conservation.

Read (READ)
The READ instruction is the only instruction that outputs serial data on the DO pin. After the read instruction and address have been decoded, data is transferred from the selected memory register into a 8-bit or 16-bit serial shift register. (Please note that one logical "0" bit precedes the actual 8-bit or 16-bit output data string.) The output on DO changes during the rising edge transitions of SK. (Shown in Figure 3.)

Auto Increment Read Operations
Sequential read is possible, since the AM93LC56 has been designed to output a continuous stream of memory content in response to a single read operation instruction. To utilize this function, the system asserts a read instruction specifying a start location address. Once the 8-bit or 16-bit of the addressed word have been clocked out, the data in consecutively higher address locations is output. The address will wrap around continuously with CS high until the chip select (CS) control pin is brought low. This allows for single instruction data dumps to be executed with a minimum of firmware overhead.

Write Enable (WEN)
Before any device programming (WRITE, WRALL, ERASE, and ERAL) can be done, the WRITE ENABLE (WEN) instruction must be executed first. When Vcc is applied, this device powers up in the WRITE DISABLE state. The device then remains in a WRITE DISABLE state until a WEN instruction is executed. Thereafter the device remains enabled until a WDS instruction is executed or until Vcc is removed. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction.) (Shown in Figure 4.)

Write Disable (WDS)
The WRITE DISABLE (WDS) instruction disables all programming capabilities. This protects the entire part against accidental modification of data until a WEN instruction is executed. (When Vcc is applied, this part powers up in the WRITE DISABLE state.) To protect data, a WDS instruction should be executed upon completion of each programming operation. (NOTE: Neither the WEN nor the WDS instruction has any effect on the READ instruction.) (Shown in Figure 5.)

■ Functional Description (Continued)

Write (WRITE)
The WRITE instruction includes 8-bit or 16-bit of data to be written into the specified register. After the last data bit has been applied to DI, and before the next rising edge of SK, CS must be brought LOW. The falling edge of CS initiates the self-timed programming cycle.

After a minimum wait of 250ns (5V operation) from the falling edge of CS (tcs), DO will indicate the READY/BUSY status of the chip if CS is brought HIGH. This means that logical "0" implies the programming is still in progress while logical "1" indicates the selected register has been written, and the part is ready for another instruction. (See Figure 6)

Note: The combination of CS HIGH, DI HIGH and the rising edge of the SK clock, resets the READY/BUSY flag. Therefore, it is important if you want to access the READY/BUSY flag, not to reset it through this combination of control signals.

Before a WRITE instruction can be executed, the device must be in the WRITE ENABLE (WEN) state.

Write All (WRALL)
The Write All (WRALL) instruction programs all registers with the data pattern specified in the instruction. While the WRALL instruction is being loaded, the address field becomes a sequence of DON'T-CARE bits. (Shown in Figure 7.)

As with the WRITE instruction, if CS is brought HIGH after a minimum wait of 250ns (tcs), the DO pin indicates the READY/BUSY status of the chip. (Shown in Figure 7.)

Erase (ERASE)
After the erase instruction is entered, CS must be brought LOW. The falling edge of CS initiates the self-timed internal programming cycle. Bringing CS HIGH after minimum of tcs, will cause DO to indicate the READ/BUSY status of the chip. To explain this, a logical "0" indicates the programming is still in progress while a logical "1" indicates the erase cycle is complete and the part is ready for another instruction. (Shown in Figure 8.)

Erase All (ERALL)
Full chip erase is provided for ease of programming. Erasing the entire chip involves setting all bits in the entire memory array to a logical "1". (Shown in Figure 9.)

Security Consideration
To protect the entire part against accidental modification of data, each programming instruction (WRITE, WRALL, ERASE, and ERALL) must satisfy two conditions before user initiate self-timed programming cycle (the falling edge of CS). One is that the AM93LC56 is at WEN status. The other is that the Vcc value must exceed a lock-out value which can be adjusted by ANALOG TECHNOLOGY INC.

■ Timing Diagram (1)

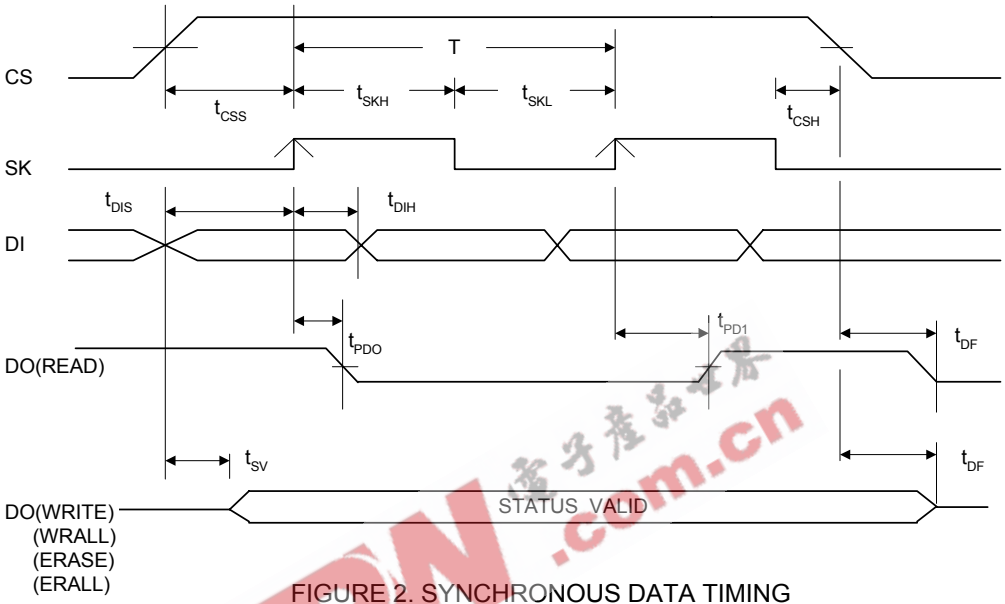
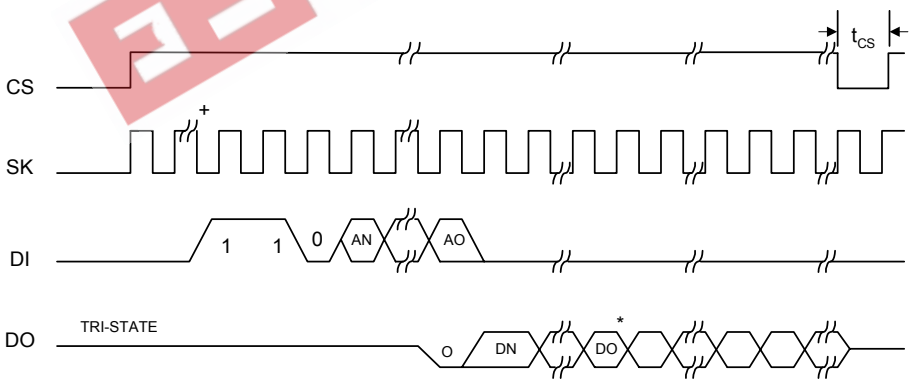


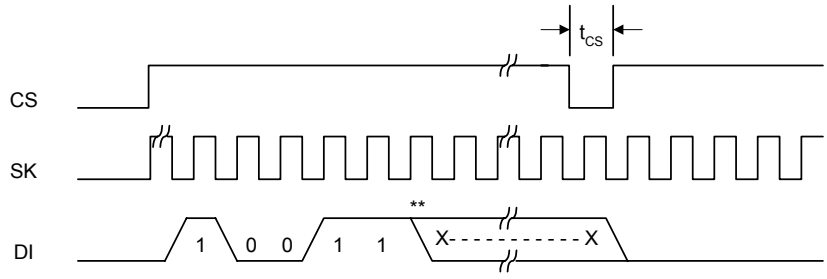
FIGURE 2. SYNCHRONOUS DATA TIMING



+For all instructions, SK cycles before start bit don't care.
*Address Pointer Cycle to the Next Register.

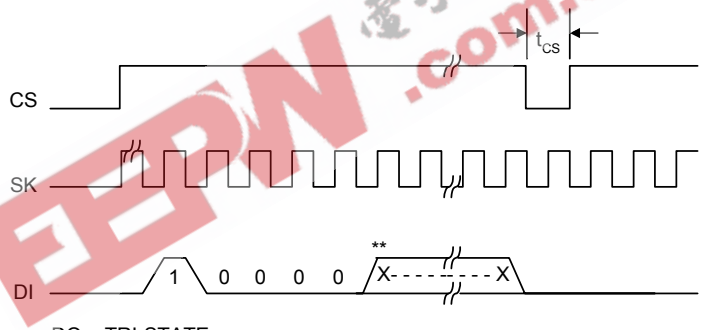
FIGURE 3. DATA READ CYCLE TIMING

■ Timing Diagram (2)



DO = TRI-STATE
**A_{N-2}~A0 don't care.

FIGURE 4. WRITE ENABLE(WEN) CYCLE TIMING



DO = TRI-STATE
**A_{N-2}~A0 don't care.

FIGURE 5. WRITE DISABLE(WDS) CYCLE TIMING

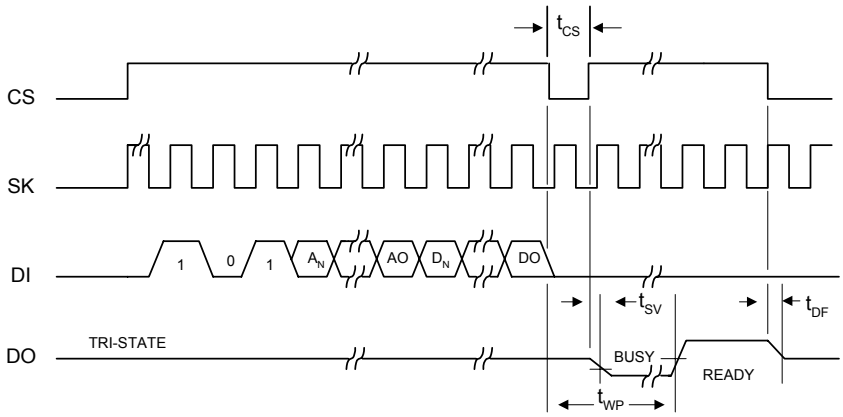


FIGURE 6. WRITE(WRITE) CYCLE TIMING

■ Timing Diagram (3)

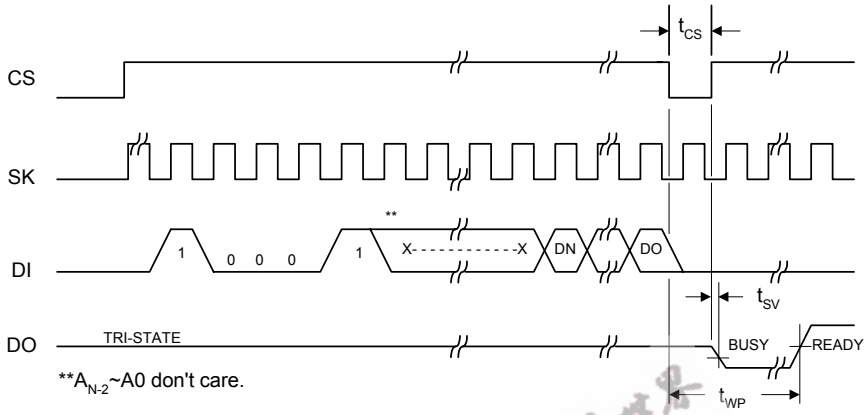


FIGURE 7. WRITE ALL(WRALL) CYCLE TIMING

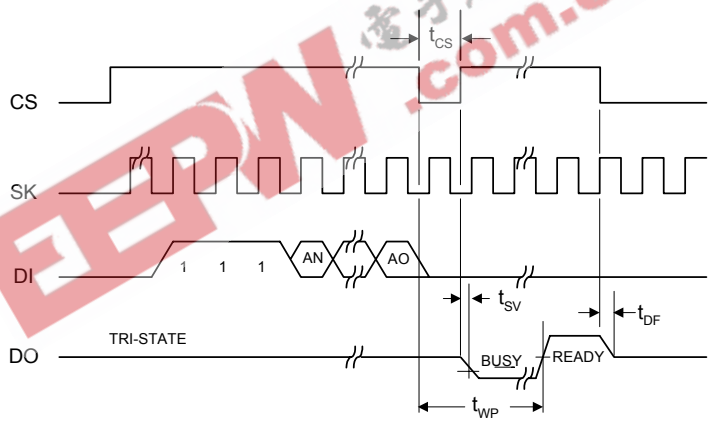


FIGURE 8. ERASE(ERASE) CYCLE TIMING

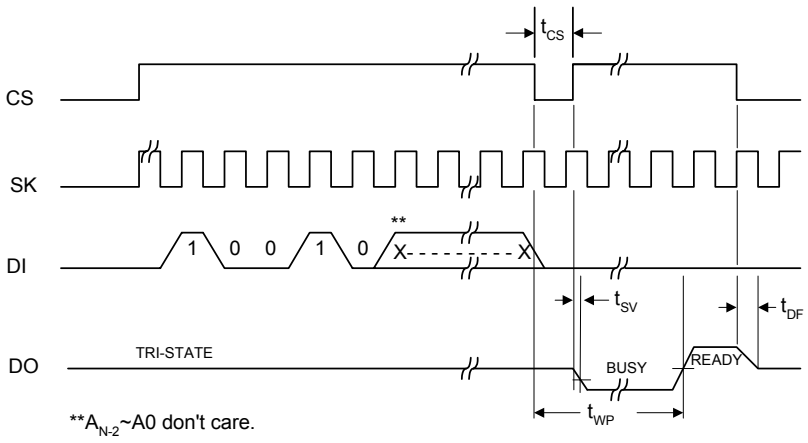
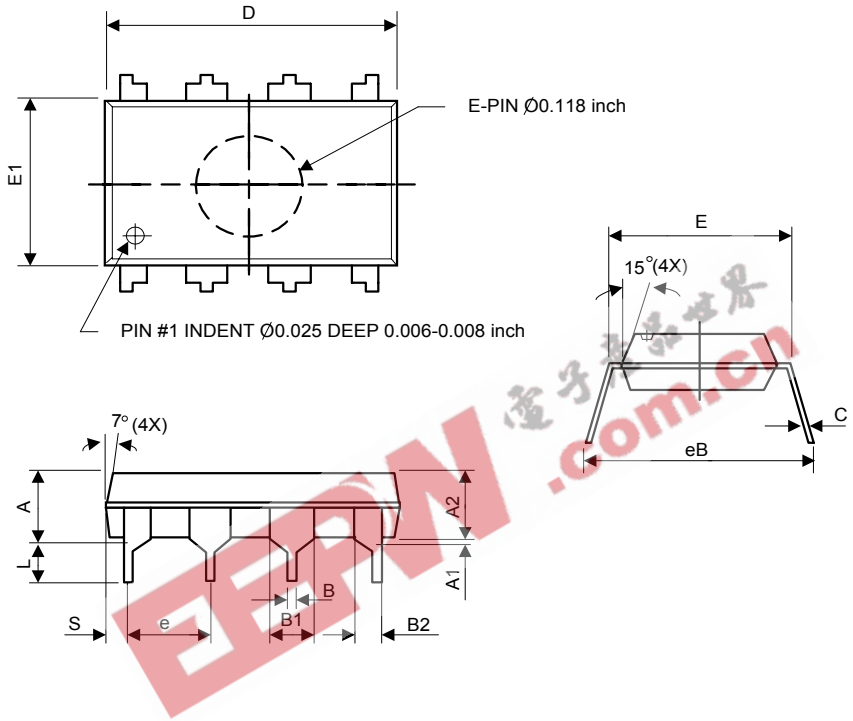


FIGURE 9. ERASE ALL(ERALL) CYCLE TIMING

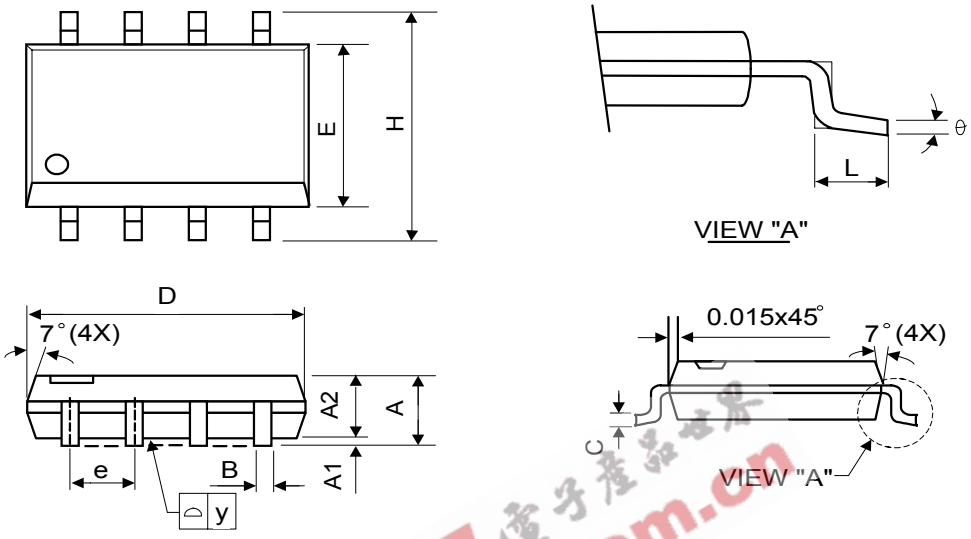
■ Package Diagrams

(1) Plastic Dual-in-line Package: PDIP-8L



Symbol	Dimensions in millimeters			Dimensions in inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	5.33	-	-	0.210
A1	0.38	-	-	0.015	-	-
A2	3.1	3.30	3.5	0.122	0.130	0.138
B	0.36	0.46	0.56	0.014	0.018	0.022
B1	1.4	1.52	1.65	0.055	0.060	0.065
B2	0.81	0.99	1.14	0.032	0.039	0.045
C	0.20	0.25	0.36	0.008	0.010	0.014
D	9.02	9.27	9.53	0.355	0.365	0.375
E	7.62	7.94	8.26	0.300	0.313	0.325
E1	6.15	6.35	6.55	0.242	0.250	0.258
e	-	2.54	-	-	0.100	-
L	2.92	3.3	3.81	0.115	0.130	0.150
eB	8.38	8.89	9.40	0.330	0.350	0.370
S	0.71	0.84	0.97	0.028	0.033	0.038

(2) JEDEC Small Outline Package: SOP-8L



Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	1.40	1.60	1.75	0.055	0.063	0.069
A1	0.10	-	0.25	0.040	-	0.100
A2	1.30	1.45	1.50	0.051	0.057	0.059
B	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.010
D	4.80	5.05	5.30	0.189	0.199	0.209
E	3.70	3.90	4.10	0.146	0.154	0.161
e	-	1.27	-	-	0.050	-
H	5.79	5.99	6.20	0.228	0.236	0.244
L	0.38	0.71	1.27	0.015	0.028	0.050
y	-	-	0.10	-	-	0.004
θ	0^{O}	-	8^{O}	0^{O}	-	8^{O}

■ Marking Information