AM93LC86

16384-bits Serial Electrically Erasable PROM (Preliminary)

■ Features

- State-of-the-art architecture
  - Non-volatile data storage
  - Standard voltage and low voltage operation
    Vcc: 2.7V ~ 5.5V
  - Full TTL compatible inputs and outputs
  - Auto increment read for efficient data dump
- Hardware and software write protection
  - Software instructions for write-enable/disable
  - VCC level verification before self-timed programming cycle
- Versatile, easy-to-use interface
  - Self-timed programming cycle
  - Automatic erase-before-write
  - Programming status indicator
  - Word and chip erasable
  - Stop SK anytime for power savings
- Durability and reliability
  - 40 years data retention
  - Minimum of 1M write cycles per word
  - Unlimited read cycles
  - ESD protection

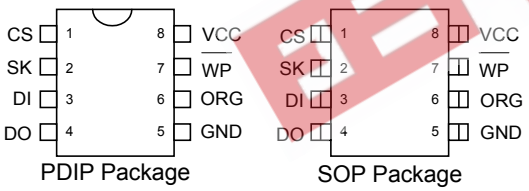
■ General Description

The AM93LC86 is the 16384-bit non-volatile serial EEPROM. The AM93LC86 provides efficient non-volatile read/write memory arranged as 1024 words of 16 bits each when the ORG Pin is connected to VCC and 2048 words of 8 bits each when it is tied to ground. The instruction set includes read, write, and write enable/disable functions. The data out pin (DO) indicates the status of the device during the self-timed non-volatile programming cycle.

The self-timed write cycle includes an automatic erase-before-write capability. Only when the chip is in the write enable state and proper Vcc operation range is the write instruction accepted and thus to protect against inadvertent writes. Data is written in 16 bits per write instruction into the selected register. If chip select (CS) is brought high after initiation of the write cycle, the data output (DO) pin will indicate the read/busy status of the chip.

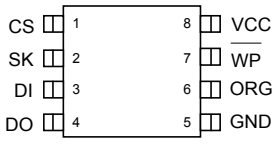
The AM93LC86 is available in space-saving 8-lead PDIP, SOP and TSSOP packages.

■ Pin Assignments



PDIP Package

SOP Package



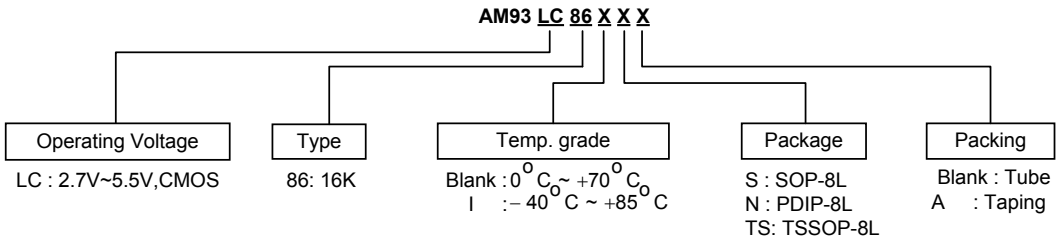
TSSOP Package

■ Pin Descriptions (note)

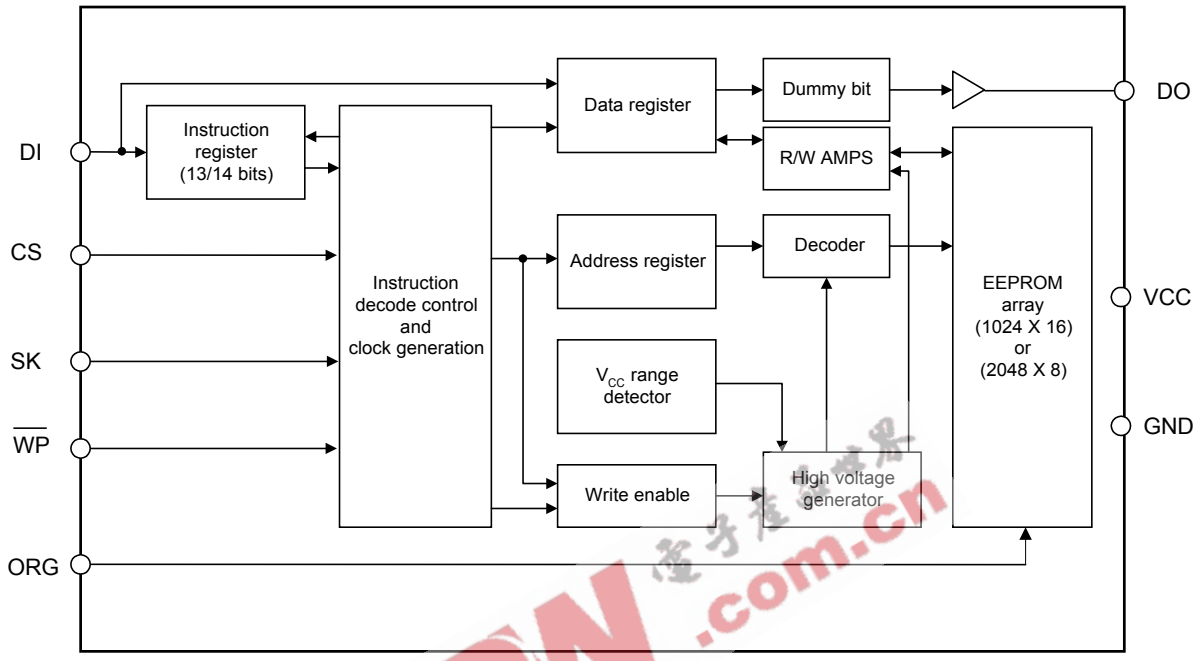
Name	Description
CS	Chip select
SK	Serial clock
DI	Data input
DO	Data output
GND	Ground
VCC	Power supply
$\overline{WP}$	Write protection (active low)
ORG	Organization

Note: See pin descriptions (continued) for more details

■ Ordering Information



■ Block Diagram



■ Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
T_{STG}	Storage temperature	-65 to +125	°C
V_{CC}	Voltage with respect to ground	-0.3 to + 6.5	V
T_{OP}	Temperature under bias	0 to + 70	°C

Note: These are stress rating only. Appropriate conditions for operating these devices given elsewhere may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

■ DC Electrical Characteristics (Vcc =2.7~5.5V, T_A = 25°C, unless otherwise noted)

Symbo	Parameter	Conditions	Min	Max	Unit
I_{CC}	Operating current**	CS=V_{IH}, SK=1MHz CMOS input levels		3	mA
I_{SB}	Standby current	CS=DI=SK=0V		10	µA
I_{IL}	Input leakage	V_{IN} = 0V to $V_{CC(CS,SK,DI)}$	-1	1	µA
I_{OL}	Output leakage	V_{OUT} = 0V to V_{CC}, CS=0V	-1	1	µA
V_{IL}	Input low voltage**	V_{CC} = 3V ± 10%	-0.1	0.15 V_{CC}	V
		V_{CC} = 5V ± 10%	-0.1	0.8	
V_{IH}	Input high voltage**	V_{CC} = 3V ± 10%	0.8 V_{CC}	V_{CC} +0.2	V
		V_{CC} = 5V ± 10%	2	V_{CC}+0.2	
V_{OL1}	Output low voltage	I_{OL} = 2.1mA TTL, V_{CC}=5V ± 10%		0.4	V
V_{OH1}	Output high voltage	I_{OH} = -400uA TTL, V_{CC}=5V ± 10%	2.4		V
V_{OL2}	Output low voltage	I_{OL} = 10uA CMOS		0.2	V
V_{OL2}	Output high voltage	I_{OH} = -10uA CMOS	V_{CC} -0.2		V

Note ** : I_{CC}, V_{IL} min and V_{IH} max are for reference only and are not tested.

■ AC Electrical Characteristics (Vcc = 2.7V ~ 5.5V, T_A = 25°C, unless otherwise noted)

Symbol	Parameter	Conditions	Min	Max	Unit
F_{SK}	SK Clock Frequency		0	1	Mhz
T_{SKH}	SK High Time		250		nS
T_{SKL}	SK Low Time		250		nS
T_{CS}	Minimum CS Low Time		250		nS
T_{CSS}	CS Setup Time	Relative to SK	50		nS
T_{DIS}	DI Setup Time	Relative to SK	100		nS
T_{CSH}	CS Hold Time	Relative to SK	0		nS
T_{DIH}	DI Hold Time	Relative to SK	100		nS
T_{PD1}	Output Delay to "1"	AC test (Fig. 1)		500	nS
T_{PD0}	Output Delay to "0"	AC test (Fig. 1)		500	nS
T_{SV}	CS to Status Valid	AC test CL = 100pF		500	nS
T_{DF}	CS to DO in 3-state	CS = VIL		100	nS
T_{WP}	Write Cycle Time			10	mS
Endurance(note)	5V, 25°C		1M		write cycles

Note: The parameter is characterized and isn't 100% tested.

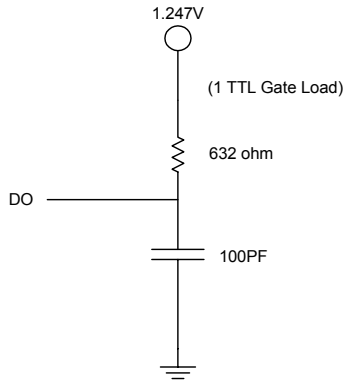


Figure 1. AC test circuit

■ Pin Capacitance (note) (T_A=25°C, F=1Mhz)

Symbol	Parameter	Max	Unit
C_{OUT}	Output capacitance	5	pF
C_{IN}	Input capacitance	5	pF

Note: The parameter is characterized and isn't 100% tested.

■ Instruction Set

Instruction (note)	Start bit	Op code	Address		Input data	
			X8	X16	× 8	× 16
READ	1	10	A_{10} ~ A_0	A_9 ~ A_0	-	-
EWEN	1	00	11XXXXXXXXX	11XXXXXXX	-	-
WRITE	1	01	A_{10} ~ A_0	A_9 ~ A_0	D_7 – D_0	D_{15} - D_0
WRAL	1	00	01XXXXXXXXX	01XXXXXXX	D_7 – D_0	D_{15} - D_0
EWDS	1	00	00XXXXXXXXX	00XXXXXXX	-	-
ERASE	1	11	A_{10} ~ A_0	A_9 ~ A_0	-	-
ERAL	1	00	10XXXXXXXXX	10XXXXXXX	-	-

Note:
READ: Read
EWEN: Erase/write enable
WRITE: Write
WRAL: Write all
EWDS: Erase/write disable
ERASE: Erase
ERAL: Erase all

■ Functional Description

Endurance and data retention
The AM93LC86 is designed for applications requiring up to 1M programming cycles (WRITE, WRAL, EARSE and ERAL). It provides 40 years of secure data retention.

Device operation
The AM93LC86 is controlled by seven 13-bit instructions. Instructions are clocked in (serially) on the DI pin. Each instruction begins with a logical "1" (the start bit). This is followed by the opcode (2 bits), the address field (10/11 bits), and data, if appropriated,. The clock signal (SK) may be halted at any time and the AM93LC86 will remain in its last state. This allows full static flexibility and maximum power conservation.

Auto increment read operations
Sequential read is possible, since the AM93LC86 has been designed to output a continuous stream of memory content in response to a single read operation instruction. To utilize this function, the system asserts a read instruction specifying a start location address. Once the 8-bit or 16-bit of the addressed word have been clocked out, the data in consecutively higher address locations is output. The address will wrap around continuously with CS high until the chip select (CS) control pin is brought low. This allows for single instruction data dumps to be executed with a minimum of firmware overhead.

Read (READ)
The READ instruction is the only instruction that outputs serial data on the DO pin. After the read instruction and address have been decoded, data is transferred from the selected memory register into a 8-bit or 16-bit serial shift register. (Please note that one logical "0" bit precedes the actual 8-bit or 16-bit output data string.) The output on DO changes during the rising edge transitions of SK. (shown in figure 3)

■ Functional Description

Erase/write enable (EWEN)
Before any device programming (WRITE, WRAL, ERASE, and ERAL) can be done, the EWEN instruction must be executed first. When Vcc is applied, this device powers up in the EWDS state. The device then remains in a erase/write disable (EWDS) state until a EWEN instruction is executed. Thereafter the device remains enabled until a EWDS instruction is executed or until Vcc is removed. (shown in Figure 4)
Note: Neither the EWEN nor the EWDS instruction has any effect on the READ instruction.

Erase/write disable (EWDS)
The erase/write disable (EWDS) instruction disables all programming capabilities. This protects the entire part against accidental modification of data until a EWEN instruction is executed. (When Vcc is applied, this part powers up in the EWDS state.) To protect data, a EWDS instruction should be executed upon completion of each programming operation.
Note:
Neither the EWEN nor the EWDS instruction has any effect on the READ instruction. (shown in figure 5)

Write (WRITE)
The WRITE instruction includes 8-bit or 16-bit of data to be written into the specified register. After the last data bit has been applied to DI, and before the next rising edge of SK, CS must be brought low. The falling edge of CS initiates the self-timed programming cycle. After a minimum wait of 250ns (5V operation) from the falling edge of CS (tcs), DO will indicate the READY/BUSY status of the chip if CS is brought HIGH. This means that logical "0" implies the programming is still in progress while logical "1" indicates the selected register has been written, and the part is ready for another instruction. (shown in figure 6)
Note:
The combination of CS HIGH, DI HIGH and the rising edge of the SK clock, resets the READY/BUSY flag. Therefore, it is important if you want to access the READY/BUSY flag, not to reset it through this combination of control signals.

Before a WRITE instruction can be executed, the device must be in the Write enable (WEN) state.

Write all (WRAL)
The Write All (WRAL) instruction programs all registers with the data pattern specified in the instruction. While the WRAL instruction is being loaded, the address field becomes a sequence of DON'T-CARE bits. (Shown in Figure 7)
As with the WRITE instruction, if CS is brought HIGH after a minimum wait of 250ns (tcs), the DO pin indicates the READY/BUSY status of the chip. (shown in figure 7)

Erase (ERASE)
After the erase instruction is entered, CS must be brought LOW. The falling edge of CS initiates the self-timed internal programming cycle. Bringing CS HIGH after minimum of tcs, will cause DO to indicate the READ/BUSY status of the chip. To explain this, a logical "0" indicates the programming is still in progress while a logical "1" indicates the erase cycle is complete and the part is ready for another instruction. (shown in figure 8)

Erase all (ERAL)
Full chip erase is provided for ease of programming. Erasing the entire chip involves setting all bits in the entire memory array to a logical "1". (shown in figure 9)

■ Timing Diagrams

Organization Key

I/O	AM93LC86 (16K)	
	X8	X16
A_N	A_{10}	A_9
D_N	D_7	D_{15}

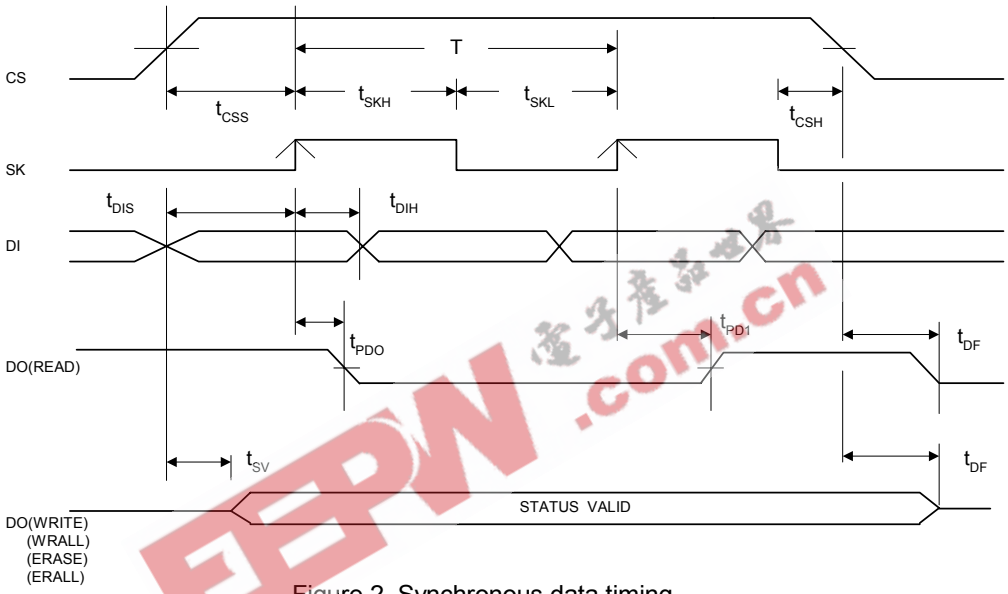
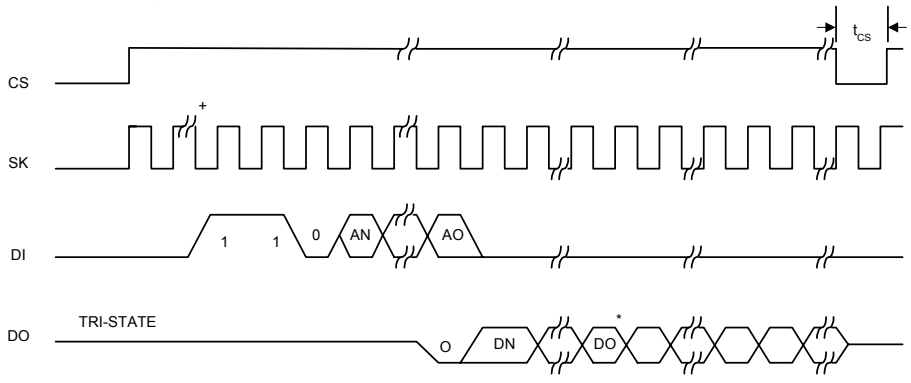
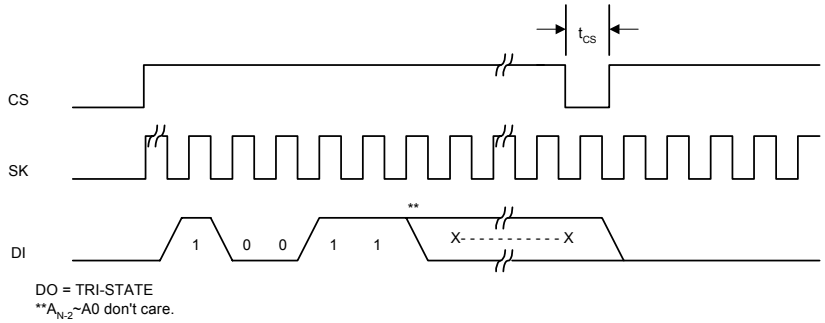


Figure 2. Synchronous data timing



+For all instructions, SK cycles before start bit don't care.
*Address Pointer Cycle to the Next Register.

Figure 3. Data read cycle timing



FIigure 4. Erase/write enable(WEN) cycle timing

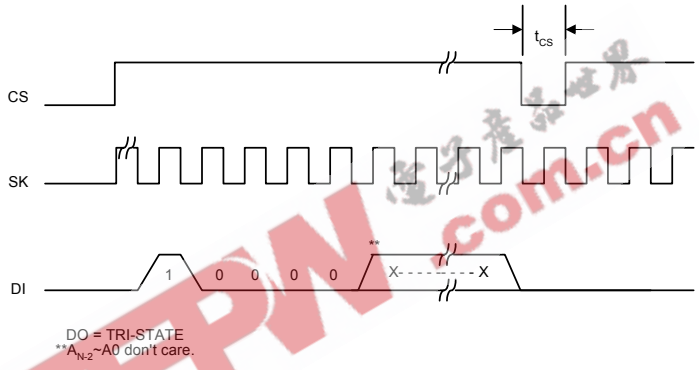


Figure 5. Erase/write disable(EWDS) cycle timing

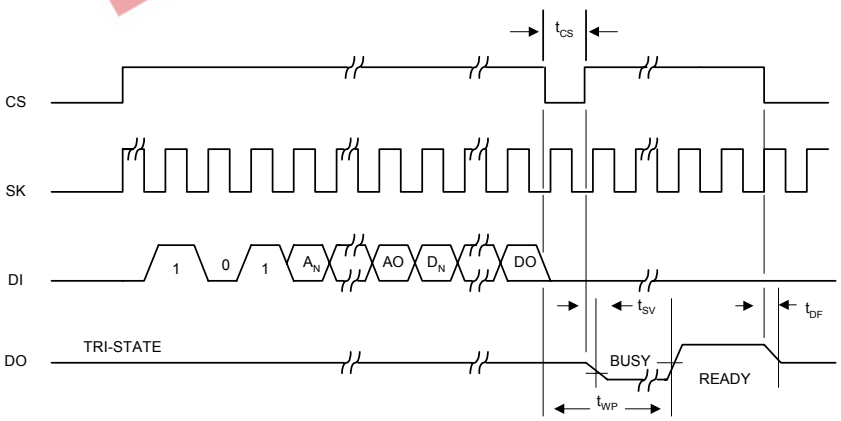


Figure 6. Write(WRITE) cycle timing

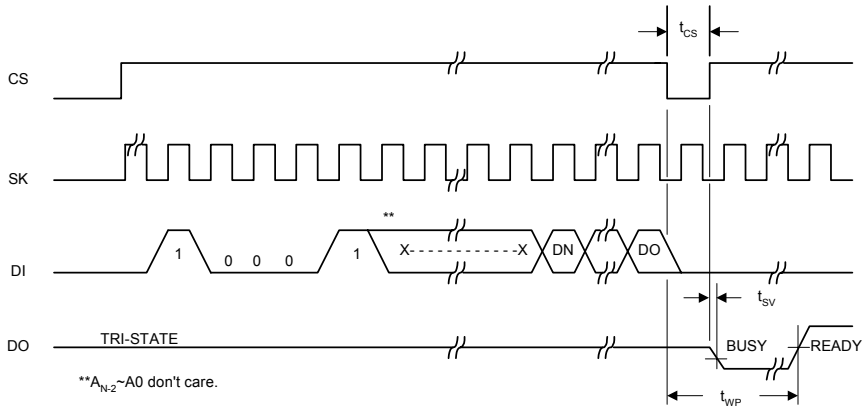


Figure 7. Write all(WRAL) cycle timing

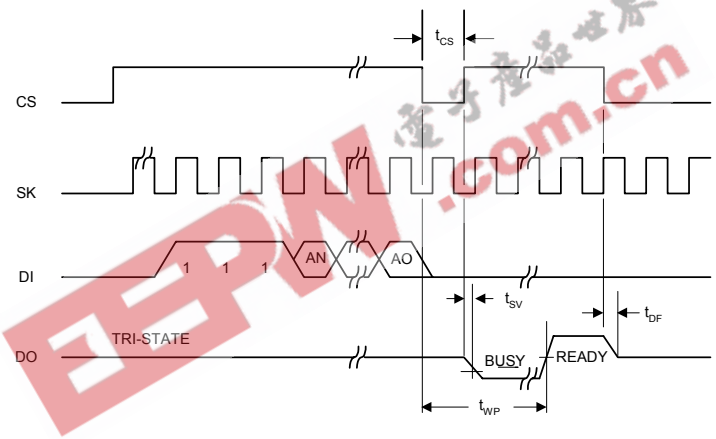


Figure 8. Erase(ERASE) cycle timing

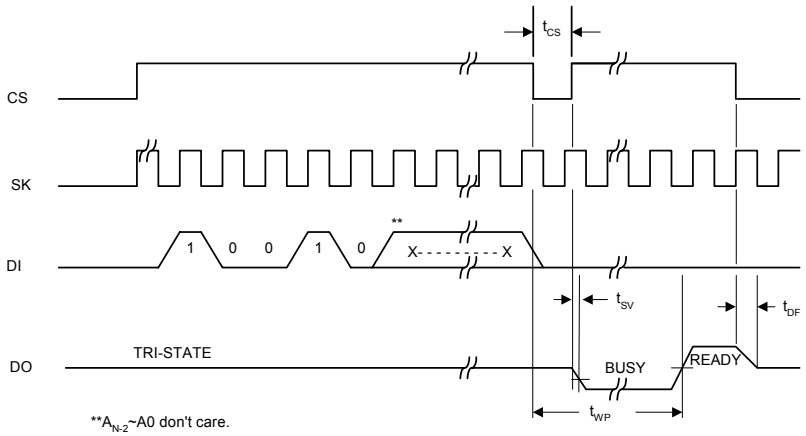


Figure 9. Erase all(ERAL) cycle timing

■ Pin Description (Continued)

Chip select (CS)
A high level selects the device. A low level deselects the device an forces it into standby mode. However, a programming cycle which is already initiated will be completed, regardless of the CS input signal. If CS is brought low during a program cycle, the device will go into standby mode as soon as the programming cycle is completed.

Serial clock (SK)
The serial clock is used to synchronize the communication between a master device and the AM93LC86. Opcode, address, and data bits are clocked in on the positive edge of SK. Data bits are also clocked out on the positive edge of SK.
SK can be stopped anywhere in the transmission sequence (at high or low level) and can be continued anytime with respect to clock high time (T_{CKH}) and clock low time (T_{CKL}). This gives the controlling master freedom in preparing opcode, address, and data.
SK is a "don't care" if CS is low (device deselected). If CS is high, but START condition has not been detected, any number of clock cycles can be received by the device without changing its status (i.e., waiting for START condition).
SK cycles are not required during the self-timed WRITE (i.e., auto ERASE/WRITE) cycles.
After detection of a start condition the specified number of clock cycles (respectively low to high transitions of SK) must be provided. These clock cycles are required to clock in all opcode, address, and data bits before an instruction is executed (see the table of instruction set). SK and DI then become don't care inputs waiting for a new start condition to be detected.
Note:
CS must go low between consecutive instructions, except when performing a sequential read.

Data input (DI)
Data input is used to clock in a start bit, opcode, address, and data synchronously with the CLK input.

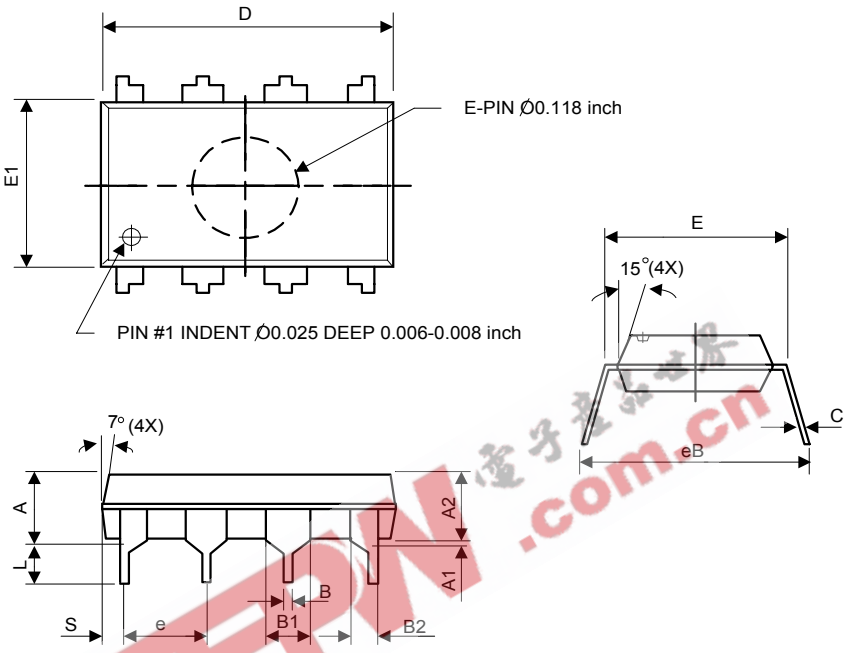
Data output (DO)
Data output is used in the READ mode to output data synchronously with the CLK input(T_{PD} after the positive edge of CLK)

Write protection ($\overline{WP}$)
This pin allows the user to enable or disable the ability to write data to the memory array. If the $\overline{WP}$ pin is floated or tied to VCC, the device can be programmed. If the $\overline{WP}$ pin is tied to GND, programming will be inhibited. There is an internal pull-up on this device that enables programming if this pin is left floating.

Organization (ORG)
When ORG is connected to VCC, the X16 memory organization is selected. When ORG is tied to GND, the X8 memory organization is selected. There is an internal pull-up resistor on the ORG pin that will select X16 organization when left unconnected.

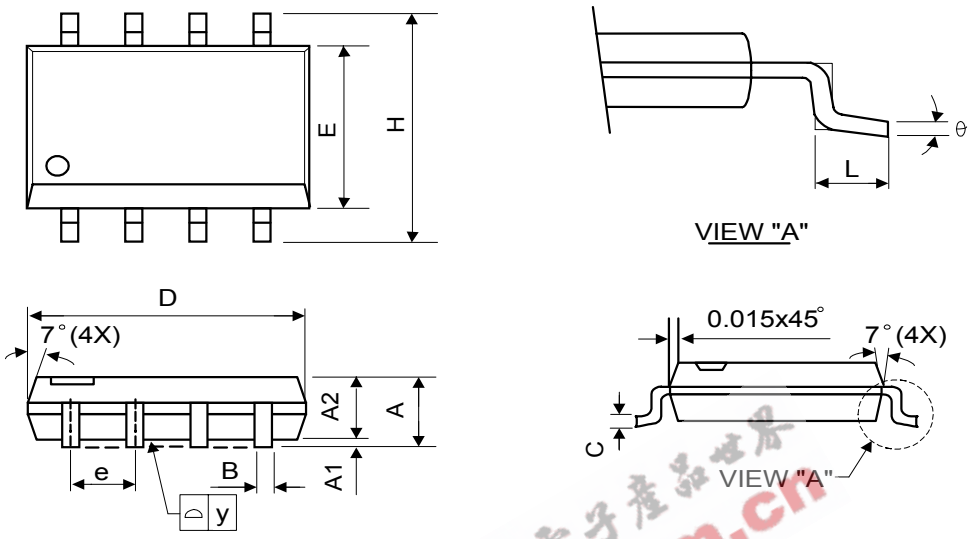
■ Package Information

(1) Package Type: PDIP-8L



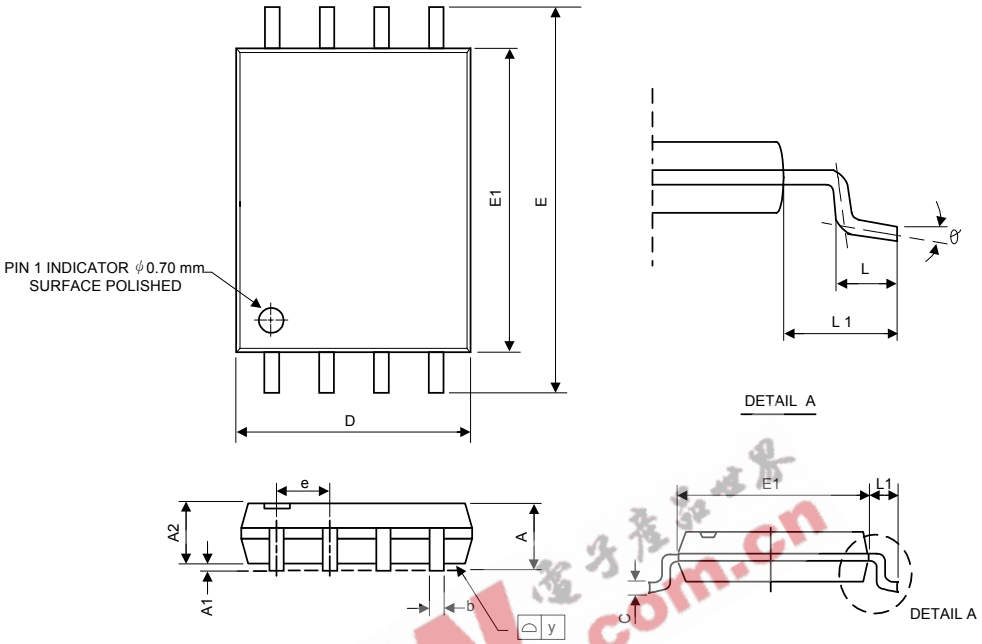
Symbol	Dimensions in millimeters			Dimensions in inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	5.33	-	-	0.210
A1	0.38	-	-	0.015	-	-
A2	3.1	3.30	3.5	0.122	0.130	0.138
B	0.36	0.46	0.56	0.014	0.018	0.022
B1	1.4	1.52	1.65	0.055	0.060	0.065
B2	0.81	0.99	1.14	0.032	0.039	0.045
C	0.20	0.25	0.36	0.008	0.010	0.014
D	9.02	9.27	9.53	0.355	0.365	0.375
E	7.62	7.94	8.26	0.300	0.313	0.325
E1	6.15	6.35	6.55	0.242	0.250	0.258
e	-	2.54	-	-	0.100	-
L	2.92	3.3	3.81	0.115	0.130	0.150
eB	8.38	8.89	9.40	0.330	0.350	0.370
S	0.71	0.84	0.97	0.028	0.033	0.038

(2) Package Type: SOP-8L



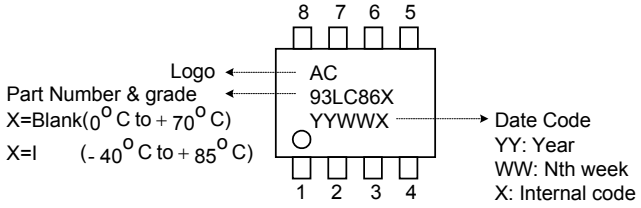
Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	1.40	1.60	1.75	0.055	0.063	0.069
A1	0.10	-	0.25	0.040	-	0.100
A2	1.30	1.45	1.50	0.051	0.057	0.059
B	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.010
D	4.80	5.05	5.30	0.189	0.199	0.209
E	3.70	3.90	4.10	0.146	0.154	0.161
e	-	1.27	-	-	0.050	-
H	5.79	5.99	6.20	0.228	0.236	0.244
L	0.38	0.71	1.27	0.015	0.028	0.050
y	-	-	0.10	-	-	0.004
θ	0^O	-	8^O	0^O	-	8^O

(3) Package Type: TSSOP-8L



Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	1.05	1.10	1.20	0.041	0.043	0.047
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	-	1.00	1.05	-	0.039	0.041
b	0.20	0.25	0.28	0.008	0.01	0.011
C	-	0.13	-	-	0.005	-
D	2.90	3.05	3.10	0.114	0.12	0.122
E	6.20	6.40	6.60	0.244	0.252	0.26
E1	4.30	4.40	4.50	0.169	0.173	0.177
e	-	0.65	-	-	0.026	-
L	0.50	0.60	0.70	0.02	0.024	0.028
L1	0.90	1.00	1.10	0.035	0.039	0.043
y	-	-	0.10	-	-	0.004
θ	0^O	4^O	8^O	0^O	4^O	8^O

■ Marking Information



PDIP/SOP/TSSOP Package