PRELIMINARY

AMD

Am79C984A

enhanced Integrated Multiport Repeater (eIMR™)

DISTINCTIVE CHARACTERISTICS

- **Repeater functions comply with IEEE 802.3 Repeater Unit specifications**
- **Four integral 10BASE-T transceivers with on-chip filtering that eliminate the need for external filter modules on the 10BASE-T transmit-data (TXD) and receive-data (RXD) lines**
- **One Reversible Attachment Unit Interface (RAUI™) port that can be used either as a standard IEEE-compliant AUI port for connection to a Medium Attachment Unit (MAU), or as a reversed port for direct connection to a Media Access Controller (MAC)**
- **Low cost suitable for non-managed multiport repeater designs**
- **Expandable to increase number of repeater ports with support for up to seven eIMR devices without the need for an external arbiter**
- **All ports can be individually isolated (partitioned) in response to excessive collision conditions or fault conditions.**
- **Full LED support for individual port status LEDs and network utilization LEDs**
- **Programmable extended distance mode on the RXD lines, allowing connection to cables longer than 100 meters**
- **Twisted Pair Link Test capability conforming to the 10BASE-T standard. The Link Test function and the transmission of Link Test pulses can be optionally disabled through the control port to allow devices that do not implement the Link Test function to work with the eIMR device.**
- **Programmable option of automatic polarity detection and correction permits automatic recovery due to wiring errors**
- **Full amplitude and timing regeneration for retransmitted waveforms**
- **CMOS device with a single +5-V supply**

GENERAL DESCRIPTION

The enhanced Integrated Multiport Repeater (eIMR) device is a VLSI integrated circuit that provides a system-level solution to designing non-managed multiport repeaters. The device integrates the repeater functions specified in Section 9 of the IEEE 802.3 standard and Twisted Pair Transceiver functions complying with the 10BASE-T standard.

The eIMR device provides four Twisted Pair (TP) ports and one RAUI port for direct connection to a MAC. The total number of ports per repeater unit can be increased by connecting multiple eIMR devices through their expansion ports, hence, minimizing the total cost per repeater port.

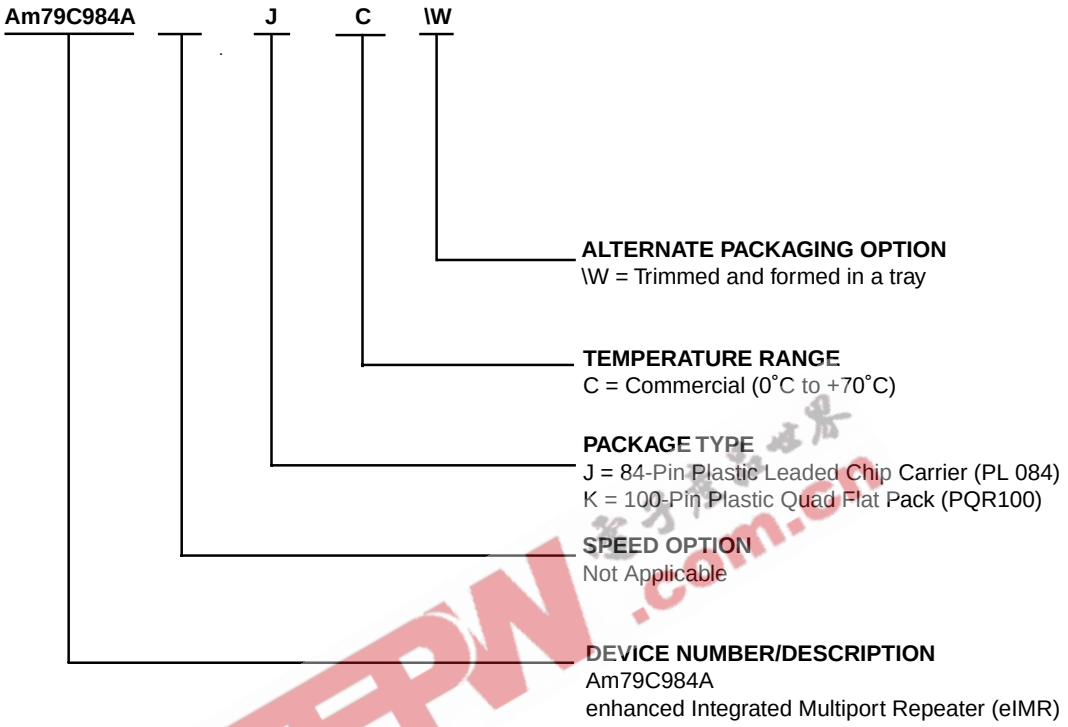
The device is fabricated in CMOS technology and requires a single +5-V supply.

Publication# **20650** Rev: **B** Amendment/**0**
Issue Date: **January 1998**

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.

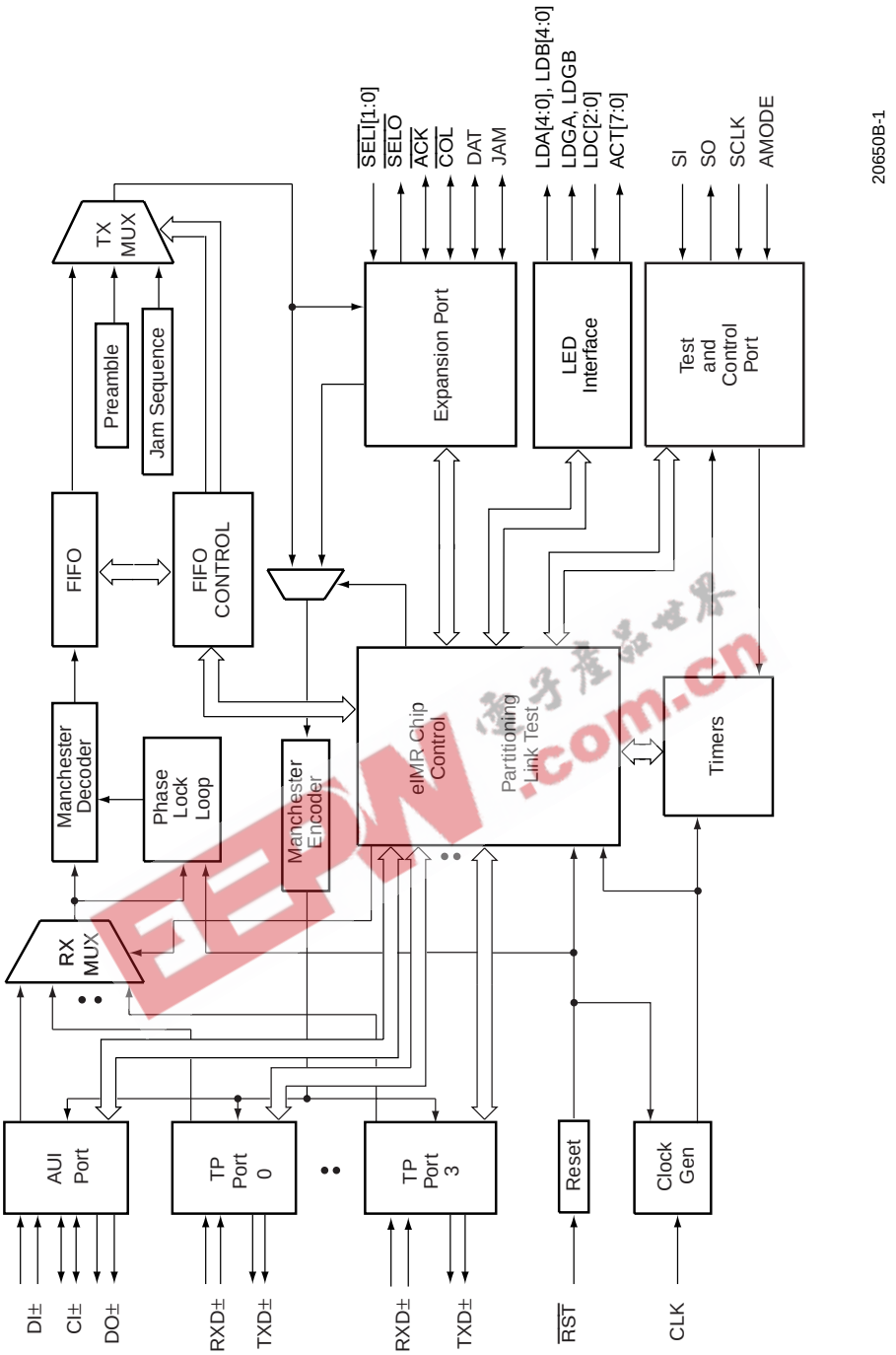


Valid Combinations	
Am79C984A	JC, KC\W

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

BLOCK DIAGRAM



RELATED AMD PRODUCTS

Part No.	Description
Am7990	Local Area Network Controller for Ethernet (LANCE)
Am7992B	Serial Interface Adapter (SIA)
Am7996	IEEE 802.3/Ethernet/Cheapernet Transceiver
Am79C90	CMOS Local Area Network Controller for Ethernet (C-LANCE)
Am79C98	Twisted Pair Ethernet Transceiver (TPEX)
Am79C100	Twisted Pair Ethernet Transceiver Plus (TPEX+)
Am79C981	Integrated Multiport Repeater Plus (IMR+™)
Am79C982	basic Integrated Multiport Repeater (bIMR™)
Am79C987	Hardware Implemented Management Information Base (HIMIB™)
Am79C988	Quad Integrated Ethernet Transceiver (QuIET™)
Am79C900	Integrated Local Area Communications Controller (ILACC™)
Am79C940	Media Access Controller for Ethernet (MACE™)
Am79C960	PCnet™-ISA Single-Chip Ethernet Controller (for ISA bus)
Am79C961	PCnet™-ISA+ Single-Chip Ethernet Controller for ISA (with Microsoft® Plug n' Play® Support)
Am79C961A	PCnet™-ISA II Full Duplex Single-Chip Ethernet Controller for ISA
Am79C965	PCnet™-32 Single-Chip 32-Bit Ethernet Controller
Am79C970	PCnet™-PCI Single-Chip Ethernet Controller (for PCI bus)
Am79C970A	PCnet™-PCI II Full Duplex Single-Chip Ethernet Controller (for PCI bus)
Am79C974	PCnet™-SCSI Combination Ethernet and SCSI Controller for PCI Systems
Am79C983	Integrated Multiport Repeater 2 (IMR2™)
Am79C985	enhanced Integrated Multiport Repeater Plus (eIMR+™)

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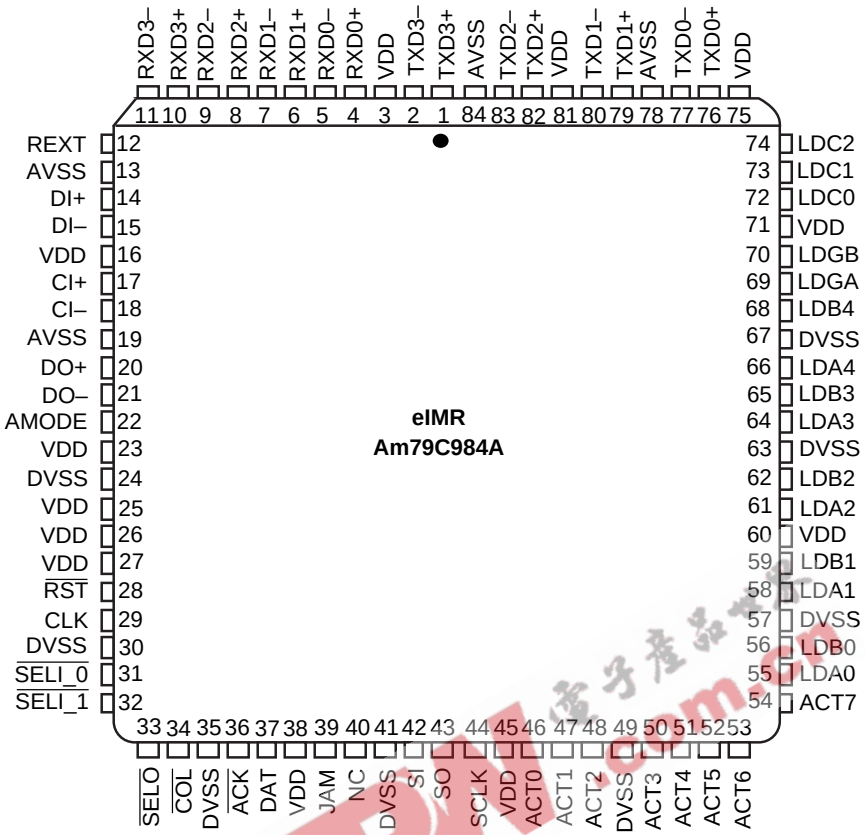

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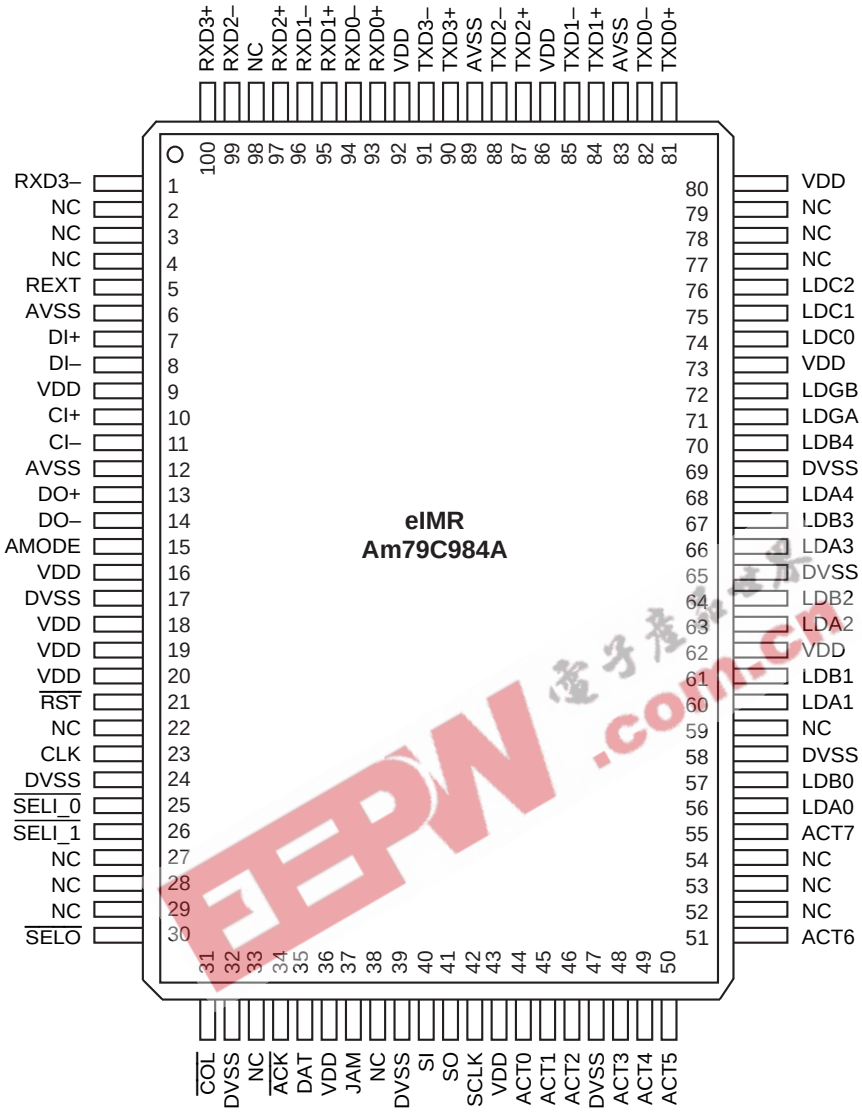
CONNECTION DIAGRAM (PQR100)



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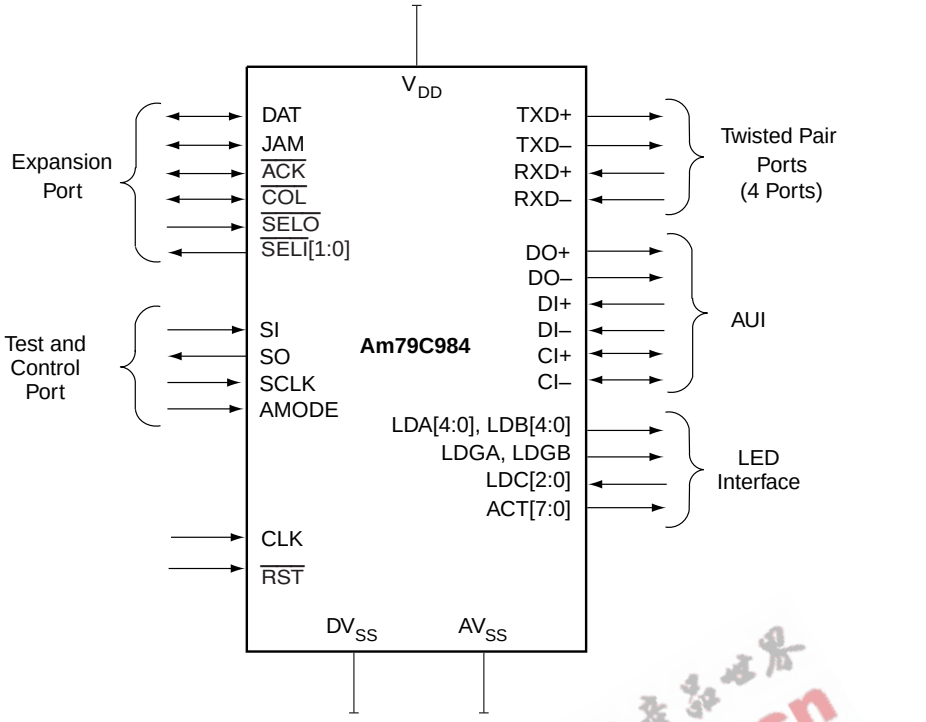

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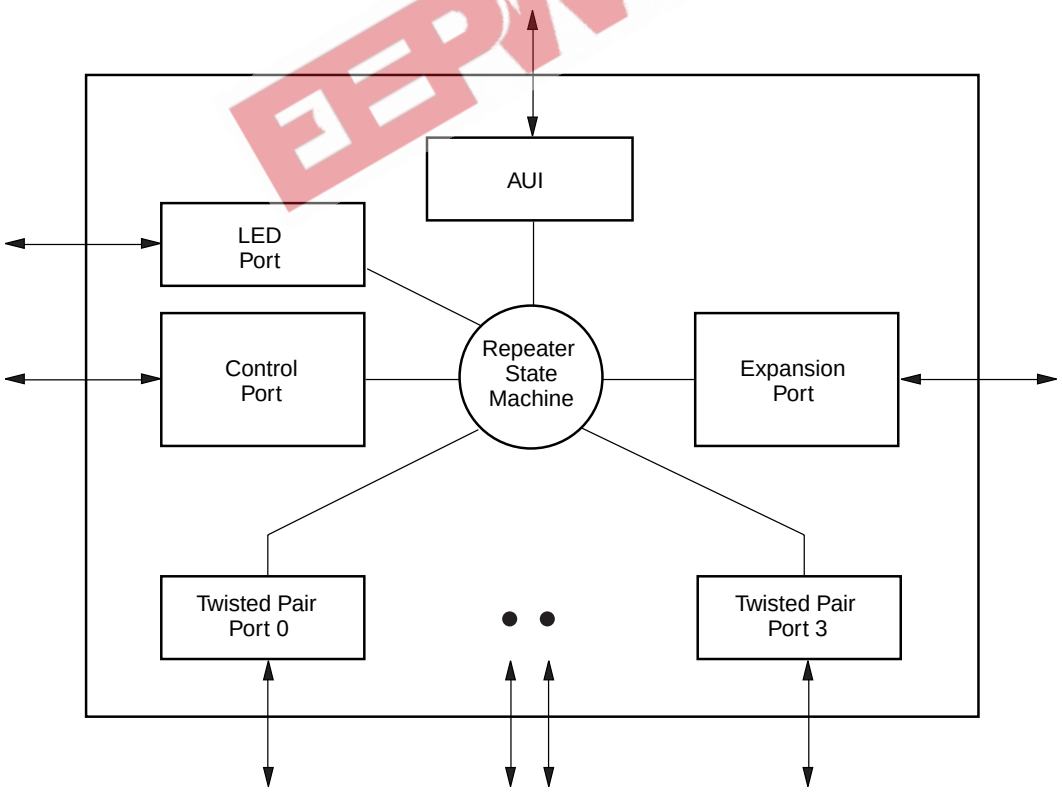
LOGIC DIAGRAM



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PIN DESIGNATIONS (PL 084)

Listed by Pin Number

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	TXD3+	22	AMODE	43	SO	64	LDA3
2	TXD3-	23	VDD	44	SCLK	65	LDB3
3	VDD	24	DVSS	45	VDD	66	LDA4
4	RXD0+	25	VDD	46	ACT0	67	DVSS
5	RXD0-	26	VDD	47	ACT1	68	LDB4
6	RXD1+	27	VDD	48	ACT2	69	LDGA
7	RXD1-	28	$\overline{\text{RST}}$	49	DVSS	70	LDGB
8	RXD2+	29	CLK	50	ACT3	71	VDD
9	RXD2-	30	DVSS	51	ACT4	72	LDC0
10	RXD3+	31	$\overline{\text{SELI\_0}}$	52	ACT5	73	LDC1
11	RXD3-	32	$\overline{\text{SELI\_1}}$	53	ACT6	74	LDC2
12	REXT	33	$\overline{\text{SELO}}$	54	ACT7	75	VDD
13	AVSS	34	$\overline{\text{COL}}$	55	LDA0	76	TXD0+
14	DI+	35	DVSS	56	LDB0	77	TXD0-
15	DI-	36	$\overline{\text{ACK}}$	57	DVSS	78	AVSS
16	VDD	37	DAT	58	LDA1	79	TXD1+
17	CI+	38	VDD	59	LDB1	80	TXD1-
18	CI-	39	JAM	60	VDD	81	VDD
19	AVSS	40	NC	61	LDA2	82	TXD2+
20	DO+	41	DVSS	62	LDB2	83	TXD2-
21	DO-	42	SI	63	DVSS	84	AVSS

PIN DESIGNATIONS (PQR100)

Listed by Pin Number

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	RXD3-	26	$\overline{\text{SELI\_1}}$	51	ACT6	76	LDC2
2	NC	27	NC	52	NC	77	NC
3	NC	28	NC	53	NC	78	NC
4	NC	29	NC	54	NC	79	NC
5	REXT	30	$\overline{\text{SELO}}$	55	ACT7	80	VDD
6	AVSS	31	$\overline{\text{COL}}$	56	LDA0	81	TXD0+
7	DI+	32	DVSS	57	LDB0	82	TXD0-
8	DI-	33	NC	58	DVSS	83	AVSS
9	VDD	34	$\overline{\text{ACK}}$	59	NC	84	TXD1+
10	CI+	35	DAT	60	LDA1	85	TXD1-
11	CI-	36	VDD	61	LDB1	86	VDD
12	AVSS	37	JAM	62	VDD	87	TXD2+
13	DO+	38	NC	63	LDA2	88	TXD2-
14	DO-	39	DVSS	64	LDB2	89	AVSS
15	AMODE	40	SI	65	DVSS	90	TXD3+
16	VDD	41	SO	66	LDA3	91	TXD3-
17	DVSS	42	SCLK	67	LDB3	92	VDD
18	VDD	43	VDD	68	LDA4	93	RXD0+
19	VDD	44	ACT0	69	DVSS	94	RXD0-
20	VDD	45	ACT1	70	LDB4	95	RXD1+
21	$\overline{\text{RST}}$	46	ACT2	71	LDGA	96	RXD1-
22	NC	47	DVSS	72	LDGB	97	RXD2+
23	CLK	48	ACT3	73	VDD	98	NC
24	DVSS	49	ACT4	74	LDC0	99	RXD2-
25	$\overline{\text{SELI\_0}}$	50	ACT5	75	LDC1	100	RXD3+

Notes:

1. *Pin 40 has a bonding option depending on internal device name.*
2. *NC = No Connection.*

PIN DESCRIPTION

AUI Port

DI+, DI–
Data In
Differential Input

DI± are differential, Manchester receiver pins. The signals comply with IEEE 802.3, Section 7.

DO+, DO–
Data Out
Differential Output

DO± are differential, Manchester output driver pins. The signals comply with IEEE 802.3, Section 7.

CI+, CI–
Collision Input
Differential Input/Output

CI± are differential, Manchester I/O signals. As an input, CI is a collision-receive indicator. As an output, CI generates a 10-MHz signal if the eIMR device senses a collision.

Twisted Pair Ports

$TXD+_{0-3}$, $TXD-_{0-3}$
Transmit Data
Differential Output

TXD± are 10BASE-T port differential drivers (4 ports).

$RXD+_{0-3}$, $RXD-_{0-3}$
Receive Data
Differential Input

RXD± are 10BASE-T port differential receive inputs (4 ports).

Expansion Bus

DAT
Data
Input/Output/3-State

If the $\overline{SELO}$ and $\overline{ACK}$ pins are asserted during non-collision conditions, the eIMR device drives NRZ data onto the DAT line, regenerating the preamble if necessary. During a collision, when JAM is HIGH, DAT is used to differentiate between single-port (DAT=1) and multiport (DAT=0) collisions. DAT is an output when $\overline{ACK}$ is asserted and the eIMR device's ports are active; DAT is an input when $\overline{ACK}$ is asserted and the ports are inactive. If $\overline{ACK}$ is not asserted, DAT is in the high-impedance state. It is recommended that DAT be pulled up or down via a high value resistor.

JAM
Jam
Input/Output/3-State

The active eIMR device drives JAM HIGH, if it detects a collision condition on one or more of its ports. The state of the DAT pin is used in conjunction with JAM to indicate a single port (DAT =1) or multiport (DAT=0) collision. JAM is in the high-impedance state if neither the $\overline{SEL}$ nor $\overline{ACK}$ signal is asserted. It is recommended that JAM be pulled up or down via a high value resistor.

$\overline{SELI}_{0-1}$
Select In
Input, Active LOW

When the expansion bus is configured for Internal Arbitration mode, these signals indicate that another eIMR device is active; $\overline{SELI}_0$ or $\overline{SELI}_1$ is driven by $\overline{SELO}$ from the upstream device. At reset, $\overline{SELI}_0$ selects between the Internal Arbitration mode and the IMR+ mode of the expansion bus; a HIGH selects the Internal Arbitration mode and a LOW selects the IMR+ mode.

$\overline{SELI\_1}$	$\overline{SELI\_0}$	Arbitration Mode
X	1	Internal
X	0	IMR+

$\overline{SELO}$
Select Out
Output, Active LOW

If the expansion bus is configured for Internal Arbitration mode, an eIMR device drives this pin LOW when it is active or when either of its $\overline{SELI}_{0-1}$ pins is LOW. An active eIMR device is defined as having one or more ports receiving or colliding and/or is still transmitting data from the internal FIFO, or extending a packet to the minimum of 96 bit times. When the expansion bus is configured for IMR+ mode, $\overline{SELO}$ is active when the eIMR device is active (acquiring the functionality of the $\overline{REQ}$ pin on the Am79C971 IMR+ device).

$\overline{ACK}$
Acknowledge
Input/Output, Active LOW, Open Drain

This signal is asserted to indicate that an eIMR device is active. It also signals to the other eIMR devices the presence of a valid collision status on the JAM line and valid data on the DAT line. When the eIMR device is configured for Internal Arbitration mode, $\overline{ACK}$ is an I/O, and must be pulled to VDD via a minimum equivalent resistance of 1 kΩ. When the eIMR device is configured for IMR+ mode, $\overline{ACK}$ is an input driven by an external arbiter.

$\overline{COL}$
Collision
Input/Output, Active LOW, Open Drain

When asserted, $\overline{COL}$ indicates that more than one eIMR device is active. Each eIMR device generates the Collision Jam sequence independently. When the eIMR device is configured for Internal Arbitration mode, $\overline{COL}$ is

an I/O and must be pulled to VDD via a minimum equivalent resistance of 1 kΩ. When the eIMR device expansion port is configured for IMR+ mode, $\overline{COL}$ is an input driven by an external arbiter.

Control Port

AMODE
AUI Mode
Input
At reset, this pin sets the AUI port to either normal or reversed mode. If AMODE is LOW at the rising edge of $\overline{RST}$, the AUI port is set to the normal mode; if AMODE is HIGH, the AUI port is set to the reversed mode.

SCLK
Serial Clock In
Input
Serial data (input or output) is clocked (in or out) on the rising edge of the signal on this pin. SCLK is asynchronous to CLK and can operate at frequencies up to 10 MHz.

SI
Serial In
Input
The SI pin is used as a test/control serial input port. Control commands are clocked in on this pin synchronous to SCLK input.

At reset, SI sets the state of the Automatic Polarity Reversal function. If SI is HIGH at the rising edge of $\overline{RST}$, Automatic Polarity Reversal is disabled. If SI is LOW at the rising edge of $\overline{RST}$, Automatic Polarity Reversal is enabled.

SO
Serial Out
Output
The SO pin is used as a control command serial output port. Responses to control commands are clocked out on this pin synchronous to the SCLK input.

LED Interface

LDA_{0-4}, LDB_{0-4}
LED Drivers
Output, Open Drain
LDA_{0-4} and LDB_{0-4} drive LED Bank A and LED Bank B, respectively. LDA_0 and LDB_0 indicate the status of the AUI port; LDA_{1-4} and LDB_{1-4} indicate the status of the four TP ports. The port attributes monitored by LDA_{0-4} and LDB_{0-4} are programmed by three pins, LDC_{0-2}.

LDGA
Global LED Driver, Bank A
Output, Open Drain
LDGA is the Global LED driver for LED Bank A. The signal represents global CRS or COL conditions. In a multiple-eIMR configuration, LDGA from each of the eIMR devices can be tied together to drive a single global LED in Bank A.

LDGB
Global LED Driver, Bank B
Output, Open Drain
LDGB is the Global LED driver for LED Bank B. The signal represents global CRS or JAB conditions. In a multiple eIMR configuration, LDGB from each of the eIMR devices can be tied together to drive a single global LED in Bank B.

LDC_{0-2}
LED Control
Input
These pins select the attributes that will be displayed on LDA_{0-4}, LDB_{0-4}, LDGA, and LDGB. If an LED is programmed to display two attributes, the attribute associated with the periodic blink takes precedence.

ACT_{0-7}
Activity Display
Output
These signals drive the activity LEDs, which indicate the percentage of network utilization. The display is updated every 250 ms.

Miscellaneous Pins

$\overline{RST}$
Reset
Input, Active LOW
When $\overline{RST}$ is LOW, the eIMR device resets to its default state. On the rising (trailing) edge of $\overline{RST}$, the eIMR also monitors the state of the $\overline{SELI}_{0-1}$, SI, and AMODE pins, to configure the operating mode of the device. In multiple eIMR systems, the falling (leading) edge of the $\overline{RST}$ signal must be synchronized to CLK.

CLK
Master Clock In
Input
This pin is a 20-MHz clock input.

REXT
External Reference
Input
This pin is used for an internal current reference. It must be tied to VDD via a 13-kΩ resistor with 1% tolerance.

VDD
Power
Power Pin
This pin supplies power to the device.

AVSS
Analog Ground
Ground Pin

This pin is the ground reference for the differential receivers and drivers.

DVSS
Digital Ground
Ground Pin

This pin is the ground reference for all the digital logic in the eIMR device.

FUNCTIONAL DESCRIPTION

The Am79C984A eIMR device is a single-chip implementation of an IEEE 802.3/Ethernet repeater (or hub). It is offered with four integral 10BASE-T ports plus one RAUI port comprising the basic repeater. The eIMR device is also expandable, enabling the implementation of high port count repeaters based on several eIMR devices.

The eIMR chip complies with the full set of repeater basic functions as defined in Section 9 of ISO 8802.3 (ANSI/IEEE 802.3c). The basic repeaters functions are summarized in the paragraphs below.

Basic Repeater Functions

The Am79C984A chip implements the basic repeater functions as defined by Section 9.5 of the ANSI/IEEE 802.3 specification.

Repeater Function

If any single network port senses the start of a valid packet on its receive lines, the eIMR device will retransmit the received data to all other enabled network ports (except when contention exists among any of the ports or when the receive port is partitioned). To allow multiple eIMR device configurations, the data will also be repeated on the expansion bus data line (DAT).

Signal Regeneration

When retransmitting a packet, the eIMR device ensures that the outgoing packet complies with the IEEE 802.3 specification in terms of preamble structure and timing characteristics. Specifically, data packets repeated by the eIMR device will contain a minimum of 56 preamble bits before the Start-of-Frame Delimiter. In addition, the eIMR restores the voltage amplitude of the repeated waveform to levels specified in the IEEE 802.3 specification. Finally, the eIMR device restores signal symmetry to repeated data packets, removing jitter and distortion caused by the network cabling. Jitter present at the output of the AUI port will be better than 0.5 ns; jitter at the TP outputs will be better than 1.5 ns.

The start-of-packet propagation delay for a repeater set is the time delay between the first edge transition of a data packet on its input port to the first edge transition of the repeated packet on its output ports. The start-of-packet propagation delay for the eIMR is within the specification given in Section 9.5.5.1 of the IEEE 802.3 standard.

Jabber Lockup Protection

The eIMR device implements a built-in jabber protection scheme to ensure that the network is not disabled by the transmission of excessively long data packets. This protection scheme causes the eIMR device to interrupt transmission for 96 bit-times if the device has been transmitting continuously for more than 65,536 bit times. This is referred to as MAU Jabber Lockup Protection (MJLP). The MJLP status for the eIMR device can be read through the Control Port, using the Get MJLP Status command.

Collision Handling

The eIMR device will detect and respond to collision conditions as specified in the IEEE 802.3 specification. Repeater configurations consisting of multiple eIMR devices also comply with the IEEE 802.3 specification, using status signals provided by the expansion bus. In particular, a repeater based on one or more eIMR devices will handle the transmit collision and one-port-left collision conditions correctly, as specified in Section 9 of the IEEE 802.3 specification.

Fragment Extension

If the total packet length received is less than 96 bits, including preamble, the eIMR device will extend the repeated packet length to 96 bits by appending a Jam sequence to the original fragment.

Auto Partitioning/Reconnection

Any of the TP ports or the AUI port can be partitioned if the duration or frequency of collisions becomes excessive. The eIMR device will continue to transmit data packets to a partitioned port, but will not respond, as a repeater, to activity on the partitioned port's receiver. The eIMR device will monitor the port and reconnect it once certain criteria are met. The criteria for reconnection are specified by the IEEE 802.3 standard. In addition to the standard reconnection algorithm, the eIMR device implements an alternative reconnection algorithm, which provides a more robust partitioning function for the TP ports and/or AUI port. The eIMR device partitions each TP port and the AUI port separately and independently of other network ports.

The eIMR device will partition an enabled network port if either of the following conditions occurs at that port:

a. A collision condition exists continuously for more than 2048 bit times. (AUI port—SQE signal active; TP port—simultaneous transmit and receive).
b. A collision condition occurs during each of 32 consecutive attempts to transmit to that port.

In the AUI port, a collision condition is indicated by an active SQE signal. In a TP port, a collision condition is indicated when the port is simultaneously attempting to transmit and receive.

Once a network port is partitioned, the eIMR device will reconnect that port, according to the selected reconnection algorithm, as follows:

a. Standard reconnection algorithm—A data packet longer than 512-bit times (nominal) is transmitted or received by the partitioned port without a collision.

b. Alternative reconnection algorithm—A data packet longer than 512-bit times (nominal) is transmitted by the partitioned port without a collision.

A partitioned port can also be reconnected by disabling and re-enabling the port.

All TP ports use the same reconnection algorithm; either they must all use the standard algorithm, or they must all use the alternative reconnection algorithm. However, the reconnection algorithm for the AUI port is programmed independently from that of the TP ports.

Detailed Functions

Reset

The eIMR device enters the reset state when the reset ($\overline{RST}$) pin is driven LOW. After the initial application of power, the $\overline{RST}$ pin must be held LOW for a minimum of 150 µs. If the $\overline{RST}$ pin is subsequently asserted while power is maintained to the eIMR device, a reset duration of only 4 µs is required. This allows the eIMR device to reset its internal logic. During reset, the eIMR registers are set to their default values. Also during reset, the eIMR device sets the output signals to their inactive state; that is, all analog outputs are placed in their idle state, no bidirectional signals are driven, all active-HIGH signals are driven LOW and all active-LOW signals are driven HIGH. In a multiple eIMR system, the reset signal must be synchronized to CLK. See Figure 10 in the *Systems Applications* section.

The eIMR device also monitors the state of the $\overline{SELI}_{0-1}$, SI, and AMODE pins on the rising (trailing) edge of $\overline{RST}$ to configure the operating mode of the device.

Table 1 summarizes the state of the eIMR chip following reset.

Table 1. eIMR States after Reset

Function	State after Reset	Pull Up/Pull Down
Active-LOW Outputs	HIGH	No
Active-HIGH Outputs	LOW	No
SO Output	HIGH	No
DAT, JAM	HIGH IMPEDANCE	Either
Transmitters (TP and AUI)	IDLE	No
Receivers (TP and AUI)	ENABLED	Terminated
AUI Partitioning/Reconnection Algorithm	STANDARD ALGORITHM	N/A
TP Partitioning/Reconnection Algorithm	STANDARD ALGORITHM	N/A
Link Test Functions for TP Ports	ENABLED, TP PORTS IN LINK FAIL	N/A
Automatic Receiver Polarity Reversal Function	DISABLED IF SI PIN IS HIGH ENABLED IF SI PIN IS LOW	N/A

AUI Port

The AUI Port is fully compatible with the IEEE 802.3, Section 7 requirement for an AUI port. It has the signals associated with an AUI port: DO, DI, and CI.

The AUI port has two modes of operation: normal and reverse. When configured for normal operation, the functionality is that of an AUI port on a MAC (CI is an input). When configured for reverse operation, the functionality is that of an AUI on a MAU (CI is an output). The mode of the AUI port is set during the trailing (rising) edge of the reset pulse, by the state of the AMODE pin. A LOW sets the AUI port to its normal mode (CI Input) and a HIGH sets the AUI port to its reversed (CI Output) mode.

The eIMR device can be connected directly to a MAC through the AUI port. This requires that the AUI port be configured for reverse operation. Refer to the *Systems Applications* section for more details.

TP Port Interface

Twisted Pair Transmitters

TXD is a differential twisted-pair driver. When properly terminated, TXD will meet the electrical requirements for 10BASE-T transmitters as specified in IEEE 802.3, Section 14.3.1.2.

The TXD signal is filtered on the chip to reduce harmonic content per IEEE 802.3, Section 14.3.2.1 (10BASE-T). Since filtering is performed in silicon, TXD can connect directly to a standard transformer, thereby, eliminating the need for external filtering modules. Proper termination is shown in the *Systems Applications* section.

Twisted Pair Receivers

RXD is a differential twisted-pair receiver. When properly terminated, RXD will meet the electrical requirements for 10BASE-T receivers as specified in IEEE 802.3, Section 14.3.1.3. The receivers do not require

external filter modules. Proper termination is shown in the *Systems Applications* section.

The receiver's threshold voltage can be programmed to an extended-distance mode. In this mode, the differential receiver's threshold is reduced to allow a longer cable than the 100 meters specified in the IEEE 802.3 standard. For programming details, refer to the *Control Commands* section.

Link Test

The integrated TP ports implement the Link Test function, as specified in the IEEE 802.3 10BASE-T standard. The eIMR device will transmit Link Test pulses to any TP port after that port's transmitter has been inactive for more than 8 ms to 17 ms. Conversely, if a TP port does not receive any data packets or Link Test pulses for more than 65 ms to 132 ms and the Link Test function is enabled for that port, then that port will enter the link-fail state. The eIMR device will disable a port in link-fail state (i.e., disable repeater transmit and receive functions) until it receives either four consecutive Link Test pulses or a data packet.

The Link Test function can be disabled via the eIMR control port on a port-by-port basis, to allow the eIMR device to operate with pre-10BASE-T networks that do not implement the Link Test function. When the Link Test function is disabled, the eIMR device will not allow the TP port to enter link-fail state, even if no Link Test pulses or data packets are being received. Note, however, that the eIMR device will always transmit Link Test pulses to all TP ports, regardless of whether or not the port is enabled, partitioned, in link-fail state, or has its Link Test function disabled. Separate control commands exist for enabling and disabling the transmission of Link Test pulses on a port-by-port basis.

Polarity Reversal

The TP ports can be programmed to receive data if a wiring error results in a data packet being received at a TP port with reversed polarity. This function will be enabled upon reception of a negative End Transmit Delimiter (ETD) or negative pulses and allows subsequent packets to be received with the correct polarity. The polarity-reversal function is executed once following reset or link-fail and can be programmed via the control port to be enabled or disabled on a port-by-port basis. The function may be enabled or disabled, following a reset, depending on the level of the SI signal on the rising edge of the $\overline{RST}$ pulse.

Visual Status Monitoring (LED) Support

The eIMR status port can be connected to LEDs to facilitate the visual monitoring of repeater port status. The status port has twelve output signals, LDA_{0-4}, and LDB_{0-4}, LDGA, and LDGB. LDA_{0-4} and LDB_{0-4} represent the four TP ports and AUI port. LDGA and LDGB are global indicators. Attributes that may be monitored are Carrier Sense (CRS), Collision (COL), Partition (PAR), Link Status (LINK), Loopback (LB), Port Disabled (DIS), and Jabber (JAB). Three control bits, LDC_{0-2}, select the particular attributes to be displayed on the LEDs. Table 2 shows how the programming combinations for LDC_{0-2} control the attributes that will be monitored.

Each LED drive pin (LDGA, LDGB, LDA_{0-4}, and LDB_{0-4}) has two states: Off and LOW. When none of the selected attributes are true, the driver is off and the diode is unlit. When an attribute is true, the driver is LOW, and the corresponding LEDs in Bank A or Bank B will be lit.

Some of the settings (LDC_2 = 1) include a blink function. This allows two attributes to be selected for a given state on the pin. As an example when LDC_{0-2} = 110, the LDA outputs relating to TP ports will be solidly lit when there is a link established at that port. However, whenever there is activity on a port, the corresponding LDA pin will switch on (LOW) and off at a period of 130 ms. Note that a partition on that port will also cause the pin to go LOW.

On LDC settings that have two attributes for a state on a pin (blink or solid-on), the attribute causing the output to blink has priority. (Those attributes are shown in Table 2 with a blink period specified next to it.) If an attribute has no blink period specified, the LED indicates the attribute by being solidly lit.

The LEDs can also be controlled via the control port. The Enable Software Override commands turn the LEDs on regardless of the attributes selected for display through the LDC setting. Enable Software Override of Bank A LEDs causes the LDA_{0-4} and LDGA pins to be driven LOW, and Enable Software Override of Bank B LEDs causes the LDB_{0-4} and LDGB pins to be driven LOW. The blink rate is set by the Software Override LED Blink Rate command. The periods are off, 512 ms, 1560 ms, or solid on.

Table 2. LED Attribute-Monitoring Program Options

LED Control			Global LEDs		TP LEDs		AUI LEDs	
LDC_2	LDC_1	LDC_0	LDGA	LDGB	LDA_{1-4}	LDB_{1-4}	LDA_0	LDB_0
0	0	0	CRS	COL	LINK (Note 2)	PAR	LB	PAR
0	0	1	CRS	COL	LINK	CRS	LB	CRS
0	1	0	Reserved (Note 5)					
0	1	1	Reserved (Note 5)					
1	0	0	CRS 260-ms blk	COL 260-ms blk	LINK CRS 260-ms blk	PAR COL 260-ms blk	CRS 260-ms blk	PAR COL 260-ms blk
1	0	1	COL	JAB	LINK (Note 3) CRS 512-ms blk	PAR (Note 3)	(Note 3) CRS 512-ms blk	PAR (Note 3)
1	1	0	CRS	COL	LINK CRS 130-ms blk	PAR or DIS	CRS 130-ms blk	PAR or DIS
1	1	1	CRS	COL	LINK (Note 4) PAR 1.56-s blk	COL (Note 4)	(Note 4) PAR 1.56-s blk	$\overline{PAR}$ (Note 4)

Notes:

1. *CRS = Carrier Sense, COL = Collision, JAB = Jabber, LINK = Link, LB = Loop Back, PAR = Partition, DIS = Port Disabled, blk = Blink (Number = period of Blink).*
2. *For the LDC_{0-2} setting of 000: If the port is partitioned, the LINK LED is off.*
3. *All LEDs blink 16 times at 260 ms per blink after reset.*
4. *All LEDs are on for approximately 4 seconds after reset.*
5. *LDC_{0-2} = '010' and '011' are undefined.*

LED software override is executed in two stages, by first issuing the blink rate (Software Override of LED Blink Rate) and then issuing the command to enable the particular port LEDs (Enable Software Override of Bank A/B LEDs). All port combinations selected for software override control will reference the blink rate last issued by the Software Override of the LED Blink Rate command.

LDA_{0-4}, LDB_{0-4}, LDGA, and LDGB are open drain output drivers that sink 12 mA of current to turn on the LEDs. In a multiple eIMR configuration, the outputs from the global LED drivers (LDGA and LDGB) of each chip can be tied together to drive a single pair of global status LEDs.

CRS and COL are extended to make it easier for visual recognition; that is, they will remain active for some time even if the corresponding condition has expired. Once carrier sense is active, CRS will remain active for a minimum of 4 ms. Once a collision is detected, COL is active for at least 4 ms. The exception to this rule is for selection LDC_{0-2} = 111. For this selection, COL is stretched to 100 µs.

When LDC_{0-2} = 000 or LDC_{0-2} = 001, the loopback attribute (LB) for the AUI port is displayed on LDA_0. LB is true when DO on the MAU is successfully looped back to DI on the AUI port. LB is false (off) if a loopback error is detected, or if the AUI port is disabled or in the reverse mode. Transmit carrier sense is sampled at the end of packet to determine the state of LB. The state of LB remains latched until carrier sense is sampled again for the next packet. The default/power-up state for LB is false (off).

Figure 1 shows the recommended connection of LEDs. When LDA_{0-4}, LDB_{0-4}, LDGA, or LDGB are LOW, the LED lights.

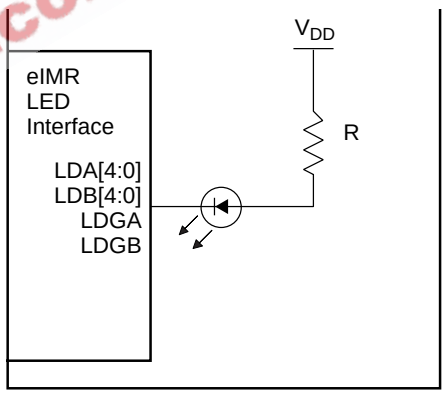

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Figure 1. Visual Monitoring Application—Direct LED Drive

Network Activity Display

The eIMR status port can drive up to eight LEDs to indicate the network-utilization level as a percentage of bandwidth. The status port uses eight dedicated outputs (ACT_{0-7}) to drive a series of LEDs. The number of LEDs in the series that will be lit increases as the amount of network activity increases. ACT_0 represents the lowest level of activity; ACT_7 represents the highest. ACT_{0-7} are open-drain outputs that typically sink 12 mA of current to turn on the LEDs. See Figure 2.

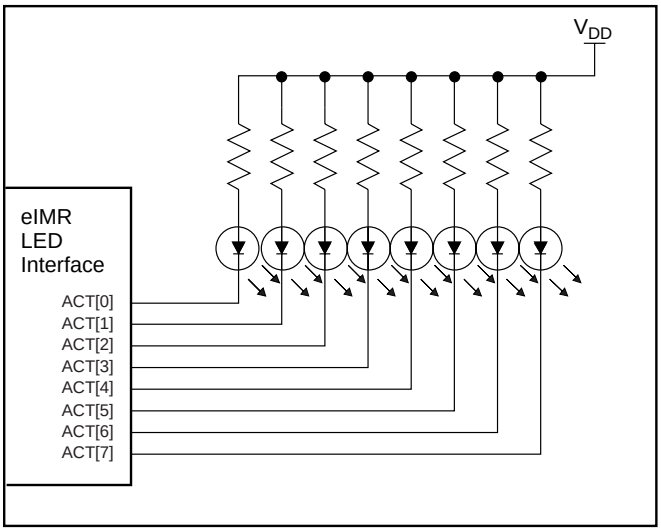


Figure 2. Network Activity Display

Table 3 shows ACT_{0-7} as a function of the percentage of network utilization. The table uses a scale that is more sensitive at low utilization levels. 100% utilization represents the maximum number of events that could occur in a given window of time.

The update rate and corresponding internal sampling window for ACT[7:0] is 250 ms. During this sampling window, a counter is used to count the number of times repeater transmit activity is TRUE. The counter uses a free-running clock which has the granularity to detect the minimum packet size of 96 bit times.

Figure 3 shows the timing relationship between the sampling window, counting clock, and transmit activity.

Table 3. Network Utilization

Number of LEDs Lit by ACT_{7-0}	Percentage Utilization
8	>80%
7	>64%
6	>32%
5	>16%
4	>8%
3	>4%
2	>2%
1	>1%

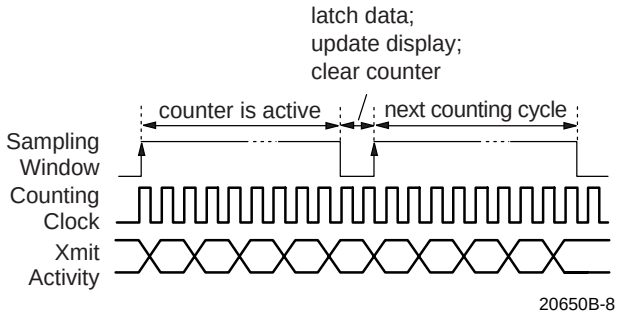


Figure 3. Activity Sampling

Expansion Bus Interface

The eIMR device expansion bus allows multiple eIMR devices to be interconnected.

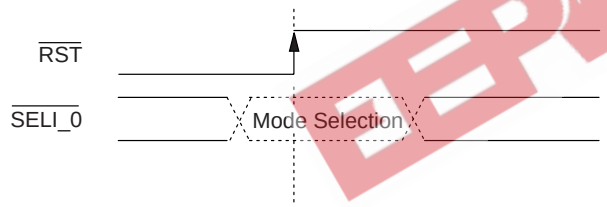
The expansion bus supports two modes of operation: internal arbitration mode and IMR+ mode. The internal arbitration mode uses a modified daisy-chain scheme to eliminate the need for any external arbitration circuitry. The IMR+ mode maintains the full functionality of the IMR+ (Am79C981) expansion bus and benefits from minimum delays. In this mode, the eIMR device requires external circuitry to handle arbitration for control of the bus.

The eIMR arbitration mode is determined at reset. This occurs on the trailing edge of $\overline{RST}$ according to the state of $\overline{SELI}_{0-1}$, as illustrated in Figure 4.

Internal Arbitration Mode

The internal arbitration mode uses a daisy-chain (cascade) configuration. $\overline{SELI}_{0-1}$ are arbitration inputs and $\overline{SELO}$ is the arbitration output. $\overline{SELO}$ goes LOW when there is activity on one or more of the eIMR ports, or a $\overline{SELI}$ input is LOW. The $\overline{SEL}$ lines are connected as shown in Figure 5. This technique allows activity indication to propagate down the chain to the end device. All unused $\overline{SELI}$ inputs must be tied to VDD.

$\overline{ACK}$ and $\overline{COL}$ are global activity I/O pins. When the eIMR device senses activity, it drives $\overline{ACK}$ LOW.



$\overline{SELI\_1}$	$\overline{SELI\_0}$	Arbitration Mode
X	1	Internal
X	0	IMR+

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Figure 4. Expansion Bus Mode Selection

An eIMR device drives $\overline{COL}$ LOW when it senses more than one device is active; that is, if the device has an active port AND a $\overline{SELI}$ input is LOW, OR both $\overline{SELI}$ inputs are LOW. In Boolean notation, the formula for $\overline{COL}$ is:

$$\overline{COL} = (\text{Active port} \,\&\, (\overline{SELI}_1 + \overline{SELI}_0)) + (\overline{SELI}_1 \,\&\, \overline{SELI}_0)$$

where

& represents the Boolean AND operation
+ represents the Boolean OR operation

$\overline{ACK}$ and $\overline{COL}$ are mutually exclusive. If an eIMR driving $\overline{ACK}$ senses $\overline{COL}$ LOW, the device will deassert $\overline{ACK}$.

DAT and JAM are synchronized to CLK. DAT is the repetition of data from any connected port (either TP or AUI port) encoded in NRZ format. JAM is an internal collision indicator. If JAM is HIGH, the active eIMR device has detected an internal collision across one or more of its ports. When this occurs, the DAT signal distinguishes between single-port collisions and multiport collisions. DAT = 1 indicates a single port collision; DAT = 0 indicates a multiport collision.

The drive capabilities of the I/O signals on the expansion bus (DAT, JAM, $\overline{ACK}$, and $\overline{COL}$) are sufficient to allow seven eIMR devices to be connected together without the use of external transceivers or buffers.

The maximum number of eIMR devices that can be daisy chained is limited by the propagation delay of the eIMR devices. In practice, the depth of the cascade is limited to three eIMR devices, thus allowing a maximum of seven eIMR devices connected together via this expansion bus as shown in Figure 5.

The active device will not drive the data line, DAT, until one bit time (100 ns) after $\overline{SELO}$ goes LOW. This is to avoid a situation where two devices drive DAT simultaneously.

IMR+ Mode

In IMR+ mode, the expansion bus requires an external arbiter. The arbiter allows only one eIMR device to control the expansion bus. If more than one device attempts to take control, the arbiter terminates all access and signals a collision condition.

In IMR+ mode, DAT and JAM retain the same functionality as in internal arbitration mode, but $\overline{ACK}$ and $\overline{COL}$ are inputs to the eIMR device, driven by the external arbiter. The arbiter should drive $\overline{ACK}$ LOW when exactly one eIMR device is active. It should drive $\overline{COL}$ when more than one eIMR device is active. $\overline{SELO}$ is an output from the eIMR device. It indicates that the eIMR device has an active port and is requesting access to the bus.

When $\overline{ACK}$ is HIGH, DAT and JAM are in the high-impedance state. DAT and JAM go active when $\overline{ACK}$ goes LOW. Refer to the *Systems Applications* section (Figure 13) for the configuration of IMR+ mode of operation.

Note: *The IMR+ mode is recommended when arbitrating between multiple boards.*

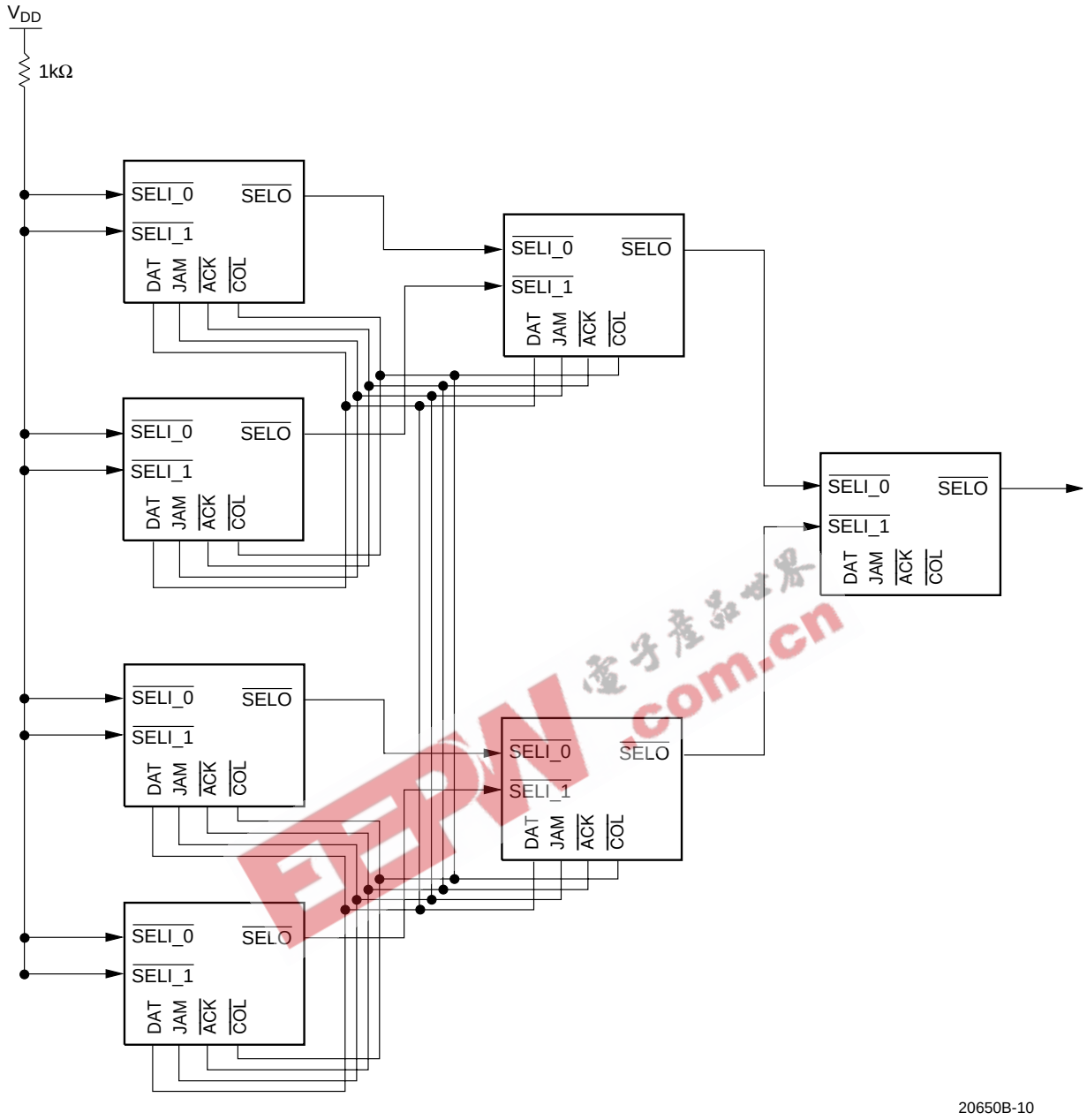


Figure 5. Internal Arbitration—eIMR Devices in Cascade

Control Functions

The eIMR device receives control commands in the form of byte-length data on the serial input pin, SI. If the eIMR device is expected to provide data in response to the command, it will send byte-length data to the serial-output pin, SO. Both the input and output data streams are clocked with the rising edge of the SCLK signal. The byte-length data is in RS232 serial-data format; that is, one start bit followed by eight data bits. The externally generated clock at the SCLK pin may be either a free-running clock synchronized to the input bit patterns, or a series of individual transitions meeting the setup-and-hold times with respect to the input bit pattern. If the latter method is used, 20 SCLK clock transitions are required for control commands that produce SO data, and 14 SCLK clock transitions are required for control commands that do not produce SO data.

Command/Response Timing

Figure 6 shows the command/response timing. At the end of a GET command, the eIMR device waits two SCLK cycles and then transmits the response on SO.

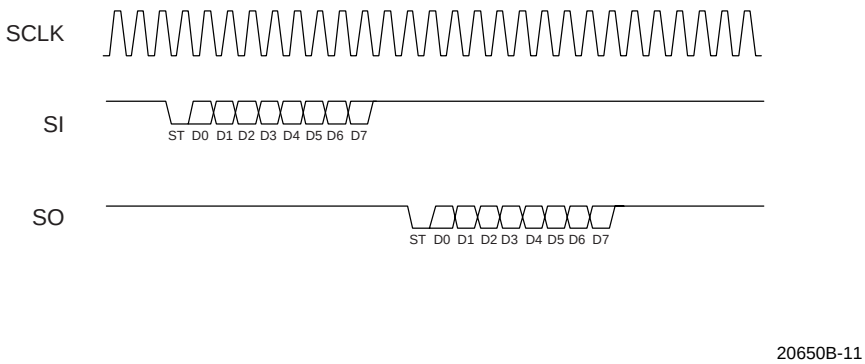


Figure 6. Control Get Command/Response

Control Commands

The following section details the operation of each control commands available in the eIMR device. In all cases, the individual bits in each command are shown with the most-significant bit (bit 7) on the left and the least-significant bit (bit 0) on the right. Table 4 and Table 5 show a summary of default states and a summary of control commands, respectively.

Note: *Data is transmitted and received on the serial data lines least-significant bit first and most-significant bit last.*

Table 4. Summary of Default States after Reset

eIMR Programmable Option—S	Off
AUI Partitioning Algorithm	Normal
TP Partitioning Algorithm	Normal
AUI/TP Port	Enabled
Link Test	Enabled
Link Pulse	Enabled
Automatic Receiver Polarity Reversal	State of SI at reset
Extended Distance Mode	Disabled
Blink Rate	Off
Software Override of LEDs	Disabled

Table 5. Control Port Command Summary

Commands	SI Data	SO Data
Set (Write Commands)		
eIMR Chip Programmable Options	0000 10S0	
Alternate AUI Partitioning Algorithm	0001 1111	
Alternate TP Partitioning Algorithm	0001 0000	
AUI Port Disable	0010 1111	
AUI Port Enable	0011 1111	
TP Port Disable	0010 00##	
TP Port Enable	0011 00##	
Disable Link Test Function (per TP port)	0100 00##	
Enable Link Test Function (per TP port)	0101 00##	
Disable Link Pulse (per TP port)	0100 10##	
Enable Link Pulse (per TP port)	0101 10##	
Disable Automatic Receiver Polarity Reversal (per TP port)	0110 00##	
Enable Automatic Receiver Polarity Reversal (per TP port)	0111 00##	
Disable Receiver Extended Distance Mode (per TP port)	0110 10##	
Enable Receiver Extended Distance Mode (per TP port)	0111 10##	
Disable Software Override of LEDs (per Port - AUI & TP)	1001 ####	
Enable Software Override of Bank A LEDs (per Port - AUI & TP, Global)	1011 ####	
Enable Software Override of Bank B LEDs (per Port - AUI & TP, Global)	1100 ####	
Software Override LED Blink Rate	1110 1###	
Get (Read Commands)		
AUI Port Status (B, S, and L Cleared)	1000 1111	PBSL 0000
AUI Port Status (B Cleared)	1000 1101	PBSL 0000
AUI Port Status (S, L, Cleared)	1000 1011	PBSL 0000
AUI Port status (None Cleared)	1000 1001	PBSL 0000
TP Port Partitioning Status	1000 0000	0000 C3..C0
Bit Rate Error Status of TP Ports	1010 0000	0000 E3..E0
Link Test Status of TP Ports	1101 0000	0000 L3..L0
Receive Polarity Status of TP Ports	1110 0000	0000 P3..P0
MJLP Status	1111 0000	M000 0000
Version	1111 1111	0000 0011

SET (Write Commands)

Chip Programmable Option

SI Data	0000 10S0
SO Data	None

The eIMR chip programmable option can be enabled (or disabled) by setting (or resetting) the S bit in the command string.

S AUI SQE Test Mask

Setting this bit allows the eIMR chip to ignore activity on the CI signal pair, during the SQE test window, following a transmission on the AUI port. Enabling this function does not prevent the reporting of this condition by the eIMR device. The two functions operate independently.

The SQE Test Window, as defined in IEEE 802.3 (Section 7.2.2.2.4) is from 6 bit times to 34 bit times (0.6 µs to 3.4 µs). This includes the delay introduced by a 50-meter AUI. CI activity that occurs outside this window is not ignored and is treated as a true collision.

Alternate AUI Partitioning Algorithm

SI Data	0001 1111
SO Data	None

Invoking this command sets the partition/reconnection scheme for the AUI port to the alternate (transmit-only) reconnection algorithm. To return the AUI port to the standard (transmit or receive) reconnection algorithm, it is necessary to reset the eIMR device. The standard partitioning algorithm is selected on reset.

Alternate TP Partitioning Algorithm

SI Data	0001 0000
SO Data	None

Invoking this command sets the partition/reconnection scheme for the TP ports to the alternate (transmit-only) reconnection algorithm. To return the TP ports to the standard (transmit or receive) reconnection algorithm, it is necessary to reset the eIMR device. The standard partitioning algorithm is selected on reset.

AUI Port Disable

SI	0010 1111
SO Data	None

This command disables the AUI port. Subsequently, the eIMR chip will ignore all inputs to this port and will not transmit a DAT or JAM pattern on the AUI port. Disabling the AUI port also sets the partitioning state machine of the AUI port to the idle state. Therefore, a partitioned port can be reconnected by first disabling the AUI port and then enabling the AUI port.

AUI Port Enable

SI	0011 1111
SO Data	None

This command enables the AUI port.

TP Port Disable

SI Data	0010 00##
SO Data	None

This command disables the TP port designated by the two least-significant bits of the command byte. Subsequently, the eIMR chip will ignore all inputs to the designated port and will not transmit a DAT or JAM pattern on that port. Disabling the TP port also sets the partitioning state machine of that port to the idle state. Therefore, a partitioned port can be reconnected by first disabling the port and then enabling it.

TP Port Enable

SI Data	0011 00##
SO Data	None

This command enables the TP port designated by the two least-significant bits of the command byte.

Disable Link Test Function (Per TP port)

SI Data	0100 00##
SO Data	None

This command disables the Link Test function of the TP port designated by the two least-significant bits of the command data. As a consequence of this, the port will no longer be disconnected if it fails the Link Test. If a port has the Link Test disabled, reading the Link Test Status indicates a 'Link Pass'.

Enable Link Test Function (Per TP port)

SI Data	0101 00##
SO Data	None

This command enables the Link Test function of the TP port designated by the two least-significant bits of the command data. As a consequence of this, the port is disconnected if it fails the Link Test.

Disable Link Pulse (Per TP Port)

SI Data	0100 10##
SO Data	None

This command disables the transmission of the Link pulse on the TP port designated by the two least-significant bits of the command byte.

Enable Link Pulse (Per TP Port)

SI Data	0101 10##
SO Data	None

This command enables the transmission of the Link pulse on the TP port designated by the two least-significant bits of the command byte.

Disable Automatic Receiver Polarity Reversal (Per TP Port)

SI Data	0110 00##
SO Data	None

This command disables the Automatic Receiver Polarity Reversal function for the TP port designated by the two least-significant bits in the command byte. If this function is disabled on a TP port receiving with reversed polarity (due to a wiring error), the TP port will fail the Link Test due to the incorrect polarity of the received Link pulses.

The state of Automatic Polarity Reversal function is set by SI on reset. If SI is HIGH at the rising edge of $\overline{RST}$, the eIMR device disables Automatic Polarity Reversal. If SI is LOW at the rising edge of $\overline{RST}$, the eIMR device enables Automatic Polarity Reversal.

Enable Automatic Receiver Polarity Reversal (Per TP Port)

SI Data	0111 00##
SO Data	None

This command enables the Automatic Receiver Polarity Reversal function for the TP port designated by the two least-significant bits in the command byte. If enabled in a TP port, the eIMR chip will automatically invert the polarity of that port's receiver circuitry if the TP port is detected as having reversed polarity (due to wiring error). After reversing the receiver polarity, the TP port could then receive subsequent (reverse polarity) packets correctly.

Disable Receiver Extended Distance Mode (Per TP Port)

SI Data	0110 10##
SO Data	None

This command disables the Receiver Extended Distance Mode and restores the RXD circuit of the transceiver to normal squelch levels for the TP port driver designated by the two least-significant bits of the command data.

Enable Receiver Extended Distance Mode (Per TP Port)

SI Data	0111 10##
SO Data	None

This command modifies the RXD circuit of the transceiver for the TP port driver designated by the two least-significant bits of the command data. The RXD squelch-threshold value is lowered to accommodate signal attenuation associated with lines longer than 100 meters. At reset, Receiver Extended Distance Mode is disabled and the RXD circuit defaults to normal squelch-threshold values.

Disable Software Override of LEDs (Per Port - AUI and TP, Global)

SI Data	1001 ####
SO Data	None

This command disables Software Override of the Port LEDs.

Individual LEDs and combinations of LEDs can be selected via the lower four bits of the command byte as follows:

####	*Port(s) affected*
0000-0011	TP0 - TP3
0100-0111	Reserved
1000	AUI port
1001	Reserved
1010	Reserved
1011	All TP ports
1100	All ports
1101	Global
1110	Reserved
1111	Reserved

Following command execution, the attributes displayed on the LEDs will be determined by LDC_{0-2}. Software Override of LEDs is disabled after reset.

Enable Software Override of Bank A LEDs (Per Port - AUI and TP, Global)

SI Data	1011 ####
SO Data	None

This command forces the LEDs in Bank A to blink. Individual LEDs and combinations of LEDs can be selected via the lower four bits of the command byte as follows:

####	*Port(s) affected*
0000-0011	TP0 - TP3
0100-0111	Reserved
1000	AUI port
1001	Reserved
1010	Reserved
1011	All TP ports
1100	All ports
1101	Global
1110	Reserved
1111	Reserved

The designated LED driver(s) will switch between LOW and 'off' at the rate set by the Software Override Blink Rate command. Enable Software Override of Bank A LEDs references the blink rate last issued and overrides any other attribute specified by LDC_{0-2}. Software Override of LEDs is disabled after reset.

Enable Software Override of Bank B LEDs (Per Port - AUI and TP, Global)

SI Data	1100 ####
SO Data	None

This command forces the LEDs in Bank B to blink. Individual LEDs and combinations of LEDs can be selected via the lower four bits of the command byte as follows:

####	Port(s) affected
0000-0011	TP0 - TP3
0100-0111	Reserved
1000	AUI port
1001	Reserved
1010	Reserved
1011	All TP ports
1100	All ports
1101	Global
1110	Reserved
1111	Reserved

The designated LED driver(s) will switch between LOW and 'off' at the rate set by the Software Override of LED Blink Rate command. Enable Software Override of Bank B LEDs references the blink rate last issued and overrides any other attribute specified by LDC_{0-2}. Software Override of LEDs is disabled after reset.

Software Override of LED Blink Rate

SI Data	1110 1###
SO Data	None

This command sets the blink period of the LEDs with Software Override enabled. The duty cycle is 50%. This command defaults to 'off' at reset.

Setting	Blink Period
1110 1000	Off
1110 1001	512 ms
1110 1010	1560 ms
1110 1011	Solid On

These settings apply to the blink rate for both Bank A and Bank B. This command must precede the Enable Software Override of Bank A/B LEDs command. All LED combinations selected for Software Override will reference the blink rate last issued.

GET (Read Commands)

AUI Port(s) Status

SI Data	1000 1111
SO Data	PBSL 0000

The combined AUI status of the eIMR device allows a single instruction to be used to monitor the AUI port. The four local status bits are:

P Partitioning Status

This bit is '0' if the AUI port is partitioned and '1' if the AUI port is connected.

B Bit Rate Error

This bit is set to '1' if there is an instance of FIFO overflow or underflow. The bit is cleared when the eIMR device is read.

S SQE Test Status

This bit is set to '1' if the SQE test error is detected by the eIMR chip. The bit is cleared when the status is read.

L Loopback Error

The MAU attached to the AUI port is required to loopback data transmitted to DO onto the DI circuit. If the loopback carrier is not detected by the eIMR device, this bit is set to '1'. This bit is cleared when the status is read.

Alternate AUI Port(s) Status

There are three further variations of the AUI Port Status Command allowing selective clearing of a combination of B,S, and L bits. These are the following:

Alternate 1: B is not cleared, S and L are Cleared

SI Data	1000 1011
SO Data	PBSL 0000

Alternate 2: S and L are not cleared, B is Cleared

SI Data	1000 1101
SO Data	PBSL 0000

Alternate 3: None of S, B, and L are Cleared

SI Data	1000 1001
SO Data	PBSL 0000

TP Port Partitioning Status

SI Data	1000 0000
SO Data	0000 P3..P0

P*n* = 0	TP Port Partitioned
P*n* = 1	TP port Connected

where *n* is a port number in the range 0–3.

The response to this command gives the partitioning status of all four TP ports. If a port is disabled, reading its partitioning status will indicate that it is connected.

Bit Rate Error Status of TP Ports

SI Data	1010 0000
SO Data	0000 E3..E0

E*n* = 0	No Error
E*n* = 1	FIFO Overflow

where *n* is a port number in the range 0–3.

The response to this command gives the bit-rate-overflow or underflow (data rate mismatch) condition of all the TP ports. A 1 indicates that the FIFO has overflowed or underflowed due to the amount of data received by the corresponding port.

Link Test Status of TP ports

SI Data	1101 0000
SO Data	0000 L3..L0

L*n* = 0 TP Port n in Link Test Failed
L*n* = 1 TP port n in Link Test Passed
where *n* is a port number in the range 0–3.

The response to this command gives the Link Test status of all the TP ports. A disabled port continues to report Link Test status. Re-enabling the port causes the port to be placed in the Link Test Fail state.

Receive Polarity Status of TP Ports

SI Data	1110 0000
SO Data	0000 P3.....P0

P*n* = 0 TP Port n Polarity Correct
P*n* = 1 TP port n Polarity Reversed
where *n* is a port number in the range 0–3.

The response to this command gives the Received Polarity status of all the TP ports. If the polarity is detected as reversed for a TP port, then the eIMR device will set the appropriate bit in this command's result only if the Polarity Reversal Function is enabled for that port.

MJLP Status

SI Data	1111 0000
SO Data	M000 0000

Each eIMR device contains an independent MAU Jabber Lock Up Protection timer. The timer is designed to inhibit the transmit function of the eIMR device if it has been transmitting continuously for more than 65536 bit times. This bit remains set and is only cleared when the MJLP status is read using this command.

Version

SI Data	1111 1111
SO Data	0000 0011

The response to this command gives the version of the eIMR device. 0011 was chosen to help distinguish the eIMR device from the IMR (Am79C980) and the IMR+ (Am79C981) devices.

SYSTEMS APPLICATIONS

eIMR to TP Port Connection

The eIMR device provides a system solution to designing non-managed multiport repeaters. The eIMR device connects directly to AC coupling modules for a 10BASE-T hub. Figure 7 shows the simplified connection.

Twisted Pair Transmitters

TXD signals need to be properly terminated to meet the electrical requirement for 10BASE-T transmitters. Proper termination is shown in Figure 8 which consists of a 110-Ω resistor and a 1:1 transformer. The load is a twisted-pair cable that meets IEEE 802.3, Section 14.4 specifications. The cable is terminated at the opposite end by 100 Ω.

Twisted Pair Receivers

RXD signals need to be properly terminated to meet the electrical requirements for 10BASE-T receivers. Proper termination is shown in Figure 9. Note that the receivers do not require external filter modules.

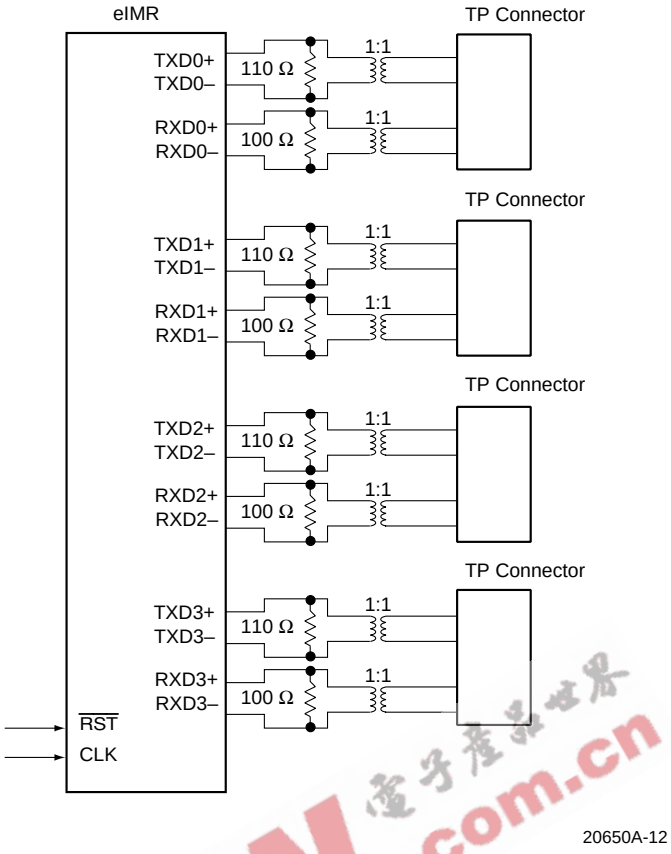


Figure 7. Simplified 10BASE-T Connection

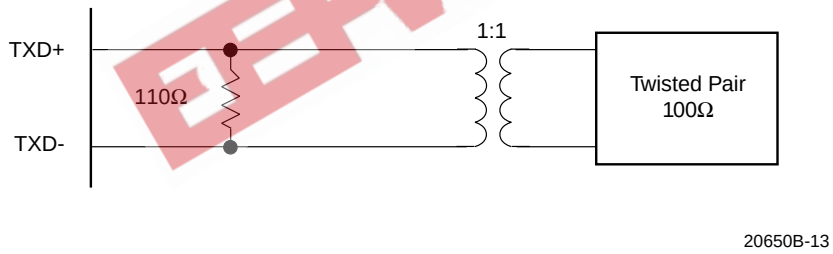


Figure 8. TXD Termination

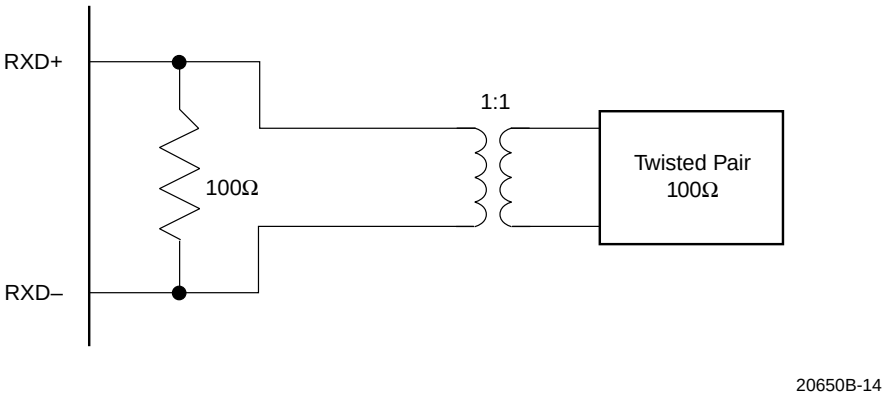
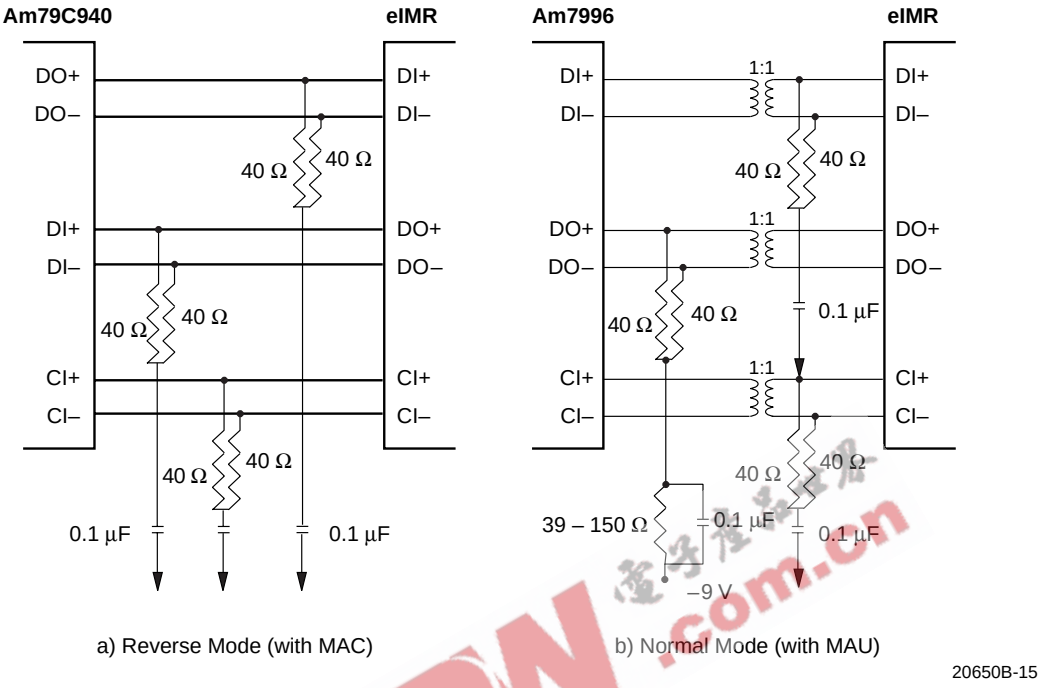


Figure 9. RXD Termination

MAC Interface

The eIMR device can be connected directly to a MAC through the AUI port. This requires that the AUI port be configured in the reverse mode and connected as shown in Figure 10a. Notice that DI is connected to DO of the MAC and DO is connected to DI of the MAC, because the reverse configuration only affects CI. Where CI is an input in the normal mode, in the reverse mode, CI is an output. Figure 10b shows the normal AUI configuration for reference.



a) Reverse Mode (with MAC)

b) Normal Mode (with MAU)

20650B-15

Figure 10. AUI Port Interconnections

Internal Arbitration Mode Connection

The internal arbitration mode uses a modified daisy-chain scheme to eliminate the need for any external arbiter. In this mode, $\overline{ACK}$ and $\overline{COL}$ need to be pulled up through a minimum resistance of 1 kΩ. The DAT and JAM pins also need to be pulled down via a high value resistor. Refer to Figure 11.

IMR+ Mode External Arbitration

The IMR+ mode maintains the full functionality of AMD's IMR+ (Am79C981) device's expansion bus. In this mode, the eIMR device requires external circuitry to handle arbitration for control of the bus. Figure 12 shows the configuration for the IMR+ mode of operation.

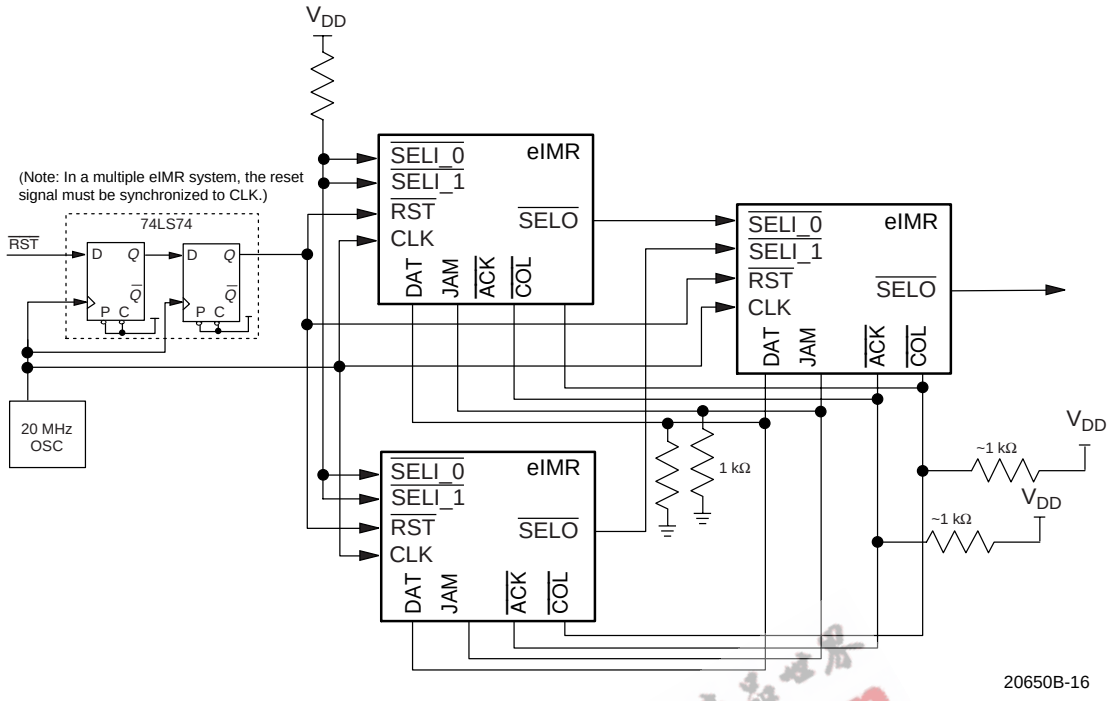


Figure 11. eIMR Internal Arbitration Mode Connection

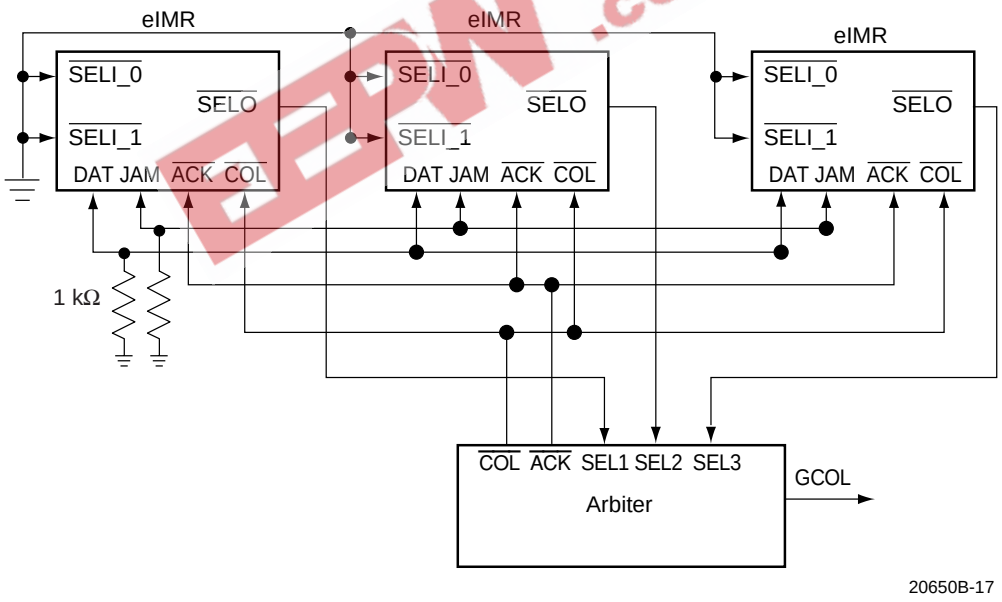


Figure 12. IMR+ Mode External Arbitration

Visual Status Display

LDA/B[4:0] and LDGA/B provide visual status indicators for the eIMR. LDA/B[4:0] displays Link, Carrier Sense, Collision, and Partition information for the TP and AUI ports. LDGA/B display global Carrier Sense, Collision, and Jabber information.

In a multiple eIMR configuration, the global LED drivers (LDGA/B) from each chip can be tied together to drive a single pair of global status LEDs. The open drain output of these drivers facilitate this configuration. Refer to Figure 13.

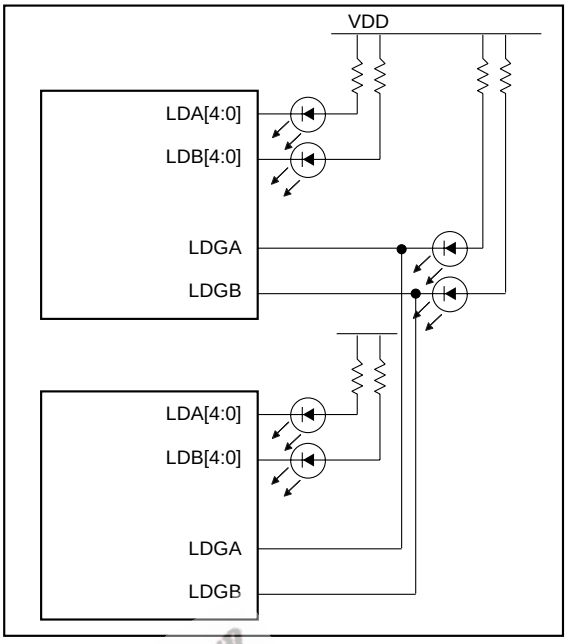


Figure 13. Visual Status Display Connection

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65° C to +150° C

Ambient Temperature Under Bias . . . . 0° C to +70° C

Supply Voltage referenced to

AV_{SS} or DV_{SS} (AV_{DD}, DV_{DD}) . . . . . –0.3 V to +6.0 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) . . . . . 0° C to +70° C

Supply Voltages (V_{DD}) . . . . . +5 V ±5%

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
Digital I/O					
V_{IL}	Input LOW Voltage	V_{SS} = 0.0 V	–0.5	0.8	V
V_{IH}	Input HIGH Voltage	V_{SS} = 0.0 V	2.0	0.5 + V_{DD}	V
V_{OL}	Output LOW Voltage	I_{OL} = 4.0 mA	–	0.4	V
V_{OH}	Output HIGH Voltage	I_{OH} = –0.4 mA	2.4	–	V
I_{IL}	Input Leakage Current	V_{SS}<V_{IN}<V_{DD}	–	10	µA
I_{ILSTR}	Input Leakage Current for STR pin	V_{SS}<V_{IN}<V_{DD}	–	50	µA
V_{OLOD}	Open Drain Output LOW Voltage (LED pins)	I_{OLOD} = 12 mA	–	0.4	V
AUI Ports					
I_{IAXD}	Input Current at DI± and CI± Pairs	V_{SS}<V_{IN}<V_{DD}	–500	500	µA
V_{AICM}	DI±, CI± Open Circuit Input Voltage Range	I_{IN} = 0	V_{DD} – 3.0	V_{DD} – 1.0	V
V_{AIDV}	Differential Mode Input Voltage Range (DI, CI)	V_{DD} = 5.0 V	–2.5	+2.5	V
V_{ASQ}	DI, CI Squelch Threshold	–	–275	–160	mV
V_{ATH}	DI Switching Threshold	(Note 1)	-35	+35	mV
V_{AOD}	Differential Output Voltage |(DO+) – (DO)|	R_L = 78 Ω	620	1100	mV
V_{AOC}	Differential Output Voltage |(CI+) – (CI–)| (Reverse Mode)	R_L = 78 Ω	620	1100	mV
V_{AODI}	DO Differential Output Voltage Imbalance	R_L = 78 Ω	–25	+25	mV
V_{AOD}OFF	DO Differential Idle Output Voltage	R_L = 78 Ω	–40	+40	mV
I_{AOD}OFF	DO Differential Idle Output Current	R_L = 78 Ω (Note 1)	–1.0	+1.0	mA
V_{AOCM}	DO+, DO- Common Mode Output Voltage	R_L = 78 Ω	2.5	V_{DD}	V
Twisted Pair Ports					
I_{IRXD}	Input Current at RXD± and CI± Pairs	AV_{SS}<V_{IN}<V_{DD}	–500	500	µA
R_{RXD}	RXD Differential Input	(Note 1)	10	–	kΩ
V_{TIVB}	RXD+, RXD– Open Circuit Input Voltage (bias)		V_{DD} – 3.0	V_{DD} – 1.5	V
V_{TID}	Differential Mode Input Range (RXD)	V_{DD} = 5.0 V	–3.1	+3.1	V

DC CHARACTERISTICS (continued)

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
Twisted Pair Ports (Continued)					
V_{TSQ+}	RXD Positive Squelch Threshold (peak)	Sinusoid 5 MHz<f<10 MHz	300	520	mV
V_{TSQ-}	RXD Negative Squelch Threshold (peak)	Sinusoid 5 MHz<f<10 MHz	–520	–300	mV
V_{THS+}	RXD Post-Squelch Positive Threshold (peak)	Sinusoid 5 MHz<f<10 MHz	150	293	mV
V_{THS-}	RXD Post-Squelch Negative Threshold (peak)	Sinusoid 5 MHz<f<10 MHz	–293	–150	mV
V_{LTSQ+}	RXD Positive Squelch Threshold (peak) - Extended Distance Mode	Sinusoid 5 MHz<f<10 MHz	180	365	mV
V_{LTSQ-}	RXD Negative Squelch Threshold (peak) - Extended Distance Mode	Sinusoid 5 MHz<f<10 MHz	–365	–180	mV
V_{LTHS+}	RXD Post-Squelch Positive Threshold - Extended Distance Mode	Sinusoid 5 MHz<f<10 MHz	90	175	mV
V_{LTHS-}	RXD Post-Squelch Negative Threshold - Extended Distance Mode	Sinusoid 5 MHz<f<10 MHz	–175	–90	mV
V_{RXDTH}	RXD Switching Threshold	(Note 1)	–60	60	mV
Power Supply Current					
I_{DD}	Power Supply Current (Idle) (Note 2)	CLK = 20 MHz V_{DD} = +5.25V	–	100	mA
	Power Supply Current (Transmitting)	CLK = 20 MHz V_{DD} = +5.25V	–	350	mA

Notes:

1. *Parameter not tested.*
2. *LED current not included. Maximum current rating on LED drivers is 12 mA.*

SWITCHING CHARACTERISTICS

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
Clock and Reset Timing					
t_{CLK}	CLK Clock Period		49.995	50.005	ns
t_{CLKH}	CLK Clock High		20	30	ns
t_{CLKL}	CLK Clock Low		20	30	ns
t_{CLKR}	CLK Rise Time		–	10	ns
t_{CLKF}	CLK Fall Time		–	10	ns
t_{PRST}	Reset Pulse Width after Power On		150	–	µs
t_{RST}	Reset Pulse Width		4	–	µs
t_{RSTSET}	Reset HIGH Setup Time with respect to CLK		15	–	ns
t_{RSTHLD}	Reset LOW Hold Time		0	–	ns
t_{XRS}	AMODE, $\overline{SELI}_0$, and SI_D Setup Time to Rising Edge of $\overline{RST}$		0	–	ns
t_{XRH}	AMODE,$\overline{SELI}_0$, and SI_D Hold Time from Rising Edge of $\overline{RST}$		400	–	ns
AUI Port Timing					
t_{DOTD}	CLK Rising Edge to DO Toggle		–	30	ns
t_{DOTR}	DO+, DO– Rise Time (10% to 90%)		–	7.0	ns
t_{DOTF}	DO+, DO– Fall Time (90% to 10%)		–	7.0	ns
t_{DORM}	DO+, DO– Rise and Fall Time Mismatch		–	1.0	ns
t_{DOETD}	DO± End of Transmission		275	375	ns
t_{PWODI}	DI Pulse Width Accept/Reject Threshold	$\|V_{IN}\|>\|V_{ASQ}\|$ (Note 2)	15	45	ns
t_{PWKDI}	DI Pulse Width Not to Turn-off Internal Carrier Sense	$\|V_{IN}\|>\|V_{ASQ}\|$ (Note 3)	136	200	ns
t_{PWOCI}	CI Pulse Width Accept/Reject Threshold	$\|V_{IN}\|>\|V_{ASQ}\|$ (Note 4)	10	26	ns
t_{PWKCI}	CI Pulse Width Not to Turn-off Threshold	$\|V_{IN}\|>\|V_{ASQ}\|$ (Note 5)	75	160	ns
t_{CITR}	CI Rise Time (In Reverse Mode)		–	7.0	ns
t_{CITF}	CI Fall Time (In Reverse Mode)		–	7.0	ns
t_{CIRM}	CI+, CI– Rise and Fall Time Mismatch (AUI in Reverse Mode)		–	1.0	ns
Expansion Bus Timing					
t_{CLKHRL}	CLK HIGH to $\overline{SELO}$ Driven LOW	C_L = 50 pF	15	30	ns
t_{CLKHRH}	CLK HIGH to $\overline{SELO}$ Driven HIGH	C_L = 50 pF	15	30	ns
t_{CLKHDR}	CLK HIGH to DAT/JAM Driven	C_L = 100 pF	14	30	ns
t_{CLKHDZ}	CLK HIGH to DAT/JAM Not Driven	C_L = 100 pF	14	30	ns
t_{DJSET}	DAT/JAM Setup Time to CLK		10	–	ns
t_{DJHOLD}	DAT/JAM Hold Time from CLK		9	–	ns
t_{CASET}	$\overline{COL}$/$\overline{ACK}$ Setup Time to CLK		10	–	ns
t_{CAHLD}	$\overline{COL}$/$\overline{ACK}$ Hold Time from CLK		9	–	ns
$t_{SCLKHLD}$	SI, SCLK Hold Time		50	–	ns

SWITCHING CHARACTERISTICS (continued)

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
Twisted Pair Port Timing					
t_{TXTD}	CLK Rising Edge to TXD± Transition Delay		–	50	ns
t_{TETD}	Transmit End of Transmission		250	375	ns
t_{PWKRD}	RXD Pulse Width Maintain/Turn-off Threshold	$\|V_{IN}\|>\|V_{THS}\|$ (Note 6)	136	200	ns
t_{PERLP}	Idle Signal Period		8	24	ms
t_{PWLP}	Idle Link Test Pulse Width		75	120	ns
Control Port Timing					
t_{SCLK}	SCLK Clock Period		100	–	ns
t_{SCLKH}	SCLK Clock HIGH		30	–	ns
t_{SCLKL}	SCLK Clock LOW		30	–	ns
t_{SCLKR}	SCLK Clock Rise Time		–	10	ns
t_{SCLKF}	SCLK Clock Fall Time		–	10	ns
t_{SISET}	SI Input Setup Time to SCLK Rising Edge		10	–	ns
t_{SIHLD}	SI Input Hold Time from SCLK Rising Edge		10	–	ns
t_{SODLY}	SO Output Delay from SCLK Rising Edge	C_L = 100 pF	–	40	ns

Notes:

1. *Parameter not tested.*
2. *DI pulses narrower than t_{PWODI} (min) will be rejected; pulses wider than t_{PWODI} (max) will turn internal DI carrier sense on.*
3. *DI pulses narrower than t_{PWKDI} (min) will maintain internal DI carrier on; pulses wider than t_{PWKDI} (max) will turn internal DI carrier sense off.*
4. *CI pulses narrower than t_{PWOCI} (min) will be rejected; pulses wider than t_{PWOCI} (max) will turn internal CI carrier sense on.*
5. *CI pulses narrower than t_{PWKCI} (min) will maintain internal CI carrier on; pulses wider than t_{PWKCI} (max) will turn internal CI carrier sense off.*
6. *RXD pulses narrower than t_{PWKRD} (min) will maintain internal RXD carrier sense on; a pulse wider than t_{PWKRD} (max) will turn RXD carrier sense off.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING WAVEFORMS

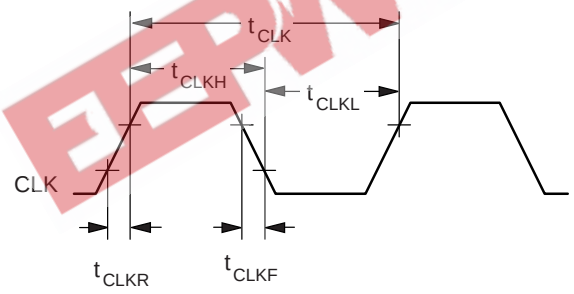


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Figure 14. Clock Timing

SWITCHING WAVEFORMS (continued)

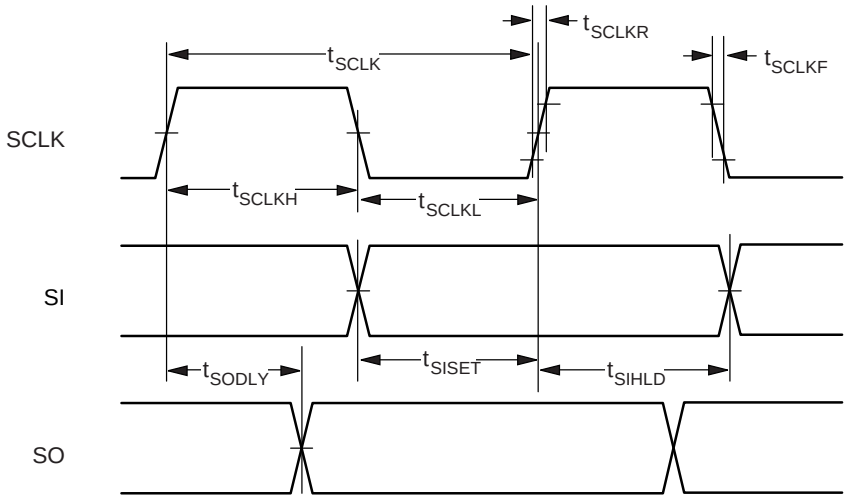
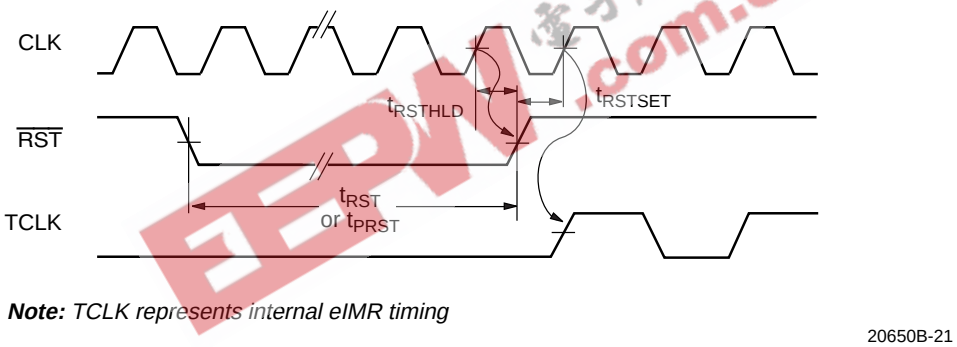


Figure 15. Control Port Timing



Note: *TCLK represents internal eIMR timing*

Figure 16. Reset Timing

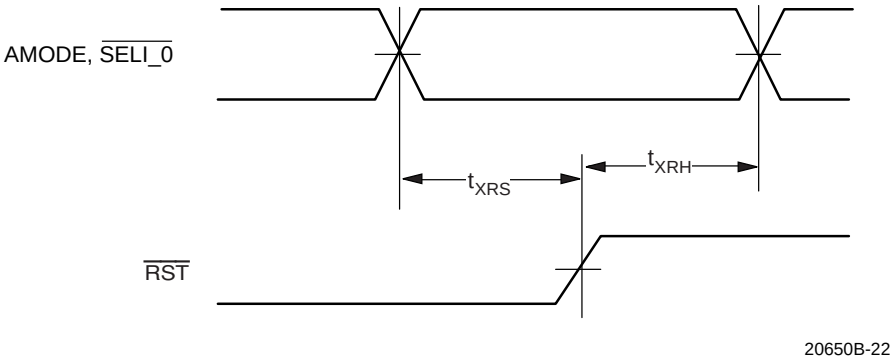
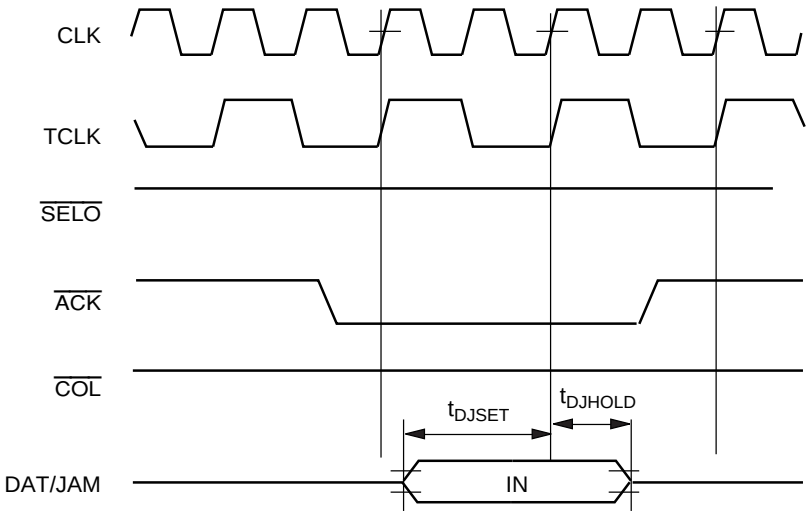


Figure 17. Mode Initialization

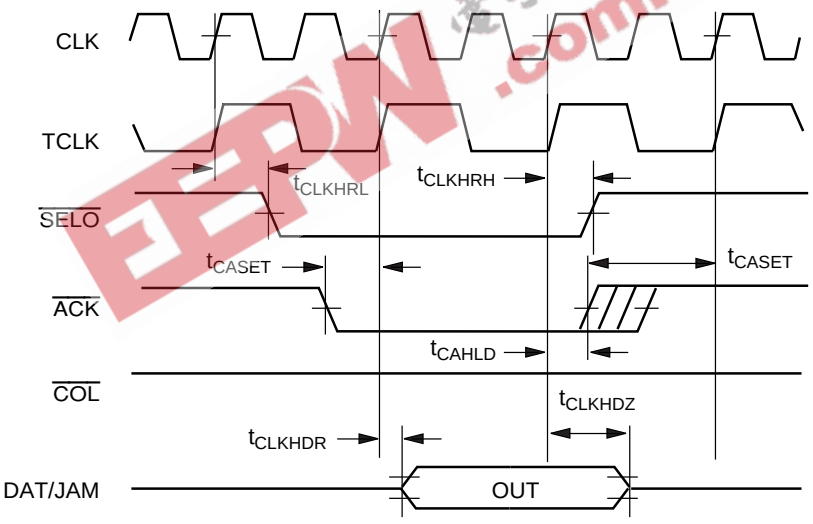
SWITCHING WAVEFORMS (continued)



Note: *TCLK represents internal eIMR timing*

20650B-23

Figure 18. Expansion Bus Input Timing

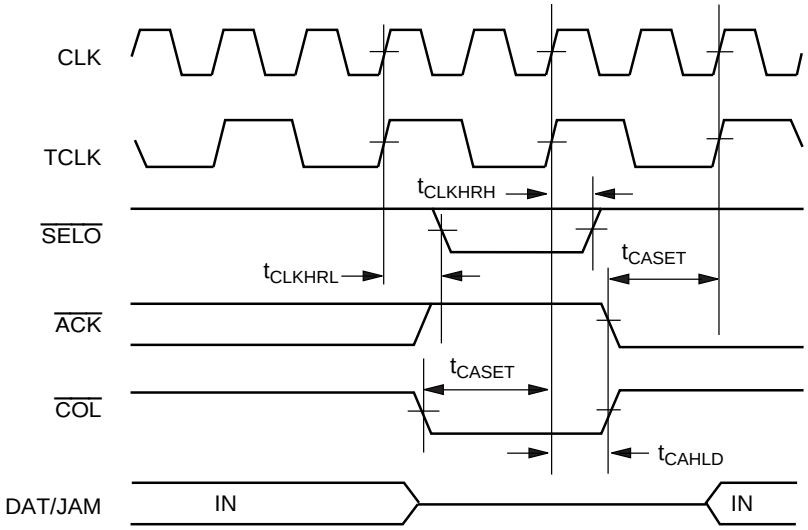


Note: *TCLK represents internal eIMR timing*

20650B-24

Figure 19. Expansion Bus Output Timing

SWITCHING WAVEFORMS (continued)



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Note: *TCLK represents internal eIMR timing*

Figure 20. Expansion Bus Collision Timing

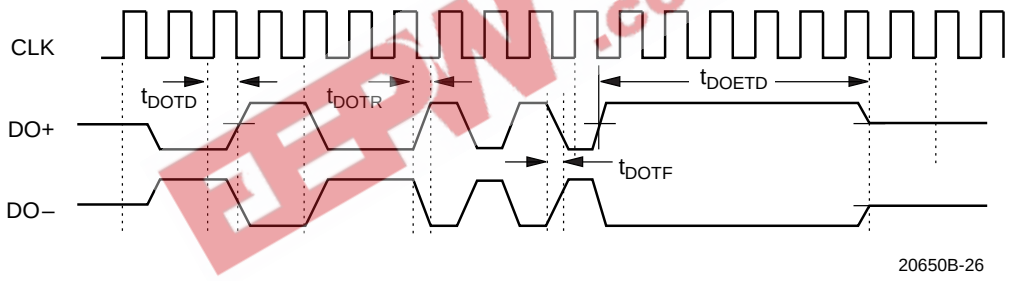

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Figure 21. AUI Timing Diagram

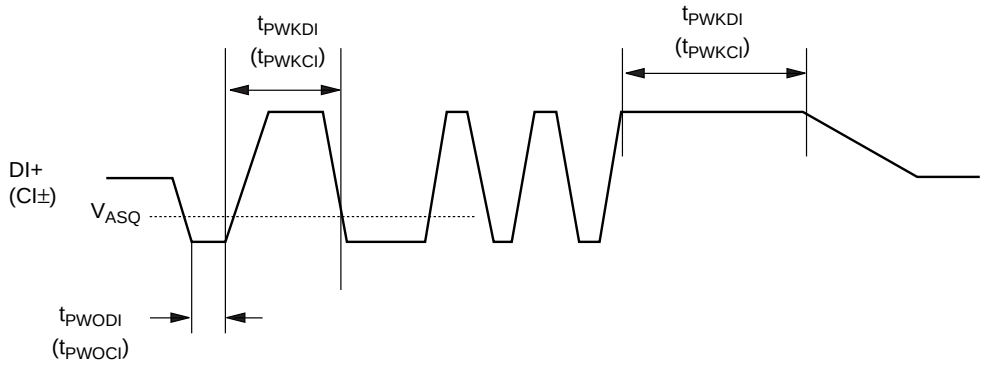

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Figure 22. AUI Receive Diagram

SWITCHING WAVEFORMS (continued)

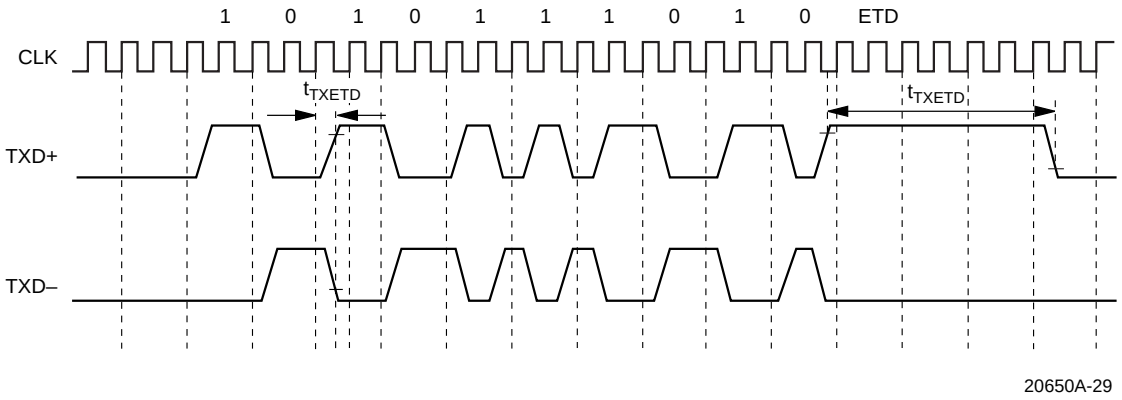


Figure 23. TP Ports Output Timing Diagram

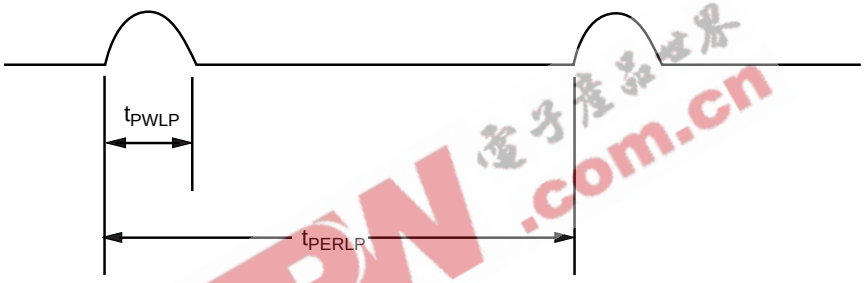


Figure 24. TP Idle Link Test Pulse

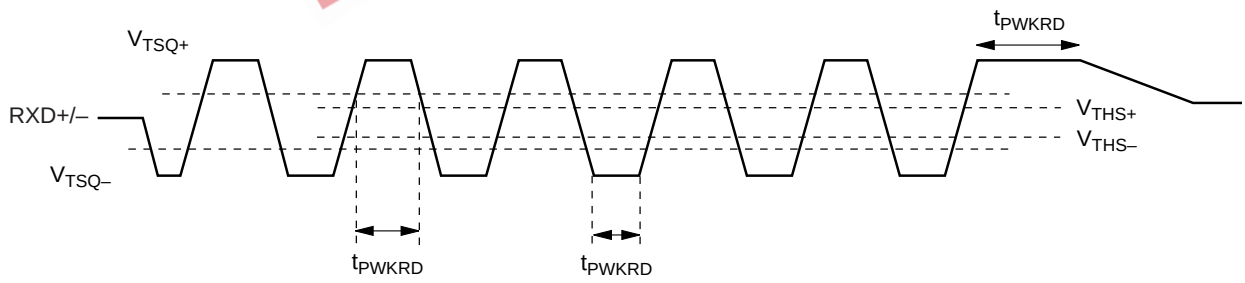


Figure 25. TP Receive Timing Diagram

SWITCHING TEST CIRCUIT

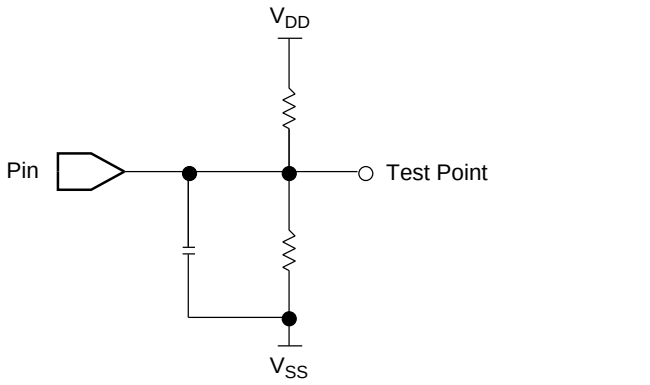
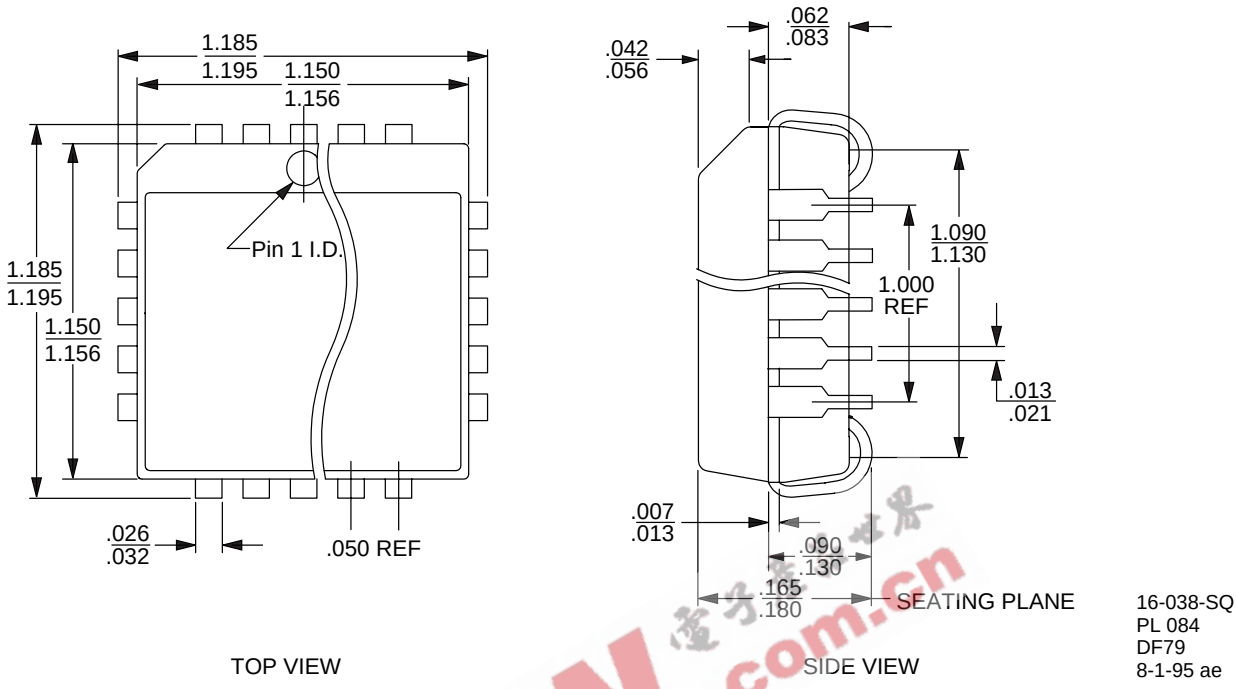


Figure 26. Switching Test Circuit

PHYSICAL DIMENSIONS

PL 084

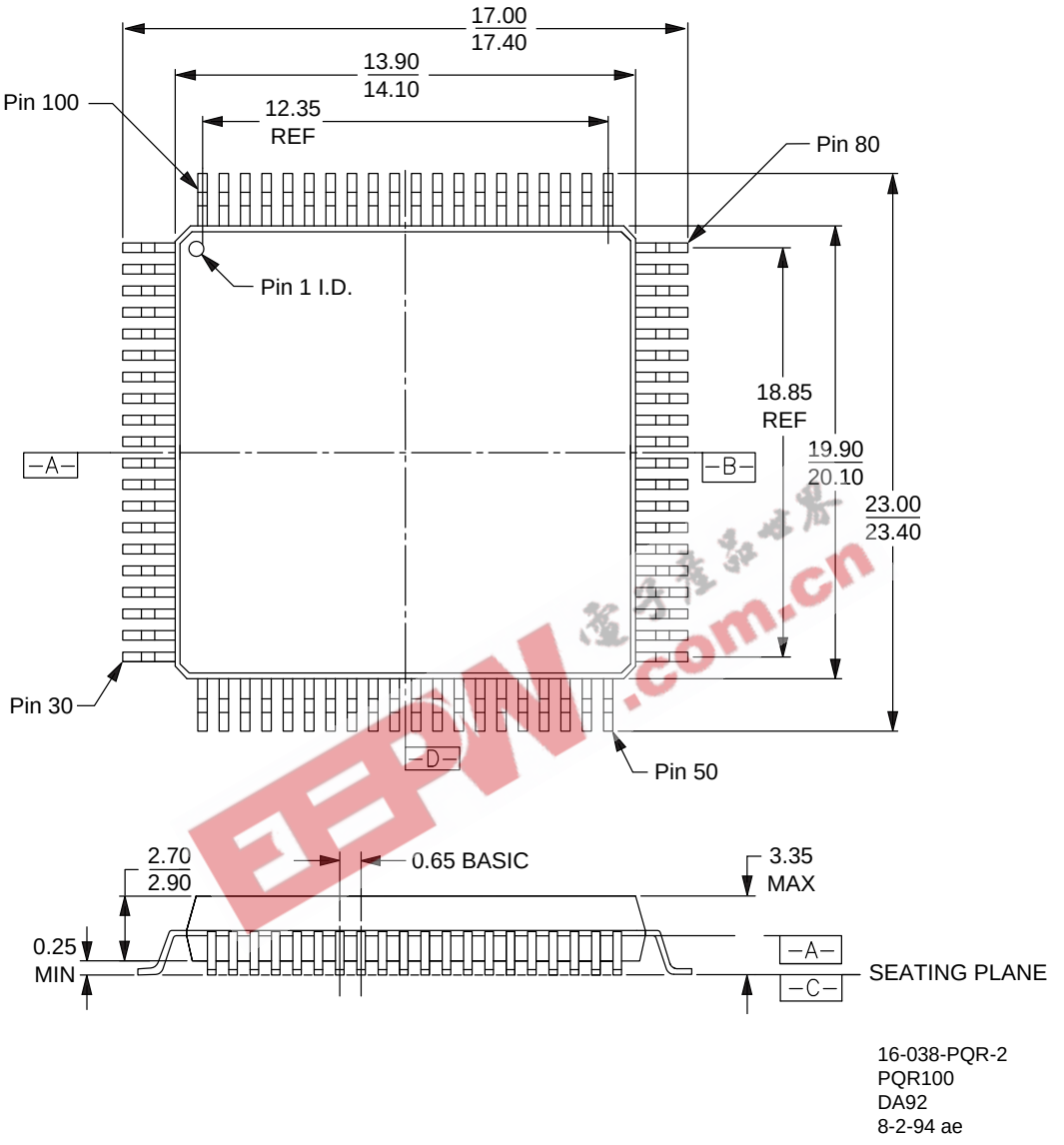
84-Pin Plastic LCC (measured in inches)



PHYSICAL DIMENSIONS

PQR100

100-Pin Plastic Quad Flat Pack



16-038-PQR-2
PQR100
DA92
8-2-94 ae