

# Am9150

## 1024x4 High-Speed Static R/W RAM

### DISTINCTIVE CHARACTERISTICS

- 1024 x 4 organization
- High speed – 20 ns Max. access time
- Separate data inputs and outputs
- Memory reset function
- High density SLIM 24-pin 300-MIL package
- Three-state output buffers
- Single +5 V power supply  $\pm 10\%$
- Low-power version

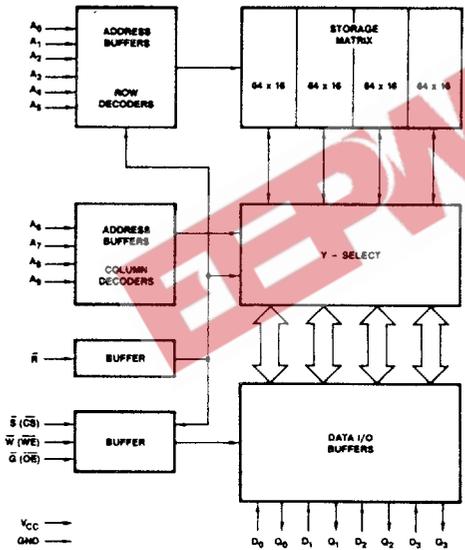
### GENERAL DESCRIPTION

The Am9150 is a high-performance, static, n-channel, read/write, random-access memory organized as 1024 x 4. It features single 5 V supply operation, TTL-compatible input and output levels, and separate input and output pins for improved system performance and ease of use.

The Am9150 also incorporates a reset feature which will reset the entire contents of the memory to logical LOW in two cycle times by controlling  $\bar{R}$  (RESET) and  $\bar{S}$  (CS).

The Am9150 has four control signals  $\bar{R}$ ,  $\bar{S}$ ,  $\bar{W}$  and  $\bar{G}$ . The  $\bar{S}$  input controls read, write and reset operations of the device and provides for easy selection of an individual device when the outputs are tied together. The  $\bar{W}$  (WE) input controls the normal read and write operations, and the  $\bar{G}$  ( $\bar{OE}$ ) controls the state of the outputs.

### BLOCK DIAGRAM



BD005261

### MODE SELECT TABLE

Inputs				Outputs	Mode
$\bar{S}$	$\bar{W}$	$\bar{G}$	$\bar{R}$		
H	X	X	X	Hi-Z	Not Selected
L	H	X	L	Hi-Z	Reset*
L	L	X	H	Hi-Z	Write
L	H	L	H	$Q_0 - Q_3$	Read
L	X	H	H	Hi-Z.	Output Disable

H = High

L = Low

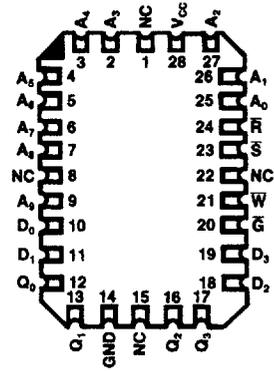
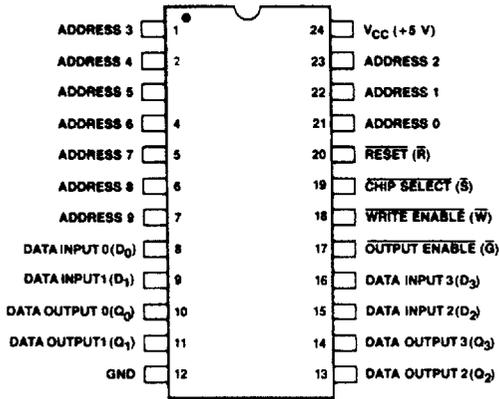
X = Don't Care

\*See Reset cycle description.

### PRODUCT SELECTOR GUIDE

Part Number	Am9150-20	Am9150-25	Am9150-35	Am9150-45	Am91L50-25	Am91L50-35	Am91L50-45
Maximum Access Time (ns)	20	25	35	45	25	35	45
$I_{CC}$ Max. (mA)	0°C to +70°C	180	180	180	130	130	130
	-55°C to +125°C	N/A	180	180	180	N/A	N/A

## CONNECTION DIAGRAMS Top View

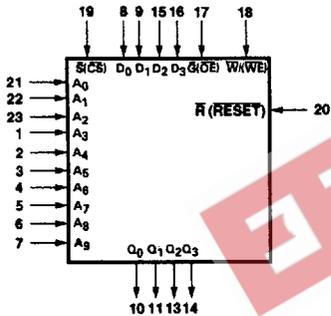


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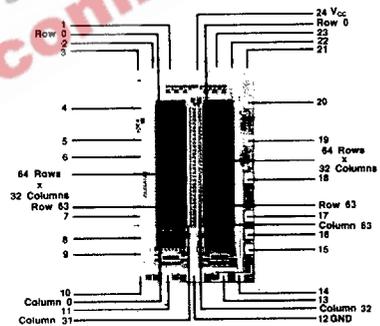
Note: Pin 1 is marked for orientation.

### LOGIC SYMBOL (DIP ONLY)



LS001821

### METALLIZATION AND PAD LAYOUT



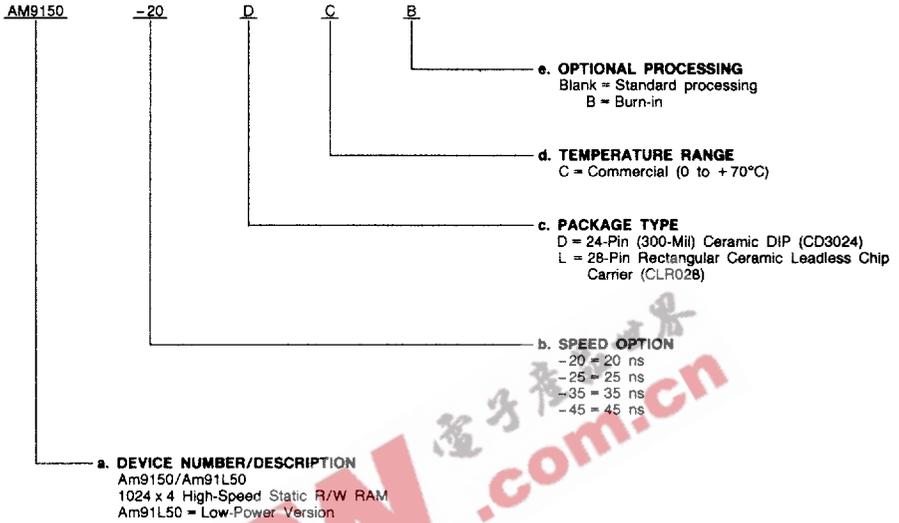
Die Size: 0.93" x 0.163"

## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Package Type**
- d. **Temperature Range**
- e. **Optional Processing**



Valid Combinations	
AM9150-20	DC, DCB, LC, LCB
AM9150-25	
AM9150-35	
AM9150-45	
AM91L50-25	
AM91L50-35	
AM91L50-45	

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult MSIS sales department to confirm availability of specific valid combinations, and to obtain additional data on MSIS's standard military grade products.

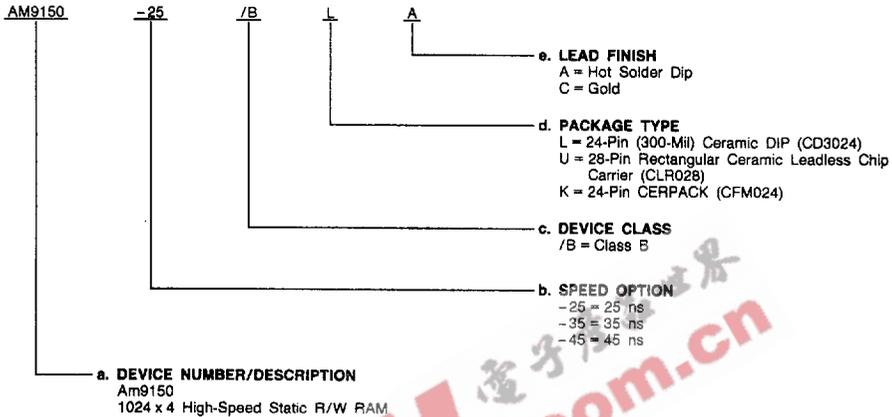
## MILITARY ORDERING INFORMATION

### APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Device Class**
- d. **Package Type**
- e. **Lead Finish**

### APL Products



Valid Combinations	
AM9150-25	/BLA
AM9150-35	/BUC
AM9150-45	/BKA

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult MSIS sales department to confirm availability of specific valid combinations, and to obtain additional data on MSIS's standard military grade products.

### Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

## PIN DESCRIPTION

### A<sub>0</sub> - A<sub>9</sub> Address (Inputs)

The 10 address inputs select one of the 1024 4-bit words in the RAM.

### $\bar{S}$ Chip Select (Input; Active LOW)

An active-LOW input which selects the device for operation. When  $\bar{S}$  is HIGH, the device is deselected and the outputs will be in a high-impedance state.

### $\bar{W}$ Write Enable (Input; Active LOW)

$\bar{W}$  controls read and write operations. When  $\bar{W}$  is HIGH and  $\bar{G}$  is LOW, data will be present at the data outputs. When  $\bar{W}$  is LOW, data present on the data inputs will be written into the selected memory location. The data outputs will be in a high-impedance state.

### $\bar{R}$ RESET (Input; Active LOW)

An active-Low pulse on  $\bar{R}$  while A<sub>0</sub> - A<sub>9</sub> are stable,  $\bar{S}$  is LOW, and  $\bar{W}$  and  $\bar{G}$  are HIGH resets the whole memory.

### $\bar{G}$ Output Enable (Input; Active LOW)

$\bar{G}$  controls the state of the data outputs in conjunction with  $\bar{S}$  and  $\bar{W}$ .

### D<sub>0</sub> - D<sub>3</sub> Data Input

Data inputs to the RAM.

### Q<sub>0</sub> - Q<sub>3</sub> Data Output

Data outputs from the RAM. The data outputs will be in a high-impedance state when either  $\bar{S}$  or  $\bar{G}$  are HIGH or  $\bar{W}$  is LOW.

### V<sub>CC</sub> Power Supply +5 Volts

### V<sub>SS</sub> Ground

## ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature .....	-65 to +150°C
Ambient Temperature with Power Applied .....	-55 to +125°C
Supply Voltage with Respect to Ground .....	-0.5 V to +7.0 V
Signal Voltages with Respect to Ground .....	-3.5 V to +7.0 V
Power Dissipation (Package Limitation) .....	1.2 W
DC Output Current .....	20 mA

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

## OPERATING RANGES (Note 2)

Commercial (C) Devices	
Ambient Temperature (T <sub>A</sub> ) .....	0 to +70°C
Supply Voltage (V <sub>CC</sub> ) .....	+5.0 V ±10%
Military (M) Devices	
Ambient Temperature (T <sub>A</sub> ) .....	-55 to +125°C
Supply Voltage (V <sub>CC</sub> ) .....	+5.0 V ±10%

Operating ranges define those limits between which the functionality of the device is guaranteed.

**DC CHARACTERISTICS** over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions	Am9150		Am91L50		Unit
			Min.	Max.	Min.	Max.	
I <sub>OH</sub>	Output HIGH Current	V <sub>OH</sub> = 2.4 V	-4		-4		mA
I <sub>OL</sub>	Output LOW Current	V <sub>OL</sub> = 0.4 V	12		12		mA
V <sub>IH</sub>	Input HIGH Voltage		2.2	6.0	2.2	6.0	V
V <sub>IL</sub>	Input LOW Voltage		-2.5	0.8	-2.5	0.8	V
I <sub>Ix</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-10	10	-10	10	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> Output Disabled	-10	10	-10	10	μA
C <sub>I</sub>	Input Capacitance	Test Frequency = 1.0 MHz T <sub>A</sub> = 25°C, All Pins at 0 V.		5		5	pF
C <sub>O</sub>	Output Capacitance	V <sub>CC</sub> = 5 V (Note 8)		7		7	
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	Max V <sub>CC</sub> $\bar{S}$ ≤ V <sub>IL</sub> Output Open	COM'L. MIL.	180 180		130 N/A	mA
I <sub>OS</sub>	Output Short Circuit Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> (Notes 7, 8)	±50	±300	±50	±300	mA

- Notes: 1. Absolute Maximum Ratings are intended for user guidelines and are not tested.  
 2. For test and correlation purposes, ambient temperature is defined as the "instant-ON" case temperature.  
 3. Test conditions assume signal transition times of 10 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30 pF load capacitance. Output timing reference is 1.5 V.  
 4. The internal write time of the memory is defined by the overlap of  $\bar{S}$  LOW and  $\bar{W}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing is referenced to the rising edge of the signal that terminates the write.  $\bar{R}$  must be HIGH.  
 5. Transition is measured at 1.5 V on the inputs to V<sub>OH</sub> - 500 mV and V<sub>OL</sub> + 500 mV on the outputs using the load shown in B. under Switching Test Circuits.  
 6.  $\bar{W}$  and  $\bar{R}$  are HIGH for read cycle.  
 7. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.  
 8. This parameter is not tested, but guaranteed by characterization.

**SWITCHING CHARACTERISTICS** over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

No.	Parameter Symbol		Parameter Description	Am9150-20		Am9150-25 Am91L50-25		Am9150-35 Am91L50-35		Am9150-45 Am91L50-45		Unit
	Standard	Alternate		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>												
1	TAVAV	t <sub>RC</sub>	Read Cycle Time (Note 6)	20		25		35		45		ns
2	TAVQV	t <sub>AA</sub>	Address Access Time		20		25		35		45	ns
3	TSLQV	t <sub>ACS</sub>	Chip Select Access Time		10		15		20		25	ns
4	TGLQV	t <sub>OE</sub>	Output Enable Access Time		10		15		20		25	ns
5	TSLOX	t <sub>CLZ</sub>	Chip Select LOW to Output in Low-Z (Notes 5, 8)	0		0		0		0		ns
6	TSHQZ	t <sub>CHZ</sub>	Chip Select HIGH to Output in Hi-Z (Notes 5, 8)	0	15	0	20	0	25	0	30	ns
7	TGLQX	t <sub>OLZ</sub>	Output Enable LOW to Output in Low-Z (Note 5, 8)	0		0		0		0		ns
8	TGHQZ	t <sub>OHZ</sub>	Output Enable HIGH to Output in Hi-Z (Notes 5, 8)	0	15	0	20	0	25	0	30	ns
9	TAXQX	t <sub>OH</sub>	Output Hold after Address Change	COM'L.	3		3		3		3	ns
				MIL.	1		1		1		1	
<b>WRITE CYCLE</b>												
10	TAVAV	t <sub>WC</sub>	Write Cycle Time (Note 4)	20		25		35		45		ns
11	TSLWH	t <sub>CW</sub>	Chip Select LOW to Write Enable HIGH	10		15		20		30		ns
12	TAVWH	t <sub>AW</sub>	Address Valid to End of Write	15		20		30		40		ns
13	TAVWL	t <sub>AS</sub>	Address Valid to Beginning of Write	5		5		5		5		ns
14	TWLWH	t <sub>WP</sub>	Write Pulse Width	10		15		20		30		ns
15	TWHAX	t <sub>WR</sub>	Address Hold after End of Write	5		5		5		5		ns
16	TDVWH	t <sub>DW</sub>	Data in Valid to Write Enable HIGH	10		15		20		30		ns
17	TWHDX	t <sub>DH</sub>	Data Hold after End of Write	5		5		5		5		ns
18	TWLQZ	t <sub>WZ</sub>	Write Enable LOW to Output in Hi-Z (Notes 5, 8)	0	15	0	20	0	25	0	30	ns
19	TWHQX	t <sub>OW</sub>	Write Enable HIGH to Output in Low-Z (Notes 5, 8)	0		0		0		0		ns
<b>RESET CYCLE</b>												
20	TAVAV	t <sub>RRC</sub>	Reset Cycle Time	40		50		70		90		ns
21	TAVRL	t <sub>RSA</sub>	Address Valid to Beginning of Reset	0		0		0		0		ns
22	TWHRL	t <sub>RSW</sub>	Write Enable HIGH to Beginning of Reset	0		0		0		0		ns
23	TSLRL	t <sub>RSCS</sub>	Chip Select LOW to Beginning of Reset	0		0		0		0		ns
24	TRLRH	t <sub>RP</sub>	Reset Pulse Width	20		20		30		40		ns
25	TRHSX	t <sub>RHCS</sub>	Chip Select Hold after End of Reset	0		0		0		0		ns
26	TRHWL	t <sub>RHW</sub>	Write Enable Hold after End of Reset	20		30		40		50		ns
27	TRHAX	t <sub>RHA</sub>	Address Hold after End of Reset	20		30		40		50		ns
28	TRLQZ	t <sub>RHZ</sub>	Reset LOW to Output in Hi-Z (Notes 5, 8)	0	15	0	20	0	25	0	35	ns
29	TRHQX	t <sub>RLZ</sub>	Reset HIGH to Output in Low-Z (Notes 5, 8)	0		0		0		0		ns

Notes: See notes following DC Characteristics table.

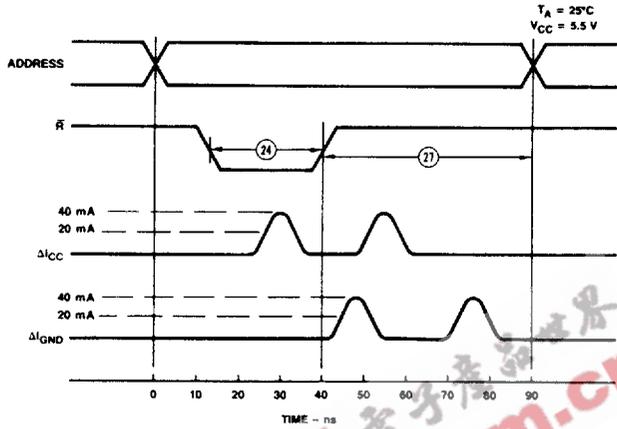
## RESET CYCLE

The reset cycle is initiated by  $\bar{R}$  going LOW for a time  $\geq t_{RP}$ , and is terminated by holding  $\bar{R}$  HIGH for a time  $\geq t_{RHA}$ . The addresses to the device must be stable during the RESET cycle time. The entire contents of the RAM will be reset to ZERO regardless of the address chosen during the cycle. The

control  $\bar{S}$  must be  $\leq V_{IL}$  maximum, and  $\bar{W}$  must be  $\geq V_{IH}$  minimum and it is recommended that  $\bar{G}$  be  $\geq V_{IH}$  minimum.

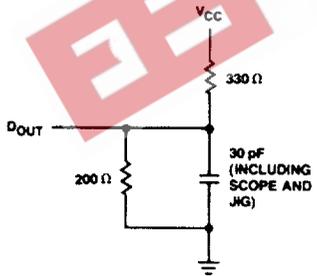
The reset cycle is normally associated with current spikes, both at  $V_{CC}$  and GND as shown in the graph. To attenuate the current spikes, an external bypass capacitor (high frequency, 0.1  $\mu\text{F}$ ) for each Am9150 socket is recommended.

Typical  $I_{CC}$  and  $I_{GND}$  During a Reset Cycle



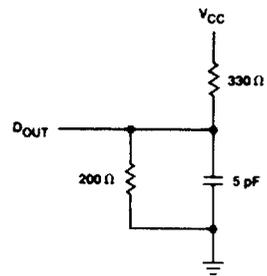
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## SWITCHING TEST CIRCUITS



TC002350

A.



TC002360

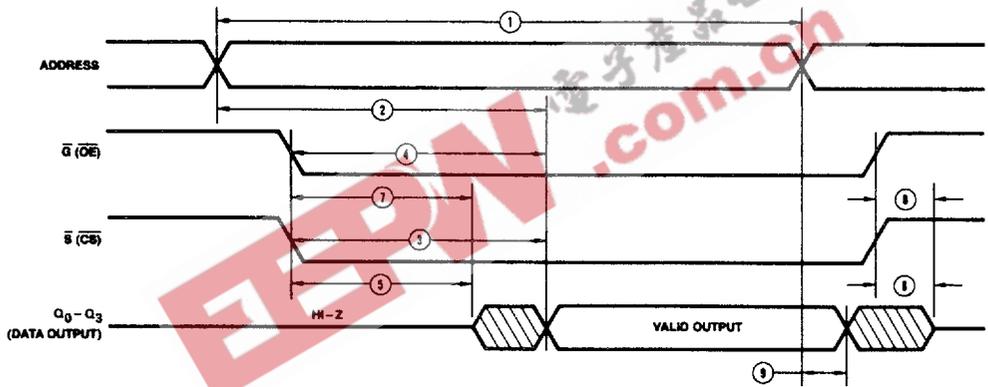
B.

## SWITCHING WAVEFORMS

### KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

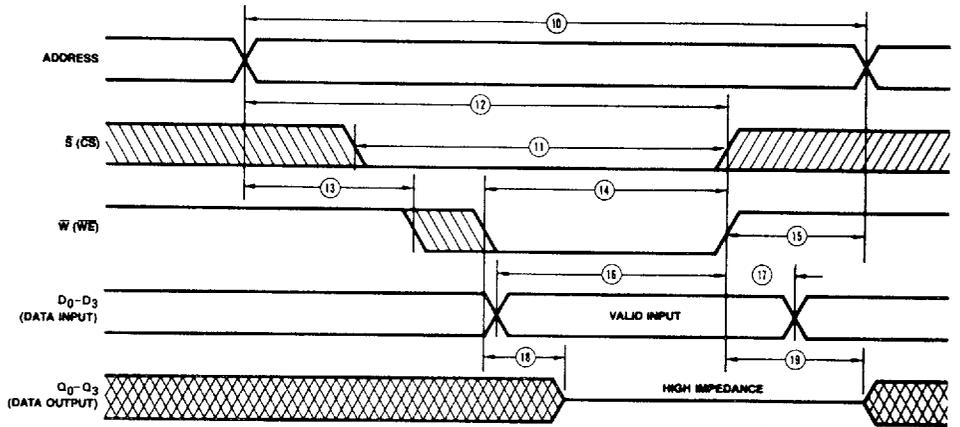
KS000010



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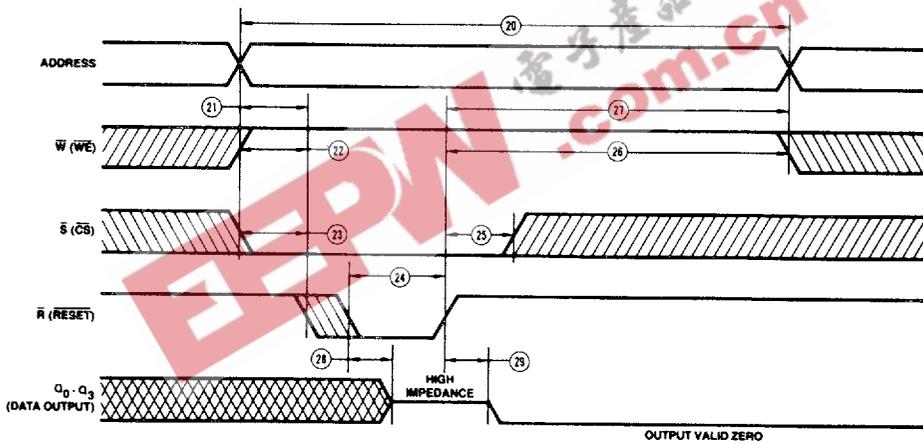
**Read Cycle**

## SWITCHING WAVEFORMS (Cont'd.)



WF009900

Write Cycle



WF009910

Reset Cycle