Am79213/Am79C203/031

Advanced Subscriber Line Interface Circuit (ASLIC™) Device
Advanced Subscriber Line Audio-Processing Circuit (ASLAC™) Device

DISTINCTIVE CHARACTERISTICS

- **Performs all of the functions of a codec-filter**
- **Single channel architecture**
- **Performs Battery-feed, Ring-trip, Signaling, Coding, Hybrid and Test (BORSCHT) functions**
- **Single hardware design meets multiple country requirements through software programming**
- **Standard microprocessor interface**
- **Industry standard PCM interface with full-time slot assignment**
- **Monitor of two-wire interface voltage and current for subscriber line diagnostics**
- **Low idle power per line**
- **On-hook transmission**
- **Only battery and +5 V supplies needed**
- **Exceeds LSSGR and CCITT central office requirements**
- **Off-hook and ground-key detectors with programmable thresholds**
- **Programmable line feed characteristics independent of battery voltage**
- **Built-in voice path test modes**
- **Analog and digital hybrid balance capability**
- **Adaptive hybrid balance capability**
- **Linear power feed with power management and thermal shutdown features**
- **Abrupt and smooth polarity reversal**
- **Power-cross detection in Ringing and Non-ringing states**
- **Software programmable**
  - — DC loop feed characteristics and current limit
  - — Loop supervision detection thresholds
  - — Off-hook detect debounce interval
  - — Two-wire AC impedance
  - — Transhybrid balance
  - — Transmit and receive gains
  - — Equalization
  - — Digital I/O pins
  - — A-law/μ-law selection
- **Linear data available on PCM ports for custom compression and expansion**
- **Compatible with inexpensive protection networks. Accommodates low tolerance fuse resistors while maintaining longitudinal balance to Bellcore specifications.**
- **Power/Service Denial state**
- **Small physical size**
- **Integrated ring trip function**
- **Four relay drivers with built-in energy absorption zener diodes**
- **Synchronized ring relay operation: zero volts ac on, zero current off**
- **Software enabled Normal or Automatic Ring-Trip state**
- **On-chip 12 kHz and 16 kHz metering generation with on and off meter pulse shaping**
- **Supports loop-start and ground-start signaling**
- **0°C to +70°C commercial operation guaranteed by production testing**
- **–40°C to +85°C temperature range operation available**

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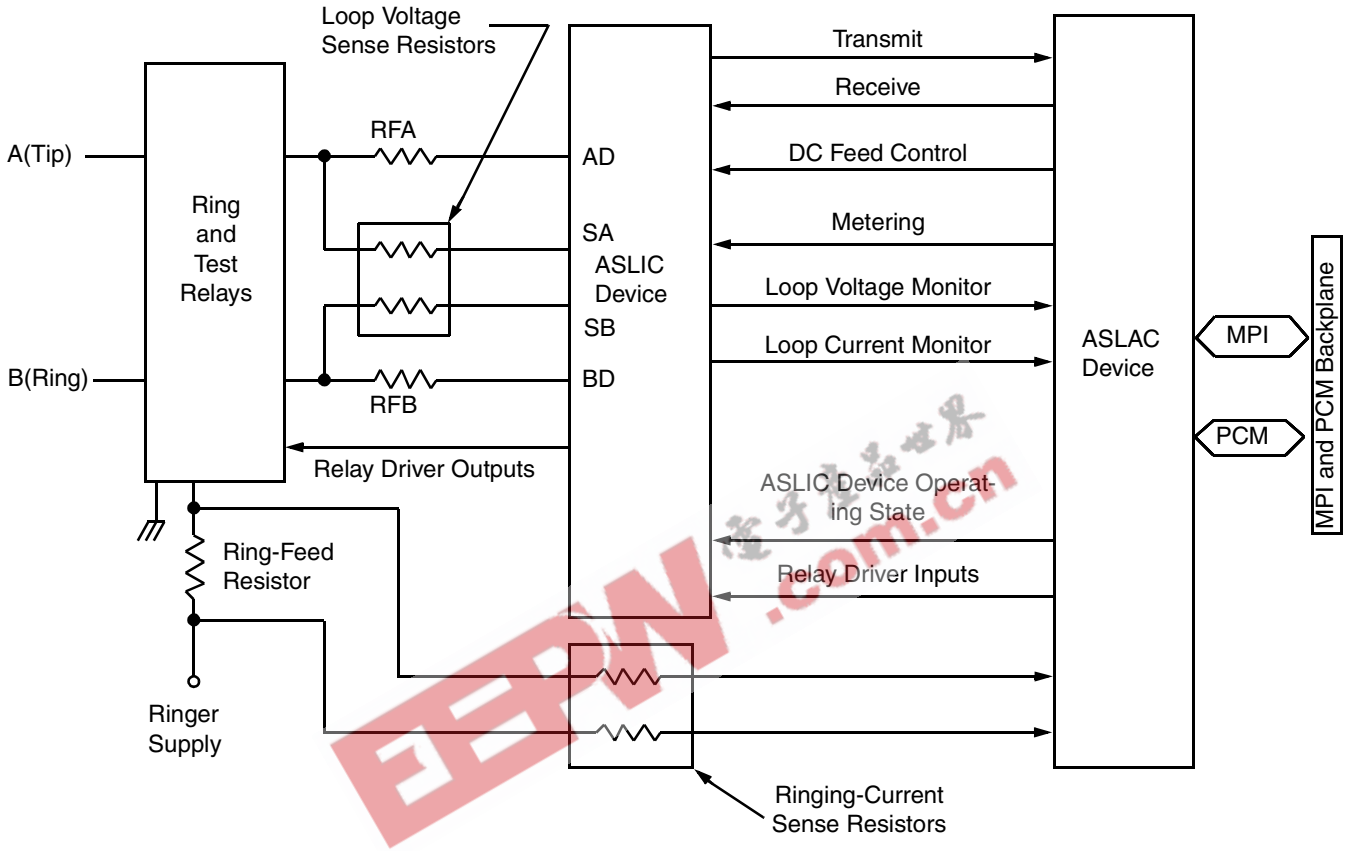
The Am79213/Am79C203/031 Advanced Subscriber Line Interface chip set implements a universal telephone line interface function. This enables the design of a single, low cost, high performance, fully software programmable line interface card for multiple country applications world wide. All AC, DC, and signaling parameters are fully programmable via the microprocessor interface. Additionally, the ASLIC device and ASLAC device have integrated self test and line test capabilities to resolve faults to the line or line circuit. The integrated test capability is crucial for remote applications where dedicated test hardware is not cost effective. The Technical Reference, PID 21325A is recommended to be used with this document.

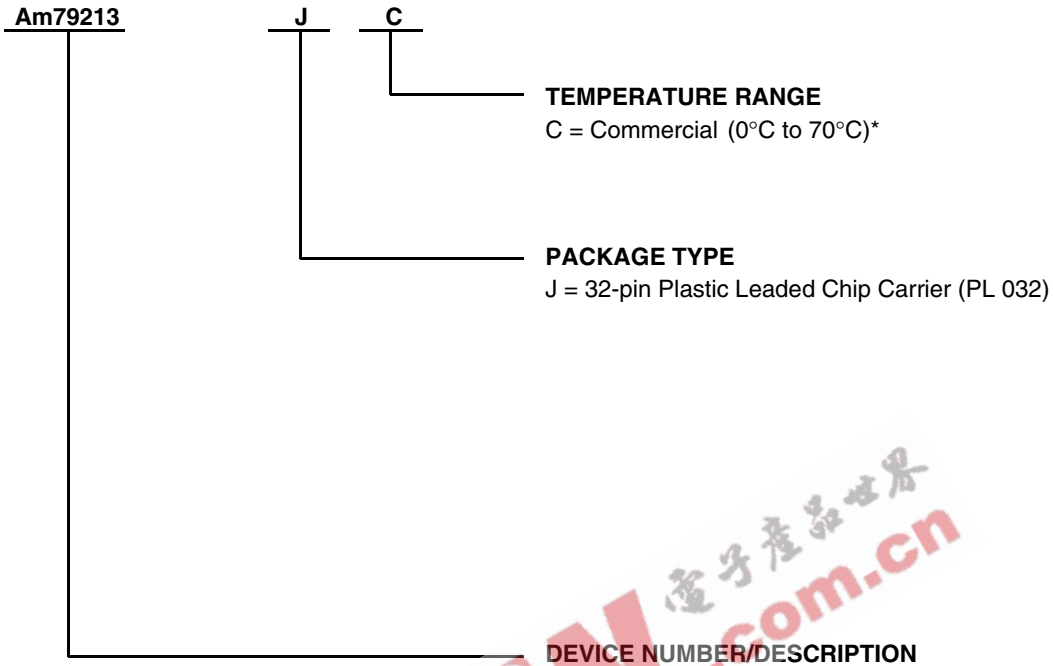
LINECARD BLOCK DIAGRAM



ORDERING INFORMATION

ASLIC Device

Must order Am79C203 or Am79C2031 with the device below.



Valid Combinations	
Am79213	JC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Legerity sales office to confirm availability of specific valid combinations and to check on newly released combinations.

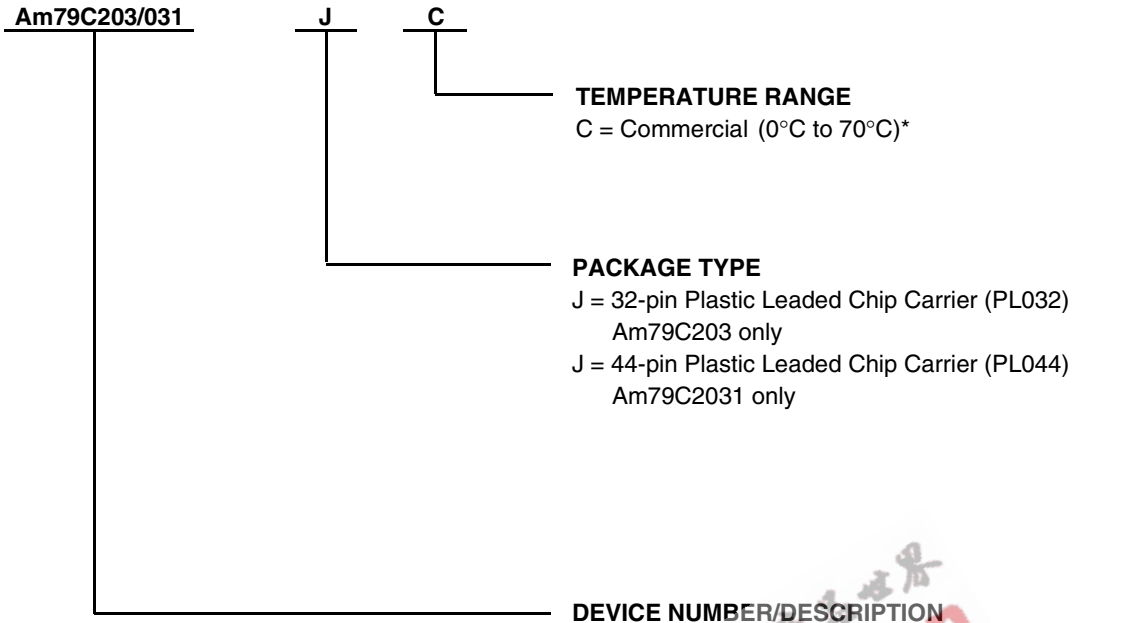
Note:

** Functionality of the device from 0°C to +70°C is guaranteed by production testing. Performance from –40°C to +85°C is guaranteed by characterization and periodic sampling of production units.*

ORDERING INFORMATION (continued)

ASLAC Device

Must order Am79213 with the device below.



Valid Combinations	
Am79C203	JC
Am79C2031	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Legerity sales office to confirm availability of specific valid combinations and to check on newly released combinations.

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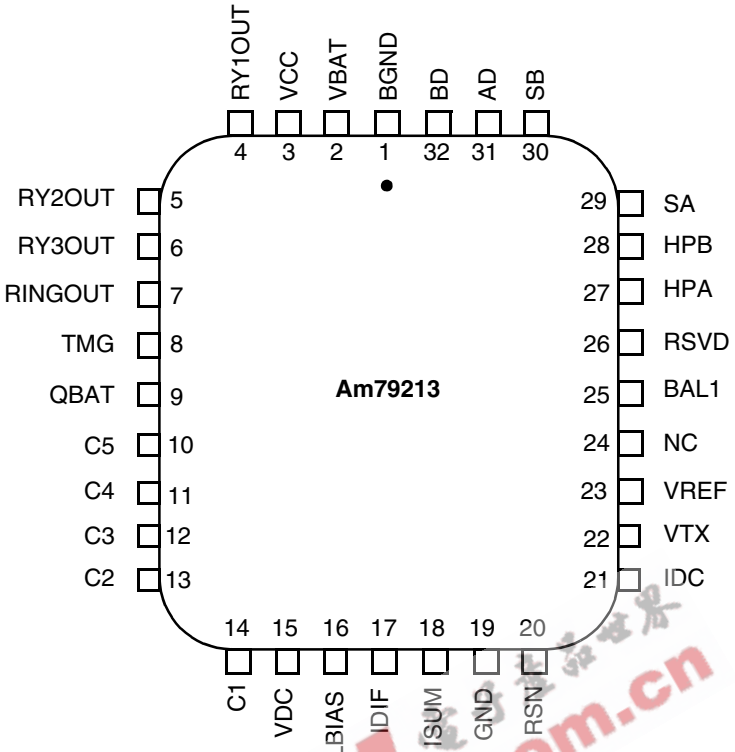
** Functionality of the device from 0°C to +70°C is guaranteed by production testing. Performance from –40°C to +85°C is guaranteed by characterization and periodic sampling of production units.*

CONNECTION DIAGRAMS

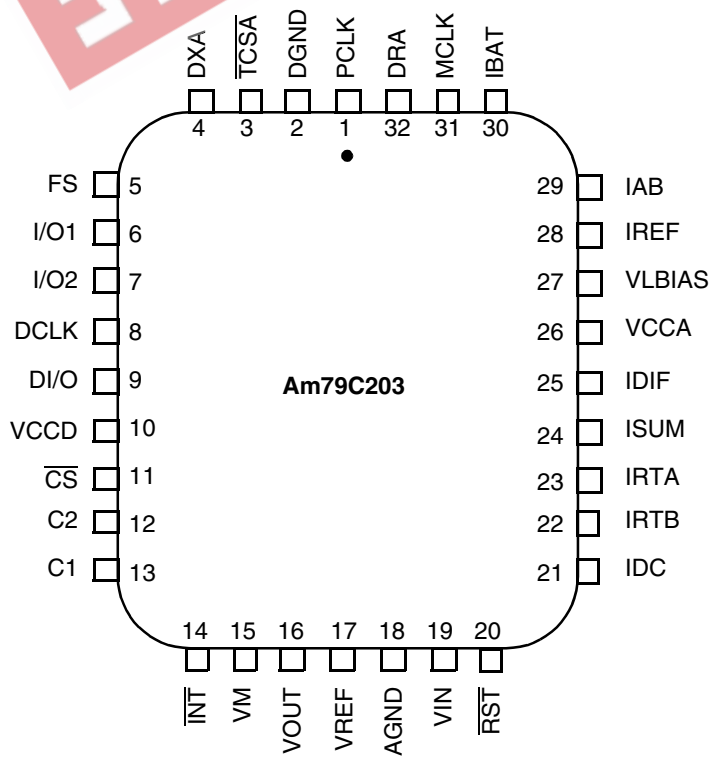
Top View

32-Pin PLCC



Notes:

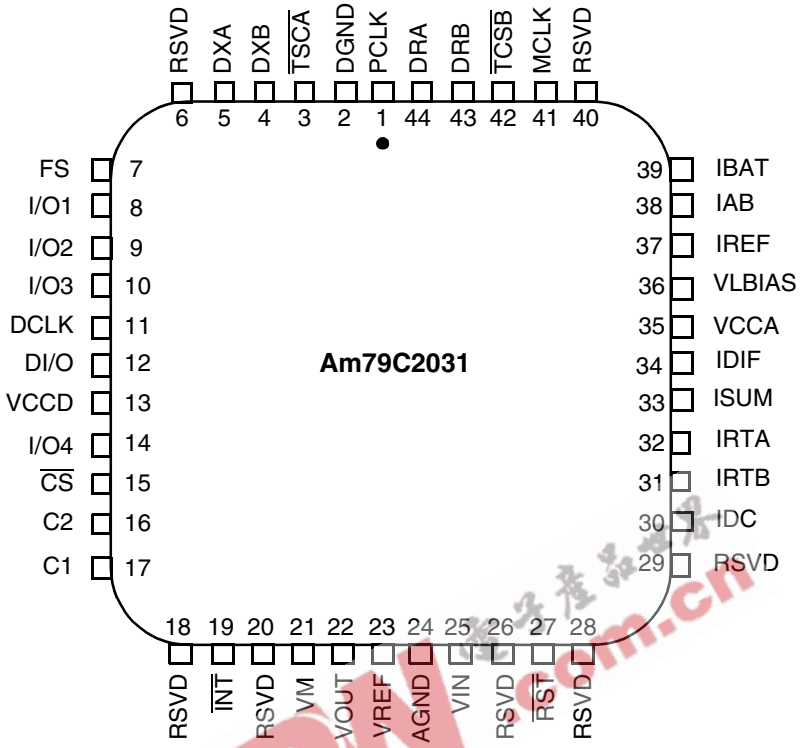
1. *RSVD = Reserved. Do not connect to this pin.*
2. *NC = No Connect*



CONNECTION DIAGRAMS (continued)

Top View

44-Pin PLCC



Note:

RSVD = Reserved. Do not connect to this pin.

PIN DESCRIPTIONS

ASLIC Device

Pin Names	Type	Description
AD, BD	Output	A and B Line Drivers. These pins provide the currents to the A and B leads of the subscriber loop.
BAL1	Input	Pre-balance. This pin receives voltages that are added to the VTX output signal. They can be used to cancel out the metering echo in the transmit path.
BGND	Gnd	Battery Ground. This pin connects to the ground return for Central Office or talk battery.
C2–C1	Input	ASLIC Device Control. These ternary logic input pins control the operating state of the ASLIC device.
C5–C3	Input	Test Relay Control. These are control inputs for the test relay drivers in the ASLIC device. A logic Low turns on the relay driver and activates the relay. C3 controls RY1OUT, C4 controls RY2OUT, and C5 controls RY3OUT.
GND	Gnd	Analog and digital ground return for VCC.
HPA, HPB	Capacitor	High-Pass Filter Capacitor Connections. These pins connect to CHP, the external high-pass filter capacitor that isolates the DC control loop from the voice transmission path.
IDC	Input	DC Loop Control Current. The DC loop current control line from the ASLAC device is connected to this pin. An internal resistance is provided between the IDC pin and RSN. An external noise filter capacitor should be connected between this pin and VREF.
IDIF	Output	A – B Leg Current. The current at this pin is proportional to the difference of the currents flowing out of the AD pin and into the BD pin of the ASLIC device.
ISUM	Output	A + B Leg Current. The current at this pin is proportional to the absolute value of the sum of the currents flowing out of the AD pin and into the BD pin of the ASLIC device.
QBAT	Power	Quiet Battery Voltage. The QBAT pin is connected to the substrate.
RINGOUT, RY1OUT, RY2OUT, RY3OUT	Output	Relay Drivers. These are open collector, high current relay driver outputs with emitters internally connected to BGND. To absorb the inductive pulse from the relay coils, an internal Zener diode is connected between the collector of each driver and BGND.
RSN	Input	Receive Summing Node. The metallic current (both AC and DC) between AD and BD is equal to ASLIC device current gain, K1, times the current into this pin. Networks that program receive gain and two-wire impedance connect to this node. This input is nominally at VREF potential.
RSVD	Input	Reserved. This is used during Legerity testing. In the application, this pin must be floating.
SA, SB	Input	A and B Lead Voltage Sense. These pins sense the voltages on the line side of the fuse resistors at the A and B leads. External sense resistors, RSA and RSB, are required to protect these pins from lightning or power cross conditions.
TMG	Thermal	Thermal Management. A resistor connected from this pin to VBAT reduces the on-chip power dissipation by absorbing excess power from the ASLIC device for short-loop conditions.
VBAT	Power	Battery Voltage. This pin supplies battery voltage to the line drivers.
VCC	Power	Power Supply. This is the positive supply for low voltage analog and digital circuits in the ASLIC device.
VDC	Output	DC Loop VoltageThe voltage on this output is referenced to VREF and is proportional to the negative absolute value of the DC subscriber loop voltage between A and B. This voltage is a fraction (β) of the voltage between HPA and HPB. This pin connects to the IAB pin on the ASLAC device through external resistor RAB. A voltage that is significantly more positive than VREF on the VDC pin indicates that the ASLIC device is in thermal shutdown.

Pin Names	Type	Description
VLBIAS	Input	Longitudinal Offset Voltage. The input to this pin is the offset reference voltage for the ASLIC device longitudinal control loop.
VREF	Input	Analog Reference. This voltage is provided by the ASLAC device and is used by the ASLIC device for internal reference purposes. All analog input and output signals interfacing to the ASLAC device are referenced to this pin. Nominally set to 2.1 V.
VTX	Output	Four-Wire Transmit Signal. The voltage between this pin and VREF is a scaled version of the AC component of the voltage sensed between the SA and SB pins. One end of the two-wire input impedance programming network connects to VTX. The voltage at VTX swings positive and negative about VREF.

ASLAC Device

Pin Names	Type	Description
AGND	Gnd	Analog (Quiet) Ground. VREF is referenced to this ground.
C2–C1	Output	ASLIC Device Control. These ternary logic output pins are dedicated to controlling the operating state of the ASLIC device. The levels of these outputs are logic High, logic Low, and high impedance.
CS	Input, Active Low	Chip Select. The chip select input (active Low) enables the device so commands and data can be written to or read from it. If chip select is held Low for 16 or more DCLK cycles (independent of MCLK or PCLK), a hardware reset is executed at the time chip select returns to logic 1.
DCLK	Input	Data Clock. The data clock input shifts data into or out of the microprocessor interface of the ASLAC device. The maximum clock rate is 4.096 MHz.
DGND	Gnd	Digital Ground. Digital ground return.
DI/O	Input/Output	Data Input/Output. Control data is serially written into and read out of the ASLAC device via the DI/O pin, with the most significant bit first. The data clock (DCLK) determines the data rate. DI/O is high impedance except when data is being transmitted from the ASLAC device under control of $\overline{CS}$.
DRA, DRB	Input	Receive PCM Data. Receive PCM data is received serially on either the DRA or DRB port, with port selection under user program control. Data is received, most significant bit first, in 8-bit PCM or 16-bit linear 2's complement bursts every 125 µs at the PCLK rate. The receive port is unaffected by the setting of the SMODE bit. (DRB – 44-pin PLCC only.)
DXA, DXB	Output	Transmit PCM Data. Transmit PCM data is transmitted serially through either the DXA or DXB port, with port selection under user control. The transmission data output is available every 125 µs and is shifted out, most significant bit first, in 8-bit PCM or 16-bit linear 2's complement bursts at the PCLK rate. DXA/B are high impedance between bursts and while the device is in the Inactive state. For signaling register operation on the PCM highway, see the SMODE description. (DXB – 44-pin PLCC only.)
FS	Input	Frame Sync. The frame sync signal is an 8 kHz pulse that identifies the beginning of a frame. The ASLAC device references individual time slots with respect to this input, which must be synchronized to PCLK.
IAB	Input	Loop Voltage Sense. The IAB pin is a current summing node referenced to VREF. An external resistor (RAB) is connected between this pin and the VDC pin of the ASLIC device, In normal operation, current flows out of this pin. When the ASLIC device is in thermal shutdown, current will be forced into this pin.
IBAT	Input	Battery Voltage Sense. The IBAT pin is a current summing node referenced to AGND and receives a current that is proportional to the system battery voltage. A sense resistor/capacitor network is connected between the QBAT pin of the ASLIC device and the IBAT pin.

Pin Names	Type	Description
IDC	Output	DC Loop Control Current. The IDC output supplies a current to the ASLIC device for proportional control of the DC loop current flowing through the subscriber loop.
IDIF	Input	Longitudinal Sense. IDIF is a current input pin fed by the IDIF pin of the ASLIC device. The current in this pin is used by the ASLAC device for supervisory and diagnostic functions. The IDIF pin has an internal input resistance so an external longitudinal noise filter capacitor can be connected.
$\overline{INT}$	Output, Active Low	Interrupt. A logic 0 on this pin indicates one or more of the bits in the signaling register has changed states. An interrupt will be generated when activity is sensed on any signal in the Signaling Register not masked by the Mask Register. Once an unmasked activity is sensed, the $\overline{INT}$ output will be driven Low and held at that state until cleared. See the description of configuration register 6 for operation.
I/O_1, I/O_2, I/O_3, I/O_4	Input/output	Control Ports. These control lines are TTL compatible and each can be programmed as an input or an output. When programmed as inputs, they can monitor external, TTL compatible logic circuits. When programmed as outputs, they can control an external logic device or they can be connected to pin C3, C4, or C5 of the ASLIC device to control test relay drivers RY1OUT, RY2OUT and RY3OUT (I/O_3, I/O_4, 44-pin PLCC version only). In the Output mode, these pins are controlled by the I/O_1, I/O_2, I/O_3, and I/O_4 bits in the Channel Control Register, MPI Command 17.
IREF	Reference	Current Reference. An external resistor (RREF) connected between this pin and analog ground generates an accurate on-chip reference current. This current is used by the ASLAC device in its DC Feed and loop-supervision circuits.
IRTA, IRTB	Inputs	Ring Trip Sense. These pins are current summing nodes referenced to VREF. They provide terminations for external resistors RSR1 and RSR2, which sense the voltages on both sides of the ringing feed resistor connected to the ring bus. To determine the ringing current in the loop, the ASLAC device senses the difference between the currents in these pins.
ISUM	Input	Metallic Sense. ISUM is a current input pin and is fed by the ISUM pin of the ASLIC device. The absolute value of the current in this pin is used by the ASLAC device for supervisory and diagnostic functions.
MCLK	Input	Master Clock. The master clock is used to operate the digital signal processor. MCLK can be 2.048 MHz, 4.096 MHz or 8.192 MHz. MCLK may be asynchronous to PCLK. Upon initialization, the MCLK input is disabled and relevant circuitry is driven by a connection to PCLK. The MCLK connection may be reestablished under user control.
PCLK	Input	PCM Clock. The PCM clock determines the rate at which PCM data is serially shifted into or out of the PCM ports. PCLK is an integer multiple of the frame sync frequency. The maximum clock frequency is 8.192 MHz and the minimum clock frequency is 128 kHz for companded data. The minimum clock frequency for linear or companded data plus signaling data is 256 kHz. The PCLK clock may be asynchronous to MCLK if the initial connection state is disabled under user control.
$\overline{RST}$	Input, Active Low	Reset. A logic 0 on this pin resets the ASLAC device to initial default conditions. It is equivalent to a hardware reset command. A signal less than 100 ns should not cause a reset. To ensure proper reset, the minimum length of a reset pulse is 50 µs.
$\overline{TSCA}$, $\overline{TSCB}$	Open Drain Outputs	Time Slot Control. The time slot control outputs are open drain (requiring an external pull-up resistor to VCCD) and are normally inactive (high impedance). $\overline{TSCA}$ is active (Low) when PCM data is present on DXA, and $\overline{TSCB}$ is active (Low) when PCM data is present on DXB. ($\overline{TSCB}$ and DRB – 44-pin PLCC only.)
VCCA	Power	Analog Power Supply. VCCA is internally connected to substrate near the analog I/O section.
VCCD	Power	Digital Power Supply. VCCD is internally connected to substrate near the digital section.
VIN	Input	Analog Input. The analog output (VTX) from the ASLIC device is applied to the ASLAC device transmit path input, VIN. The signal is sampled, processed, encoded, and transmitted on the PCM Highway.

Pin Names	Type	Description
VLBIAS	Output	Longitudinal Reference. VLBIAS is programmed by VOFF and supplies the longitudinal reference voltage for the longitudinal control loop to the ASLIC device.
VM	Output	12/16 kHz Metering Signal. For 12/16 kHz teletax, an internally generated and shaped 12 or 16 kHz sine wave metering pulse is output from this pin.
VOUT	Output	Analog Output. The voice data from the received PCM channel (timeslot) is digitally processed and converted to an analog signal which is present on the VOUT pin of the ASLAC device.
VREF	Output	Analog Reference. This pin provides a voltage reference to be used as the analog zero level reference on the ASLIC device.

ASLIC/ASLAC DEVICES FUNCTIONAL DESCRIPTION

The ASLIC/ASLAC devices chip set integrates all functions of the subscriber line. The chip set comprises an ASLIC device and an ASLAC device. The set provides two basic functions: 1) the ASLIC device, a high-voltage, bipolar device that drives the subscriber line, maintains longitudinal balance, and senses line conditions; and 2) the ASLAC device, a low-voltage CMOS device that combines CODEC, DC Feed control, and line supervision. A complete schematic of a linecard using the ASLIC/ASLAC devices chip set is shown in the Figure 7.

The ASLIC device uses reliable, bipolar technology to provide the power necessary to drive a wide variety of subscriber lines. It can be programmed by the ASLAC device to operate in eight different states that control Power Consumption and Signaling states. This enables full control over the subscriber loop. The ASLIC device is customized to be used exclusively with the ASLAC device, providing a two-chip universal line interface. The ASLIC device requires only a +5 V power supply and a negative battery supply for its operation.

The ASLIC device implements a linear loop current feeding method with the enhancement of thermal management to limit the amount of power dissipated on the ASLIC device by dissipating excess power in an external resistor.

The ASLAC device is a high-performance, CMOS CODEC/filter device with additional digital filters and circuits that allow software control of transmission, DC Feed, and supervision.

Advanced CMOS technology makes the ASLAC device an economical device that has both the functionality and the low power consumption required by linecard designers to maximize linecard density at minimum cost.

When used with an ASLIC device, the ASLAC device provides a complete software-configurable solution to linecard functions. In addition, the ASLIC/ASLAC devices chip set provides system-level solutions for loop supervisory functions and metering. In total, the ASLIC/ASLAC devices chip set provides a programmable solution that can satisfy worldwide linecard requirements by software configuration.

All software-programmed coefficients and DC Feed parameters are easily calculated with the AmSLAC3™ software. This software is provided free of charge and runs on an IBM-compatible PC. It allows the designer to enter a description of system requirements, then the software returns the necessary coefficients and the predicted system response.

The ASLAC device uses the industry standard microprocessor (MPI) and PCM interfaces to communicate with the system and for interfacing to the 64 kilobit per second voice network.

The ASLIC device interface unit inside the ASLAC device processes information regarding line voltages, loop currents, and battery voltage levels. These inputs allow the ASLAC device to place several key ASLIC device performance parameters under programmable supervision.

The main functions that can be observed and/or controlled through the ASLAC device control interface are:

- DC Feed characteristics
- Ground-key detection
- Off-hook detection
- Metering signal
- Longitudinal operating point
- Subscriber line voltage and currents
- Ring trip
- Abrupt and smooth battery polarity reversal

To accomplish these functions, the ASLAC device collects the following information from the ASLIC device and the Central Office system:

- The sum and difference of the currents in each loop leg, ISUM, and IDIF
- Currents proportional to the:
  - voltage across the loop (IAB)
  - battery voltage (IBAT)
  - ringing current in the loop (IRTA – IRTB)

The outputs supplied by the ASLAC device are then:

- A current proportional to the desired DC loop current (IDC)
- A voltage proportional to the desired longitudinal offset voltage (VLBIAS)
- A 12/16 kHz metering signal (appears on VM for 12/16 kHz teletax)

The ASLAC device performs the CODEC and filter functions associated with the four-wire section of the subscriber line circuitry in a digital switch. These functions involve converting an analog voice signal into digital PCM samples and converting digital PCM samples back into an analog signal. During conversion, digital filters are used to band-limit the voice signals.

The user-programmable filters set the receive and transmit gain, perform the transhybrid balancing function, permit adjustment of the two-wire termination impedance, and provide frequency response adjustment (equalization) of the receive and transmit paths. Adaptive transhybrid balancing is also included.

The PCM data can be either 8-bit companded A-law code, 8-bit companded µ-law code, or 16-bit linear code. Voice data is transmitted and received via the PCM highway; control information is written to and read from the ASLAC/ASLIC devices chip set over the microprocessor interface.

Besides the CODEC functions, the ASLAC device provides all the sensing, feedback, and clocking necessary to completely control ASLIC device functions with programmable parameters. The line status is continuously available in the ASLAC Device Signaling Register, which is continuously available via the MPI interface, or on the PCM highway via a user-programmable mode. A programmable interrupt provides added flexibility in monitoring line status. System-level parameters under programmable control include active and disable loop-current limits, feed resistance, and apparent battery-feed voltage. The longitudinal operating point is programmable to optimize the ASLIC device signal swing capability.

The ASLAC device provides signals at 12 or 16 kHz for metering functions. The frequency and level of these signals are programmable.

The ASLAC device provides extensive loop supervision capability, including off-hook, ring-trip, and ground-key detection. Detection thresholds for these functions are programmable. A programmable debounce timer is available that eliminates false detection due to contact bounce. For subscriber line diagnostics, AC and DC line conditions can be monitored using special test modes. Results are read using the MPI commands.

ELECTRICAL REQUIREMENTS

Power Dissipation

Loop resistance = 0 to ∞ (not including fuse resistors), 2 x 50 Ω fuse resistors, VBAT = QBAT = –48 V, VCC = +5 V. For power dissipation measurements, DC Feed conditions are programmed as follows:

VAPP (apparent voltage) = 50.2 V

ILA (Active state current limit) = 42.3 mA

ILD (Disable state current limit) = 21.2 mA

RFD (feed resistance) = 807 Ω

VAS (anti-sat activate voltage) = 8.2 V

N2 (anti-sat feed resistance factor) = 2

VOFF (longitudinal offset voltage) = 6 V

RTMG (thermal management resistor) = 1200 Ω

RREF (reference current setting resistor) = 7.87 kΩ

Table 1. Power Dissipation

Description	Test Conditions	Min	Typ	Max	Unit
ASLIC device power dissipation Normal polarity	On-hook Disconnect		30	70	mW
	On-hook Standby		50	105	
	On-hook Disable		120	215	
	On-hook Active		330	450	
	Off-hook Active R_L = 294 Ω		850	1200	
	Off-hook Disable R_L = 600 Ω		800	950	
ASLAC device power dissipation MCLK, PCLK = 2.048 MHz	ASLAC device activated		85	110	
	ASLAC device inactive, MPI Standby state command issued		22	25	
ASLAC device power dissipation MCLK, PCLK > 2.048 MHz	ASLAC device activated		95	120	
	ASLAC device inactive, MPI Standby state command issued		23	26	

Thermal Resistance

The junction-to-air thermal resistance of the ASLIC device in a 32-pin PLCC package will be less than 45°C/W.

The junction-to-air thermal resistance of the ASLAC device in a 32-pin PLCC package will be less than 45°C/W.

The junction-to-air thermal resistance of the ASLAC device in a 44-pin PLCC package will be less than 44°C/W.

ABSOLUTE MAXIMUM ELECTRICAL AND THERMAL RATINGS

ASLIC Device

Storage temperature ..... $-55°C \le T_A \le +150°C$

Ambient temperature, under bias ..... $-40°C \le T_A \le +85°C$

Ambient relative humidity (noncondensing) ..... 5% to 100%

V_{CC} with respect to AGND/DGND ..... –0.4 V to +7 V

V_{BAT}, Q_{BAT} with respect to BGND ..... +0.4 V to –75 V

V_{CC} with respect to V_{BAT}, Q_{BAT} ..... +80 V

BGND with respect to AGND/DGND ..... –0.5 V to +0.5 V

Voltage on relay outputs ..... +7 V

AD or BD to BGND:
- Continuous ..... –75 V to +1 V
- 10 ms (f = 0.1 Hz) ..... –75 V to +5 V
- 1 µs (f = 0.1 Hz) ..... –90 V to +10 V
- 250 ns (f = 0.1 Hz) ..... –120 V to +15 V

Current into SA or SB: 10 µs rise to Ipeak; 1000 µs fall to 0.5 Ipeak; 2000 µs fall to I = 0 ..... Ipeak = ±5 mA

Current into SA or SB: 2 µs rise to Ipeak; 10 µs fall to 0.5 Ipeak; 20 µs fall to I = 0 ..... Ipeak = ±12.5 mA

Current through AD or BD ..... ±150 mA

C5–C1 to DGND or AGND ..... –0.4 V to V_{CC} + 0.4 V

Maximum power dissipation, T_A = 70°C ..... 1.67 W

Note: *Thermal limiting circuitry on chip will shut down the circuit at a junction temperature of about 160°C. The device should never be exposed to this temperature. Operation above 145°C junction temperature may degrade device reliability. See the SLIC Packaging Considerations for more information.*

ASLAC Device

Storage temperature ..... $-60°C \le T_A \le +125°C$

Ambient temperature, under bias ..... $-40°C \le T_A \le +85°C$

Ambient relative humidity (noncondensing) ..... 5% to 100%

V_{CCA}, V_{CCD} with respect to DGND ..... –0.4 V to +6 V

V_{CCA} with respect to V_{CCD} ..... ±0.4 V

V_{IN} with respect to DGND ..... –0.4 V to V_{CCA} + 0.4 V

AGND ..... DGND ±0.4 V

Latch up immunity (any pin) ..... ±100 mA

Any other pin with respect to DGND ..... –0.4 V to V_{CC} + 0.4 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Environmental

Ambient temperature ..... 0°C to +70°C Commercial*

Ambient relative humidity ..... 15% to 85%

ASLIC Device

V_{CC} ..... +5 V ± 5%

V_{BAT}, Q_{BAT} ..... –18 V to –70 V

BGND with respect to GND ..... –100 mV to +100 mV

Load resistance on V_{TX} to ground ..... 10 kΩ min

ASLAC Device

Supplies V_{CCA}, V_{CCD} ..... +5 V ± 5%

DGND ..... 0 V

AGND ..... DGND ± 50 mV

Operating ranges define those limits over which the functionality of the device is guaranteed by production testing.

** Functionality of the device from 0°C to +70°C is guaranteed by production testing. Performance from –40°C to +85°C is guaranteed by characterization and periodic sampling of production units.*

PERFORMANCE SPECIFICATIONS

(See note 1) T_A = 0°C to 70°C unless otherwise noted.

Table 2. ASLIC Device DC Specifications

No.	Item	Condition	Min	Typ	Max	Unit	Note
1	2-wire loop voltage	Standby state, R_L = 1 MΩ	Q_{BAT} – 1.8	Q_{BAT} – 1.1	Q_{BAT} – 0.5	V	4
		Active state, $RL_{AD–BD}$ = 600 Ω IRSN = 140 µA	19.51	21.1	22.68		
		Disable state, $RL_{AD–BD}$ = 600 Ω IRSN = 80 µA	11.34	12.19	13.04		
2	Feed resistance per leg at pins AD and BD	Standby state	130	250	375	Ω	
3	ISUM current	Standby state, R_L = 1930 Ω	44.6	56		µA	
	IDIF current	Standby state A to Q_{BAT} B to ground	 35.4 43.4				
4	Ternary input voltage boundaries for C2–C1 pins. Mid-level input source must be high impedance or 3-state						
	Low boundary				0.8	V	
	High boundary		V_{CC} – 1				
	Logic inputs C2–C1 Input High current			–80	200	µA	
	Input Low current			90	200		
	3-state voltage	I_{C1} = I_{C2} = 1 µA	0.8		3.5	V	4
5	Logic inputs C5–C3 Input High voltage		2.0				
	Input Low voltage				0.8		
	Input High current		–200		40	µA	
	Input Low current		–400		40		
6	V_{TX} output offset	BAL1 pin open	–50		+50	mV	
7	V_{REF} input voltage	IREF = ±1 mA	2.0	2.1	2.2	V	
8	β, Ratio of V_{DC} to loop voltage: $\beta = \frac{\lvert VDC\rvert - VREF}{\lvert VSA - VSB\rvert}$	Tj < 145°C, V_{DC} is referenced to V_{REF}, 35.7 kΩ resistor connected from V_{DC} to V_{REF}. VSA – VSB = 40 V.	0.0253	0.0242	0.0232	V/V	
9	Thermal shutdown threshold voltage output on V_{DC}	I_{VDC} = 20 µA	4.2	V_{CC} – 0.4		V	4
10	Gain from VLBIAS pin to AD or BD pin		5.58	6.0	6.42	V/V	
11	Input resistance to AGND, VLBIAS pin	VLBIAS = 3 V	20	33.3		kΩ	

Table 2. ASLIC Device DC Specifications (continued)

No.	Item	Condition	Min	Typ	Max	Unit	Note
12	ISUM/ILOOP	ILOOP = 10 mA	1/333	1/300	1/273		
13	IDIF/ILONG	ILONG = 10 mA	1/667	1/600	1/546		
14	Input current, SA and SB pins			1	3	µA	4
15	Input current HPA and HPB pins			0.1	3		
16	IDC input impedance		1.26	1.8	3	kΩ	
17	K1	Incremental DC current gain		254		A/A	13
18	Metallic offset current			0	–0.4	mA	

ASLIC Device Relay Driver Schematic

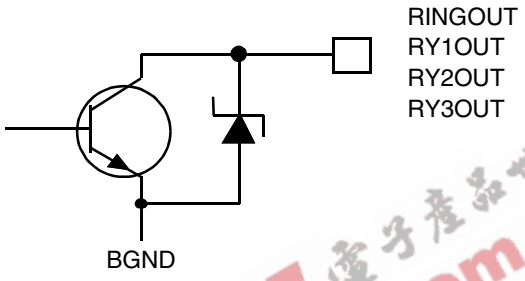


Table 3. ASLIC Device Relay Driver Specifications

Item	Condition		Min	Typ	Max	Unit	Note
On voltage	25 mA per relay sink	1 relay on		0.225	0.3	V	
		4 relays on		0.4	0.5		4
	40 mA per relay sink	1 relay on		0.45	0.7		
		4 relays on		0.8	1.0		4
Off leakage, each relay driver	V_{OH} = +6 V		0		100	µA	

Table 4. ASLIC Device Transmission Specifications

No.	Item	Condition	Min	Typ	Max	Unit	Note
1	R_{SN} input impedance	f = 300 Hz to 3400 Hz		1		Ω	4
2	V_{TX} output impedance			3			
3	Gain, BAL1 to V_{TX}		1.4	1.5	1.6	V/V	
4	BAL1 input impedance		3.17	5	7.5	kΩ	4
5	Input impedance A or B to GND			70	135	Ω	

Table 4. ASLIC Device Transmission Specifications (continued)

No.	Item	Condition	Min	Typ	Max	Unit	Note
6	2- to 4-wire gain	–10 dBm, 1 kHz T_A = –40°C to 0°C/70°C to 85°C	–12.19 –12.24	–12.04	–11.89 –11.84	dB	
7	2- to 4-wire gain variation with frequency	300 to 3400 Hz relative to 1 kHz T_A = –40°C to 0°C/70°C to 85°C	–0.1 –0.15		+0.1 +0.15		
8	2- to 4-wire gain tracking	+3 dBm to –55 dBm Reference: –10 dBm T_A = –40°C to 0°C/70°C to 85°C	–0.1 –0.15		+0.1 +0.15		
9	4- to 2-wire gain	–10 dBm, 1 kHz T_A = –40°C to 0°C/70°C to 85°C	–0.15 –0.20	0	+0.15 +0.20		
10	4- to 2-wire gain variation with frequency	300 to 3400 Hz relative to 1 kHz T_A = –40°C to 0°C/70°C to 85°C	–0.1 –0.15		+0.1 +0.15		
11	4- to 2-wire gain tracking	+3 dBm to –55 dBm Reference: –10 dBm	–0.1 –0.15		+0.1 +0.15		
12	Total harmonic distortion 2-wire	300 Hz to 3400 Hz 0 dBm +4 dBm			 –50 –40		
	4-wire	–12 dBm –8 dBm			 –50 –40		
	2-wire metering overload level	VLBIAS = 2.4 V, ILOOP = 30 mA, V_{BAT} = Q_{BAT} = –60 V, DC LOAD = 200 Ω, Load at 16 kHz = 10 kΩ		42		Vp-p	4
13	Idle channel noise C-message weighted	Active and Disable states 2-wire T_A = –40°C to 0°C/70°C to 85°C		+7	+11 +15	dBrnC	 4
		4-wire		–5			4
	Psophometric weighted	2-wire T_A = –40°C to 0°C/70°C to 85°C		–83	–79 –75	dBmp	
		4-wire		–95			4
14	Longitudinal balance (IEEE method) Normal polarity	L - T 200 to 1000 Hz T_A = –40°C to 0°C/70°C to 85°C 1000 to 3400 Hz T_A = –40°C to 0°C/70°C to 85°C	58 53 53 48	63 58		dB	
		T - L 200 to 3400 Hz	40				
		L - T, IL = 0 50 to 3400 Hz		63			4
	Reverse polarity	L - T 200 to 1000 Hz T_A = –40°C to 0°C/70°C to 85°C	50 48				
15	PSRR (V_{BAT}, Q_{BAT})	50 to 3400 Hz	25	45			3, 5
		3.4 kHz to 50 kHz	25	40			4
		ASLIC device in Anti-Sat state (loop open) f = 50 Hz, CB = 100 nF f = 200 to 3400 Hz, CB = 100 nF	 2 12				4, 8

Table 4. ASLIC Device Transmission Specifications (continued)

No.	Item	Condition	Min	Typ	Max	Unit	Note
16	PSRR (V_{CC})	50 to 3400 Hz	25	45		dB	3, 5
		3.4 kHz to 50 kHz	25	35			2, 4
17	Low frequency induction (REA method)	Active state, VLONG = 30 Vrms, I_L = 20 mA, f = 60 Hz			+23	dBrnC	4
18	Longitudinal AC current per wire	f = 15 to 60 Hz	20			mArms	

Table 5. ASLAC Device DC Specifications

No.	Item	Condition	Min	Typ	Max	Unit	Note
1	Input Low voltage	(Any digital input)	–0.5		0.8	V	
2	Input High voltage	(Any digital input)	2.0		V_{CC} + 0.5		
3	Input leakage current	(Any digital input)	–10		+10	µA	15
4	Input hysteresis (FS and $\overline{RST}$ only)			0.5		V	4
5	Ternary output voltages C2–C1						
	High voltage	I_{OUT} = ±200 µA	V_{CC} – 0.85			V	
	Low voltage	I_{OUT} = ±200 µA			0.65		
	Output current	Mid level	–1		+1	µA	
6	Output Low voltage on digital outputs DXA, DXB, DI/O, $\overline{TNT}$, $\overline{TSCA}$, $\overline{TSCB}$, I/O_1, I/O_2, I/O_3, I/O_4	I_{OL} = 2 mA			0.4	V	
	$\overline{TSCA}$, $\overline{TSCB}$	I_{OL} = 14 mA			0.4		
	I/O_1, I/O_2, I/O_3, I/O_4	I_{OL} = 10 mA			1.0		
7	Output High voltage (all digital outputs except $\overline{INT}$ in the Open Drain state and $\overline{TSC}$)	I_{OH} = 400 µA	V_{CC} – 0.4				
8	DC Feed	ILA = 47.6 mA, RFD = 403 Ω, N2 = 2, VAS = 10.3 V, IBAT = 69.9 µA					19
	IDC	Active state, Normal polarity, IAB = 0, VAPP = 50.2 V	172.7	188.5	204.9	µA	
	$\frac{\Delta IAB}{\Delta IDC}$	In resistive-feed region	0.0624	0.0694	0.0764	A/A	
	IAB	IBAT = 69.9 µA Adjust IAB until IDC = 0	27.93	29.93	31.93	µA	19
	Measured VAPP	Programmed VAPP = 50.2 V		±2.2		V	
	Measured VAS	Programmed VAS = 10.3 V		±1.6			

Table 5. ASLAC Device DC Specifications (continued)

No.	Item	Condition	Min	Typ	Max	Unit	Note
9	IDC error among programmed ILA, ILD	Any ILA or ILD programmed value > 20 mA (IDC > 78.7 µA)		±5		%	4, 19
		Any ILA or ILD programmed value ≤ 20 mA (IDC ≤ 78.7 µA)		±4		µA	19
10	Offset voltage allowed on V_{IN}		–50		+50	mV	10
11	V_{OUT} offset voltage	AISN off	–40		+40		10, 19
		AISN on	–80		+80		10
12	Output voltage, V_{REF}	Load current = 0 to 1 mA Source or sink	2.0	2.1	2.2	V	19
13	Capacitance load on V_{REF} or V_{OUT}				200	pF	4
14	Output current V_{OUT}	Source or sink	–1		+1	mA	
15	Input resistance IDIF pin to V_{REF}		8.84	13.6	18.36	kΩ	6
16	VLBIAS operating voltage	Source current < 250 µA or sink current < 25 µA	+1		+2.4	V	18
17	Percent error of VLBIAS voltage	For VLBIAS equation see longitudinal control loop	–5		+5	%	
18	Capacitance load on VLBIAS				120	pF	6
19	Capacitance load on IRTA or IRTB				400		

Table 6. ASLAC Device Transmission and Signaling Specifications

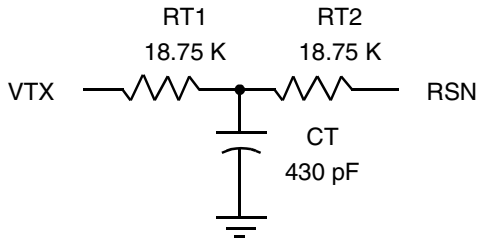
No.	Item	Condition	Min	Typ	Max	Unit	Note
1	Insertion loss	Input: 1014 Hz, –10 dBm0 RG = AR = AX = GR = GX = 0 dB, AISN, R, X, B, and Z filters disabled				dB	7
	A-D	T_A = 0°C to 70°C	–0.25	0	+0.25		
		T_A = –40°C to 0°C/70°C to 85°C	–0.30	0	+0.30		
	D-A	T_A = 0°C to 70°C	–0.25	0	+0.25		
		T_A = –40°C to 0°C/70°C to 85°C	–0.30	0	+0.30		
	A-D + D-A	T_A = 70°C	–0.20	0	+0.20		
		T_A = 0°C –70°C; VCC = 4.75 – 5.25 V	–0.25	0	+0.25		
		T_A = –40°C to 0°C/70°C to 85°C	–0.34	0	+0.34		
2	Level set error (error between setting and actual value)	A-D AX + GX	–0.1		+0.1		
		D-A AR + GR	–0.1		+0.1		
3	DR to DX gain in Full Digital Loopback mode	DR input: 1014 Hz, –10 dBm0 RG = AR = AX = GR = GX = 0 dB, AISN, R, X, B, and Z filters disabled	–0.3		+0.3		
		T_A = –40°C to 0°C/70°C to 85°C	–0.35		+0.4		
4	Idle channel noise, psophometric weighted (A-law)	AX = 0 dB AR = 0 dB A-D (PCM output)			–68	dBm0p	12
		D-A (V_{OUT})			–78		
5	Idle channel noise, C-message weighted (μ-law)	AX = 0 dB AR = 0 dB A-D (PCM output), GX = +8 dB			+16	dBrnC0	
		D-A (2 wire), GR = –8 dB			+12		
6	Coder offset decision value, Xn	A-D, Input signal = 0 V, A-law	–5		+5	Bits	6
7	GX step size	0 ≤ GX < 10 dB 10 ≤ GX ≤ 12 dB			0.1 0.3	dB	4
8	GR step size	–12 ≤ GR ≤ 0 dB			0.1		
9	PSRR (V_{CC}) Image frequency	Input: 4800 to 7800 Hz 200 mV p-p Measure 8000 Hz input frequency					
		A-D	37			dB	4
		D-A	37				
10	Group delay PCLK ≥ 1.53 MHz PCLK ≤ 1.03 MHz	1014 Hz; –10 dBm0 B, X, R, and Z filters set to default			590 655	μs	4, 14

Table 6. ASLAC Device Transmission and Signaling Specifications (continued)

No.	Item	Condition	Min	Typ	Max	Unit	Note
11	Switchhook thresholds	All TSH settings	–0.45 or –10		+0.45 or +10	mA %	9,16, 19
	Switchhook hysteresis	All TSH settings		–10		%	4
12	Ground-key thresholds	All TGK settings	–0.90 or –10		+0.90 or +10	mA %	9,16, 19
	Ground-key hysteresis	All TGK settings		–10		%	4
13	Voltage that sets thermal shutdown bit	Voltage on ASLIC device VDC with RAB = 35.7 kΩ	+4.19			V	
14	IDIF fault-current thresholds	Tip-to-battery fault current (mA)					
	FT, pkFT	19.3, 50.6	–10		+10		16, 19
	FT, pkFT hysteresis			–10			4
15	AISN gain accuracy	G_{AISN} = ±0.0625	–16		+16	%	4
		G_{AISN} = ±0.125	–8		+8		
		G_{AISN} = ±0.1875	–6		+6		
		G_{AISN} = ≤ –0.25 or G_{AISN} ≥ +0.25	–4		+4		
16	Metering voltage (MTRA) accuracy	Measured at ASLAC device VM pin	–7		+7		
17	Metering voltage noise	Wide-band signal to noise	40			dB	
18	Ring-trip accuracy		–5		5	%	4,17, 20
19	Ring-trip hysteresis	V_{ZX} I_{ZX}		4 5		V µA	4, 17
20	Power-cross accuracy	During transmission	–10		+10	%	17, 20
		During ringing	–10		+10		

Notes:

1. *Unless otherwise specified, test conditions are:*
   V_{CC} = 5 V, R_{TMG} = 1200 Ω, Q_{BAT} = BAT = –51 V, R_{AB} = 35.7 kΩ, R_{BAT1} = R_{BAT2} = 365 kΩ, R_{REF} = 7.87 kΩ, R_{RX} = 75 kΩ, R_L = 600 Ω, R_{SA} = R_{SB} = 200 kΩ, C_{HP} = 220 nF, C_{DC1} = 1.0 µF, 50 Ω fuse resistors, R_{SR1} = R_{SR2} = 750 kΩ, C_{AD} = C_{BD} = 22 nF, C_B = 100 nF and the following network is connected between V_{TX} and R_{SN}:



Ambient temperature = 70°C
Active state, normal polarity for transmission performance
0 dBm = 1 mW @ 600 Ω (0.775 Vrms)

Programmed DC Feed conditions:
VAPP (apparent battery voltage) = 50.2 V
ILA (Active state loop-current limit) = 47.6 mA
ILD (Disable state loop-current limit) = 21.2 mA
RFD (DC Feed resistance) = 403 Ω
VAS (anti-sat activate voltage) = 10.3 V
N2 (anti-sat feed resistance factor) = 2
VOFF (longitudinal offset voltage) = 8.4 V

RG = GX = GR = AX = AR = 0 dB

R, X, B, and Z filters set to default

AISN = 0

TSH < ILD

TSH = Programmed switchhook detect threshold current

ILD = Programmed disable limit current

DC Feed conditions are normally set by the ASLAC device. When the ASLIC device is tested by itself, its operating conditions must be simulated as if it were connected to an ideal ASLAC device. When the ASLAC device is tested by itself, its operating conditions must simulate as if it were connected to an ideal ASLIC device.

2. *These tests are performed with the following load impedances:*
   Frequency < 12 kHz - longitudinal impedance = 500 Ω; metallic impedance = 300 Ω
   Frequency > 12 kHz - longitudinal impedance = 90 Ω; metallic impedance = 135 Ω
3. *This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.*
4. *Not tested or partially tested in production. This parameter is guaranteed by characterization or correlation to other tests.*
5. *When the ASLIC/ASLAC devices are in the anti-sat operating region, this parameter will be degraded. The exact degradation will depend on system design.*
6. *Guaranteed by design.*
7. *Overall 1.014 kHz insertion loss error of the ASLIC/ASLAC devices kit is guaranteed to be ≤ 0.34 dB.*
8. *These VBAT/QBAT, PSRR specifications are valid only when the ASLIC device is used with the ASLAC device that generates the anti-sat reference. Since the anti-sat reference depends upon the battery voltage sensed by the IBAT pin of the ASLAC device, the PSRR of the kit will depend upon the amount of battery filtering provided by CB.*
9. *Must meet at least one of these specifications.*
10. *These voltages are referred to VREF.*
11. *These limits refer to the two-wire output of an ideal ASLIC device but reflect only the capabilities of the ASLAC device.*
12. *When relative levels (dBm0) are used, the specification holds for any setting of (AX + GX) gain from 0 to 12 dB or (AR + GR + RG) from 0 to –12 dB.*
13. *This parameter tested by inclusion in another test.*
14. *The group delay specification is defined as the sum of the minimum values of the group delays for the transmit and the receive paths when the transmit and receive time slots are identical and the B, X, R, and Z filters are disabled with null coefficients. For PCLK frequencies between 1.03 MHz and 1.53 MHz, the group delay may vary from one cycle to the next. See also Figure 2, Group Delay Distortion.*
15. *I/O_1 and I/O_2 have an additional circuit that pulls the pin High during 3-state.*
16. *These limits reflect only the capabilities of the ASLAC device.*
17. *RSR1 = RSR2 = 750 kΩ, RGFD1 = 510 Ω.*
18. *DC Feed performance derates by 5% when operating from –40°C to 0°C and 70°C to 85°C.*
19. *Threshold values derate by 5% when operating from –40°C to 0°C and 70°C to 85°C.*
20. *Power cross and ring trip values derate by 5% when operating from –40°C to 0°C and 70°C to 85°C.*

In the following section, the transmit path is defined as the section between the analog input to the ASLAC device (VIN) and the PCM voice output of the ASLAC device A-law/µ-law speech compressor (shown in the technical overview document). The receive path is defined as the section between the PCM voice input to the ASLAC device speech expander and the analog output of the ASLAC device (VOUT). All limits defined in this section are tested with B = 0, Z = 0 and X = R = RG = 1.

When RG is enabled, a nominal gain of –6.02 dB is added to the digital section of the receive path.
When AR is enabled, a nominal gain of –6.02 dB is added to the analog section of the receive path.
When AX is enabled, a nominal gain of +6.02 dB is added to the analog section of the transmit path.

When the gains in the transmit path are set to AX = 0 dB and GX = 0 dB, a 1014 Hz sine wave with a nominal voltage of 0.596 Vrms for µ-law and 0.6 Vrms for A-law at the ASLAC device analog input will correspond to a level of 0 dBm0 at the PCM voice output. Under these conditions, the overload level of the transmit path is 1.25 Vpeak referenced to VREF.

When the gains in the receive path are set to AR = GR = 0 dB, a 1014 Hz sine wave with a level of 0 dBm0 at the PCM voice input will correspond to a nominal voltage of 0.596 Vrms for µ-law and 0.6 Vrms for A-law at the analog output of the ASLAC device. Under these conditions, the maximum receive output level is 1.25 Vpeak referenced to VREF.

When relative levels (dBm0) are used in any of the following transmission characteristics, the specification holds for any setting of (AX + GX) gain from 0 to 12 dB or (AR + GR + RG) from 0 to –12 dB.

These transmission characteristics are valid for 0°C to 70°C and for VCC = +5 V ± 0.25 V.

Attenuation Distortion

The deviations from nominal attenuation will stay within the limits shown in Figure 1. The reference frequency is 1014 Hz and the signal level is –10 dBm0. Minimum transmit attenuation at 60 Hz is 24 dB.

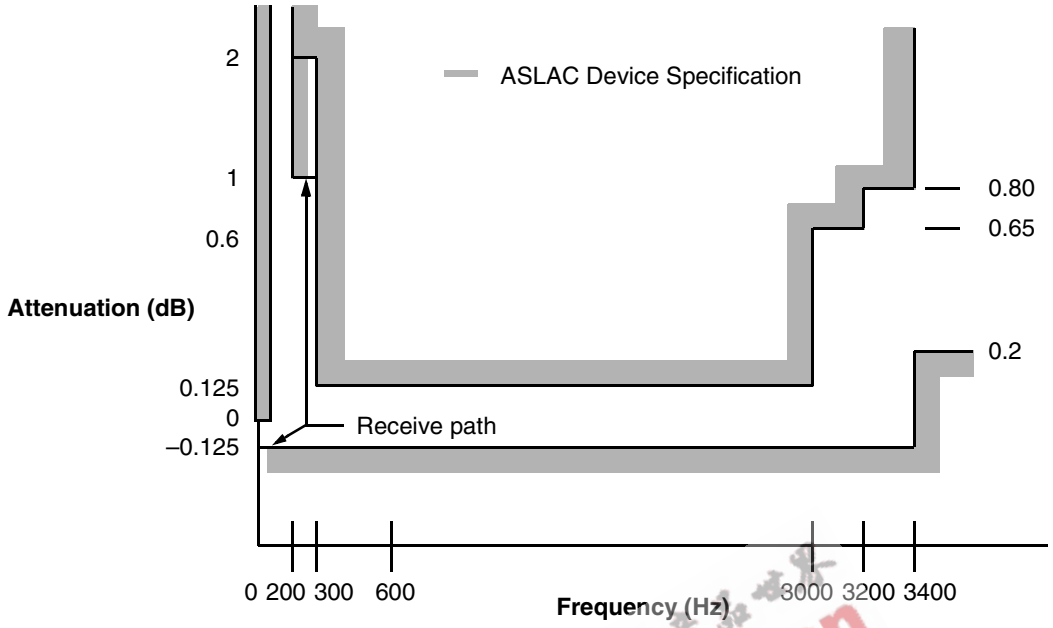


Figure 1. Transmit and Receive Path Attenuation vs. Frequency

Group Delay Distortion

For either transmission path, the group delay distortion is within the limits shown in Figure 2. The minimum value of the group delay is taken as the reference. The signal level should be –10 dBm0.

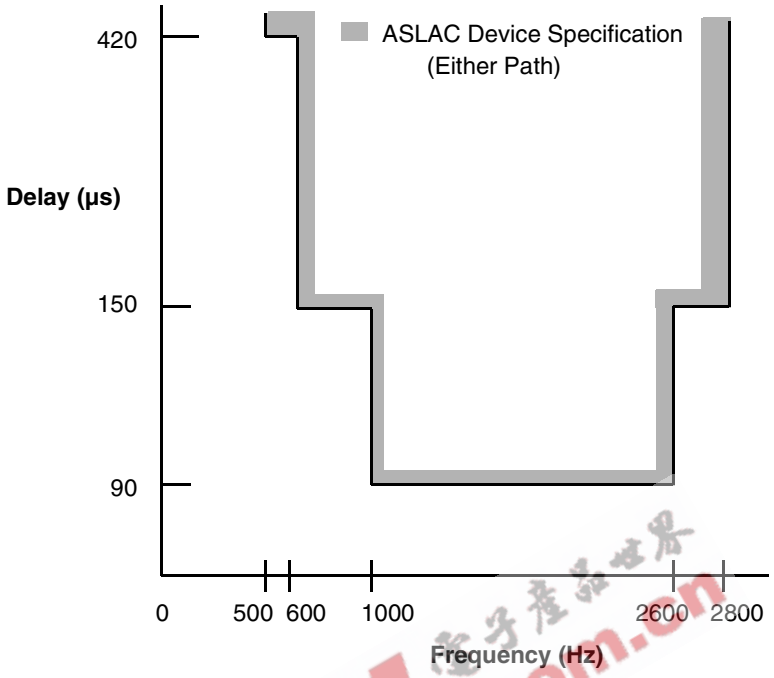


Figure 2. Group Delay Distortion

Single Frequency Distortion

The output signal level at any single frequency in the range of 300 Hz to 3400 Hz, other than that due to an applied 0 dBm0 sine wave signal with frequency f_0 in the same frequency range, is less than –46 dBm0. With f_0 swept between 0 to 300 Hz and 3400 Hz to 12 kHz, any generated output signals other than f_0 are less than –28 dBm0. This specification is valid for either transmission path.

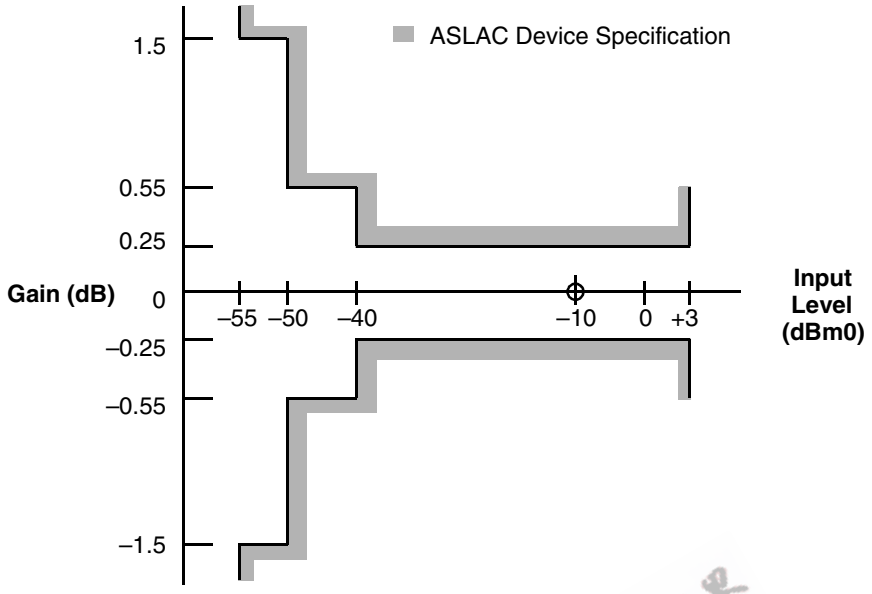
Intermodulation Distortion

Two sine wave signals of different frequencies f1 and f2 (not harmonically related) in the range 300 Hz to 3400 Hz and of equal levels in the range –4 dBm0 to –21 dBm0 will not produce 2 • (f1 – f2) products having a level greater than –42 dB relative to the level of the two input signals.

A sine wave signal in the frequency band 300 Hz to 3400 Hz with input level –9 dBm0 and a 50 Hz signal with input level –23 dBm0 will not produce intermodulation products exceeding a level of –56 dBm0. These specifications are valid for either transmission path.

Gain Linearity

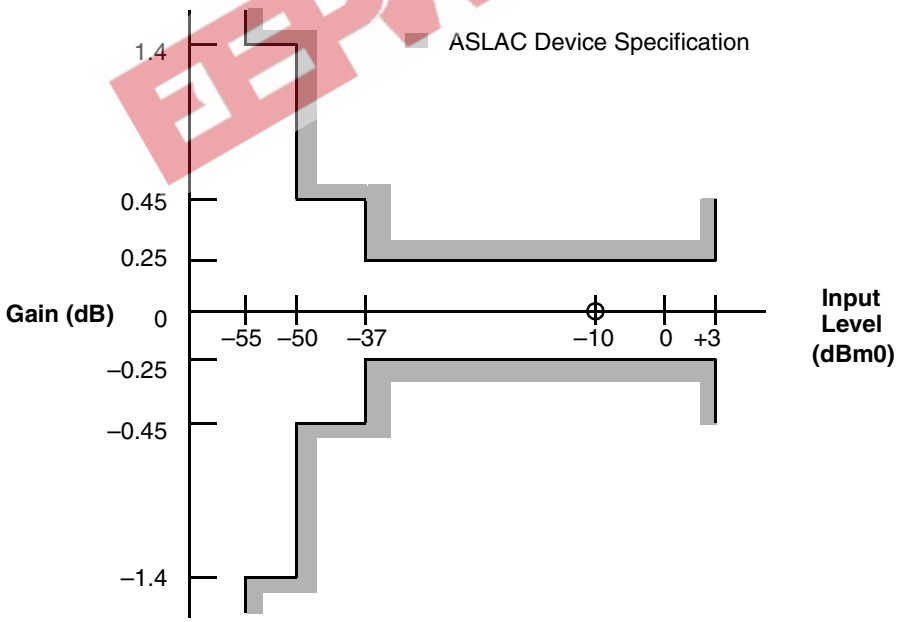
The gain deviation relative to the gain at –10 dBm0 is within the limits shown in Figure 3 (A-law) and Figure 4 (µ-law) for either transmission path when the input is a sine wave signal of 1014 Hz.



Note:

Relax specification by 0.05 dB at –40°C.

Figure 3. A-law Gain Linearity with Tone Input (Both Paths)



Note:

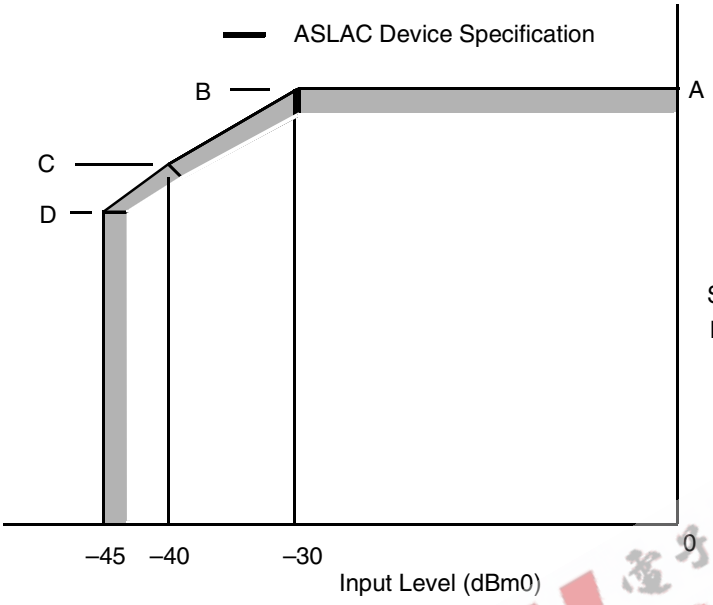
Relax specification by 0.05 dB at –40°C.

Figure 4. µ-law Gain Linearity with Tone Input (Both Paths)

Total Distortion, Including Quantizing Distortion

The signal-to-total distortion ratio will exceed the limits shown in Figure 5 for either path when the input signal is a sine wave signal of frequency 1014 Hz.

Improved distortion at lower levels in LSSGR applications can be obtained by proper selection of the GX and GR ranges.



	A-law	μ-law
A	35.5 dB	35.5 dB
B	35.5 dB	35.5 dB
C	30 dB	31 dB
D	25 dB	27 dB

Figure 5. Total Distortion with Tone Input (Both Paths)

Overload Compression

Figure 6 shows the acceptable region of operation for input signal levels above the reference input power (0 dBm0). The conditions for this figure are:

(1) 1 dB < transmit path ≤ +12 dB; (2) –12 dB ≤ receive path < –1 dB; (3) digital voice output connected to digital voice input; and (4) measurement analog-to-analog.

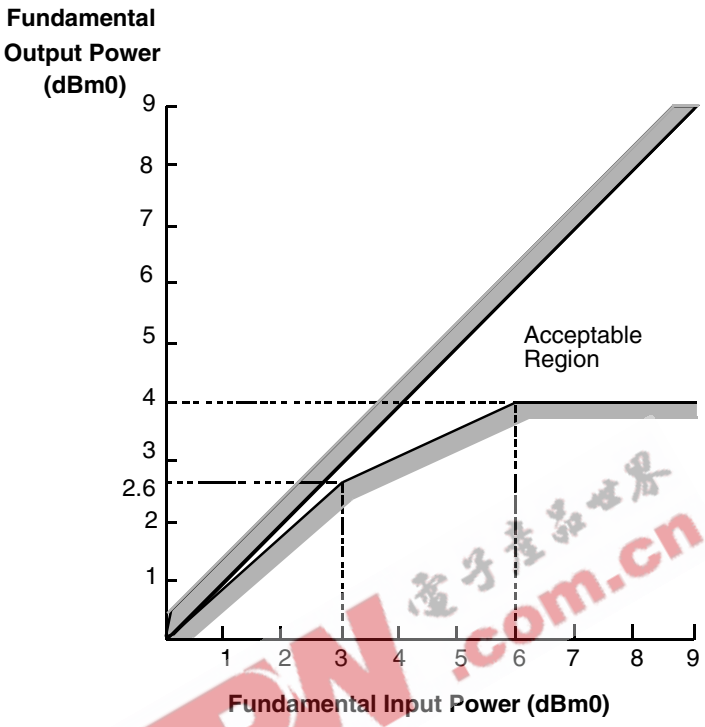


Figure 6. A/A Overload Compression

SWITCHING CHARACTERISTICS

Microprocessor Interface

Min. and Max. values are valid for all digital outputs with a 100 pF load, except DI/O, DXA, and DXB, which are valid with 150 pF loads.

Table 7. Microprocessor Interface

No.	Symbol	Parameter	Min	Typ	Max	Units	Note
1	t_{DCY}	Data clock period	244			ns	
2	t_{DCH}	Data clock High pulse width	97			ns	1
3	t_{DCL}	Data clock Low pulse width	97			ns	1
4	t_{DCR}	Rise time of clock			25	ns	
5	t_{DCF}	Fall time of clock			25	ns	
6	t_{ICSS}	Chip select setup time, Input mode	70		t_{DCY} – 10	ns	
7	t_{ICSH}	Chip select hold time, Input mode	0		t_{DCH} – 20	ns	
8	t_{ICSL}	Chip select pulse width, Input mode		$8t_{DCY}$		ns	
9	t_{ICSO}	Chip select off time, Input mode	5			µs	1, 7
10	t_{IDS}	Input data setup time	30			ns	6
11	t_{IDH}	Input data hold time	30			ns	
12	t_{OLH}	SLIC output latch valid	0	1.2	1.9	µs	
13	t_{OCSS}	Chip select setup time, Output mode	70		t_{DCY} – 10	ns	
14	t_{OCSH}	Chip select hold time, Output mode	0		t_{DCH} – 20	ns	
15	t_{OCSL}	Chip select pulse width, Output mode		$8t_{DCY}$		ns	
16	t_{OCSO}	Chip select off time, Output mode	5			µs	1, 7
17	t_{ODD}	Output data turn on delay			50	ns	
18	t_{ODH}	Output data hold time	3			ns	
19	t_{ODOF}	Output data turn off delay			50	ns	
20	t_{ODC}	Output data valid	0		50	ns	
21	t_{RST}	Reset pulse width	50			µs	

Table 8. PCM Interface

No.	Symbol	Parameter	Min	Typ	Max	Units	Note
22	t_{PCY}	PCM clock period	0.122		7.8125	µs	2
23	t_{PCH}	PCM clock High pulse width	48			ns	
24	t_{PCL}	PCM clock Low pulse width	48			ns	
25	t_{PCF}	Fall time of clock			15	ns	
26	t_{PCR}	Rise time of clock			15	ns	
27	t_{FSS}	FS setup time	30		t_{PCY} – 35	ns	
28	t_{FSH}	FS hold time	0			ns	
29	t_{FCH}	FS High pulse width	t_{PCY}			ns	
30	t_{TSD}	Delay to $\overline{TSC}$ valid	5		80	ns	3
31	t_{TSO}	Delay to $\overline{TSC}$ off	5		80	ns	3, 4
32	t_{DXD}	PCM data output delay	5		80	ns	5
33	t_{DXH}	PCM data output hold time	5		80	ns	5
34	t_{DXZ}	PCM data output delay to High-Z	5		80	ns	5
35	t_{DRS}	PCM data input setup time	25			ns	
36	t_{DRH}	PCM data input hold time	5			ns	

Master Clock

For 2.048 MHz ± 100 ppm, 4.096 MHz ± 100 ppm, or 8.192 MHz ± 100 ppm operation:

Table 9. Master Clock

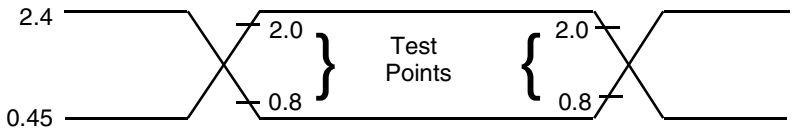
No.	Symbol	Parameter	Min.	Typ.	Max.	Units	Note
37	t_{MCY}	Master clock period (2.048 MHz)	488.23	488.28	488.33	ns	2
		Master clock period (4.096 MHz)	244.11	244.14	244.17	ns	
		Master clock period (8.192 MHz)	122.05	122.07	122.09	ns	
38	t_{MCR}	Rise time of clock			15	ns	
39	t_{MCF}	Fall time of clock			15	ns	
40	t_{MCH}	MCLK High pulse width	48			ns	
41	t_{MCL}	MCLK Low pulse width	48			ns	

Notes:

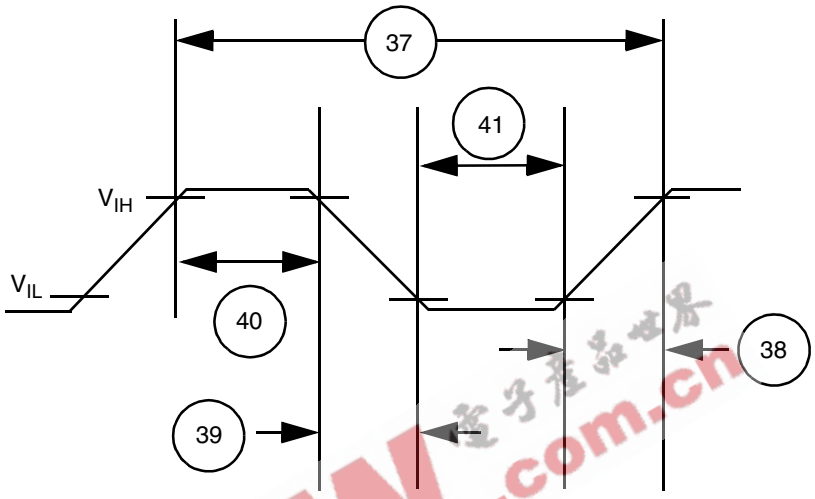
1. *DCLK may be stopped in the High or Low state indefinitely without loss of information.*
2. *The PCM clock (PCLK) frequency must be an integer multiple of the frame sync (FS) frequency with an accuracy of 800 ppm relative to the MCLK frequency. This allowance includes any jitter that may occur between the PCM signals (FS, PCLK) and MCLK. The actual PCLK rate is dependent on the number of channels allocated within a frame. The ASLAC device supports 2 to128 channels. The minimum clock frequency is 128 kHz. A PCLK of 1.544 MHz may be used for standard U.S. transmission systems.*
3. *$\overline{TSC}$ is delayed from FS by a typical value of N • tPCY, where N is the value stored in the time/clock slot register.*
4. *t_{TSO} is defined as the time at which the output driver turns off. The actual delay time is dependent on the load circuitry. The maximum load capacitance on $\overline{TSC}$ is 150 pF and the minimum pullup resistance is 360 Ω.*
5. *There is special circuitry that will prevent high-power dissipation from occurring when the DXA or DXB pins of two ASLAC devices are tied together and one ASLAC device starts to transmit before the other has gone into a high-impedance state.*
6. *The first data bit is enabled on the falling edge of Chip Select or on the falling edge of DCLK, whichever occurs last. If chip select is held Low for less than eight clocks, no command or data is accepted. If chip select is held Low for more than eight clocks, the last 8 data bits are used as command or data.*
7. *The ASLAC device requires 40 cycles of the 8 MHz internal clock (5 µs) between SIO operations. If the MPI is being accessed while the MCLK (or PCLK if in combined clock mode) input is not active, a Chip Select Off time of 20 µs is required.*

SWITCHING WAVEFORMS

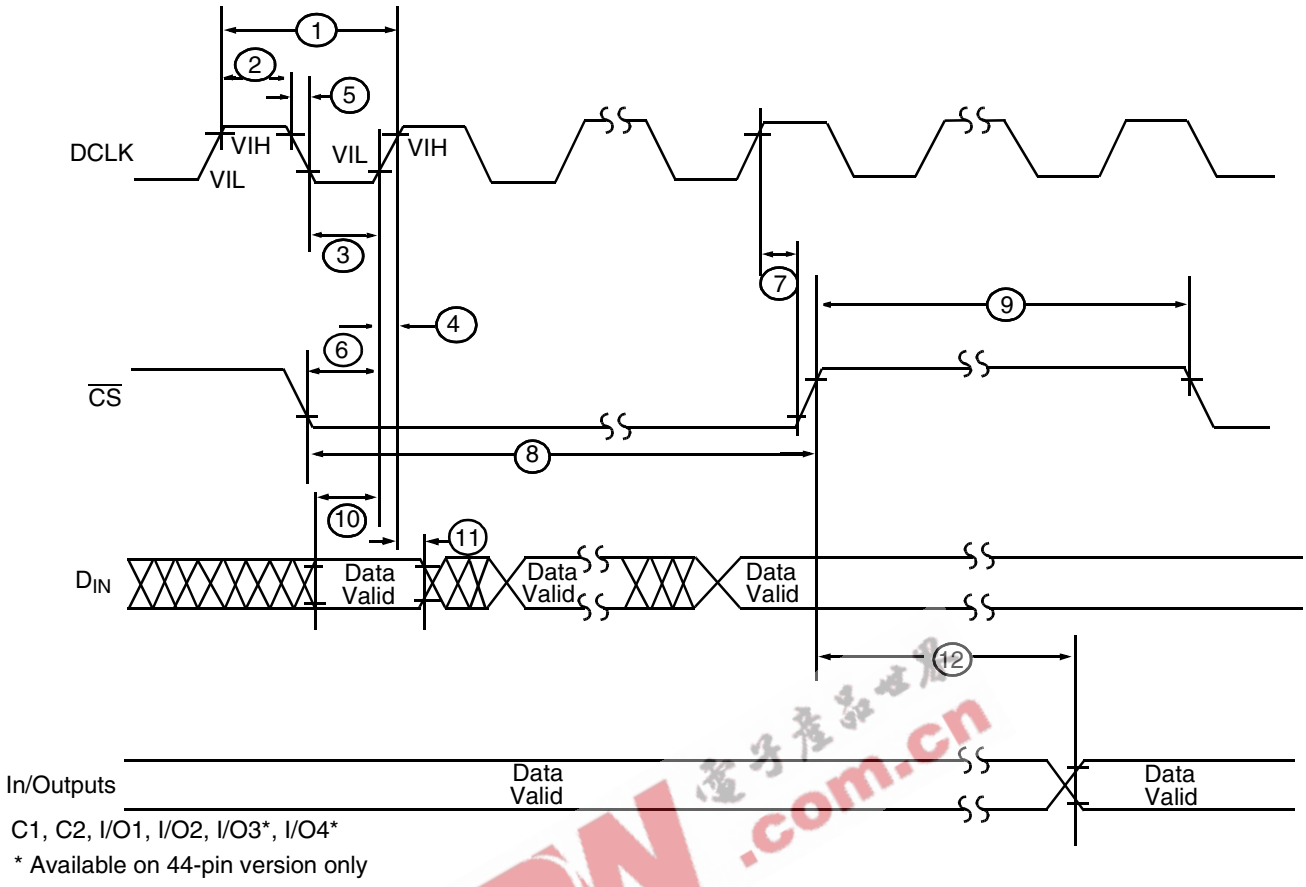
Input and Output Waveforms for AC Tests



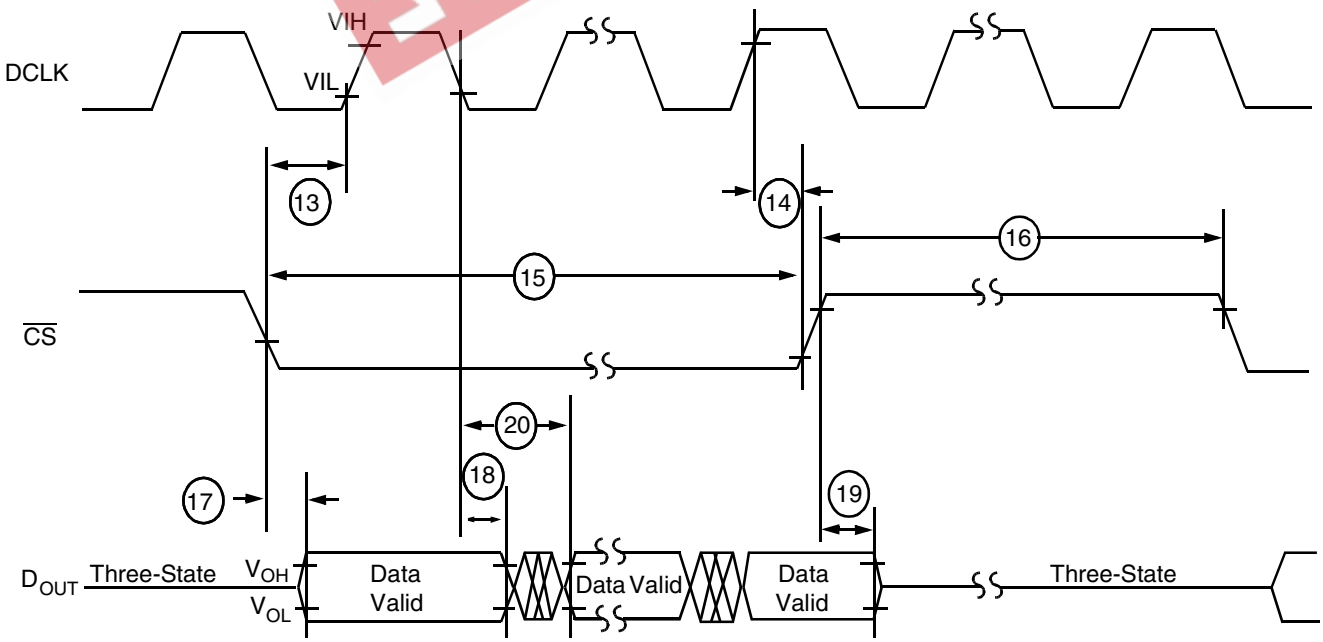
Master Clock Timing



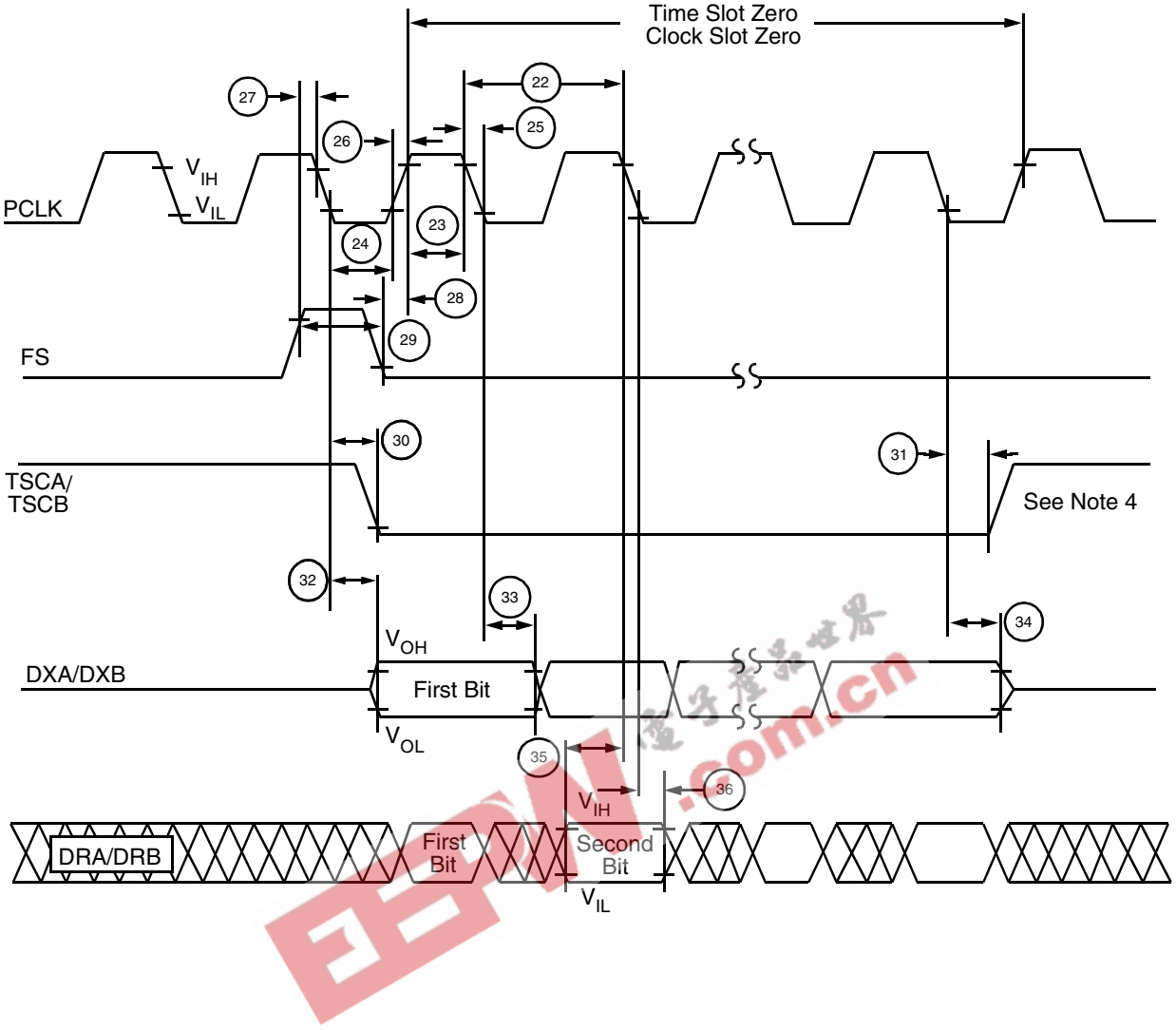
Microprocessor Interface (Input Mode)



Microprocessor Interface (Output Mode)



PCM Highway Timing for XE = 0 (Transmit on Negative PCLK Edge)



PCM Highway Timing for XE = 1 (Transmit on Positive PCLK Edge)

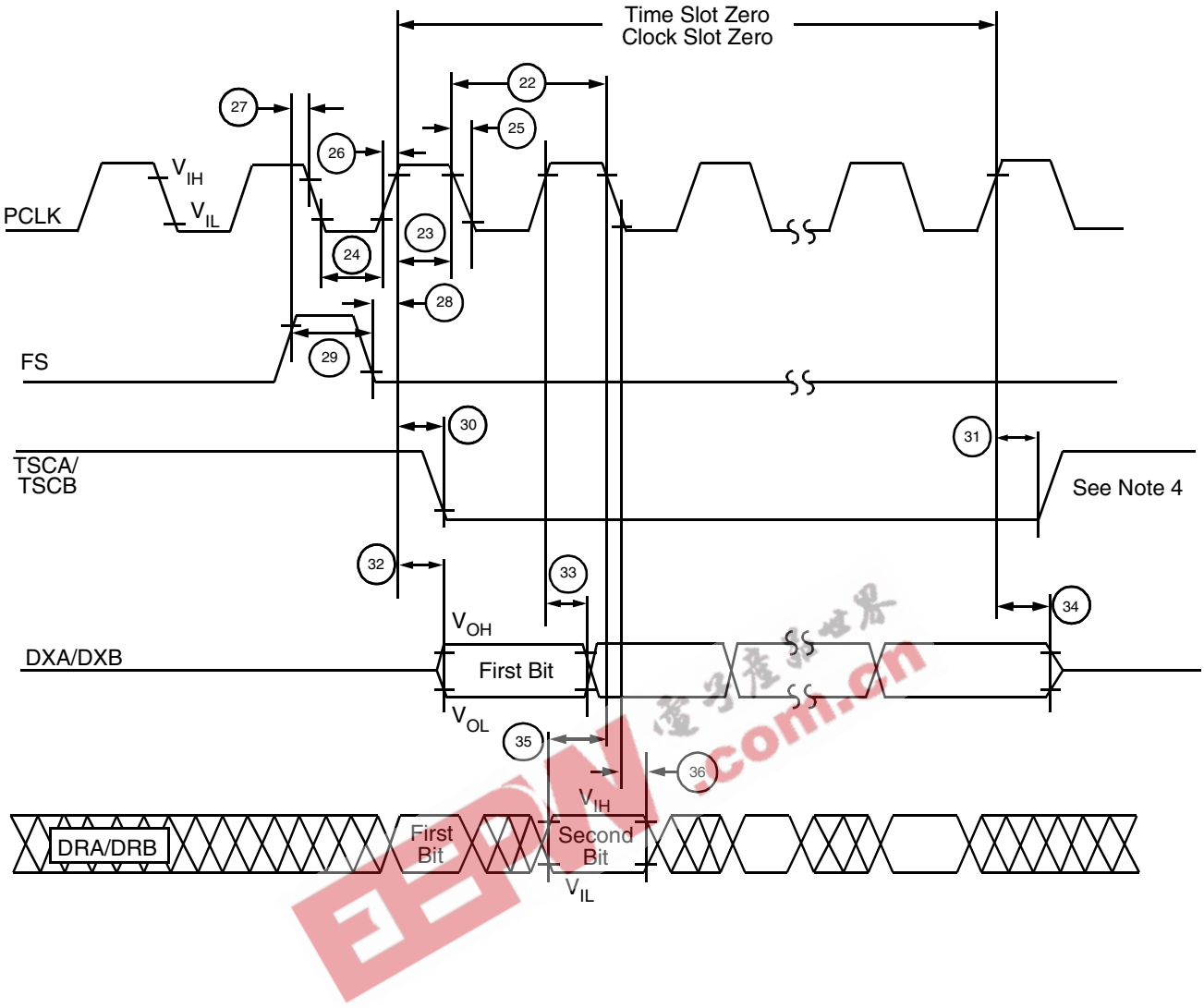
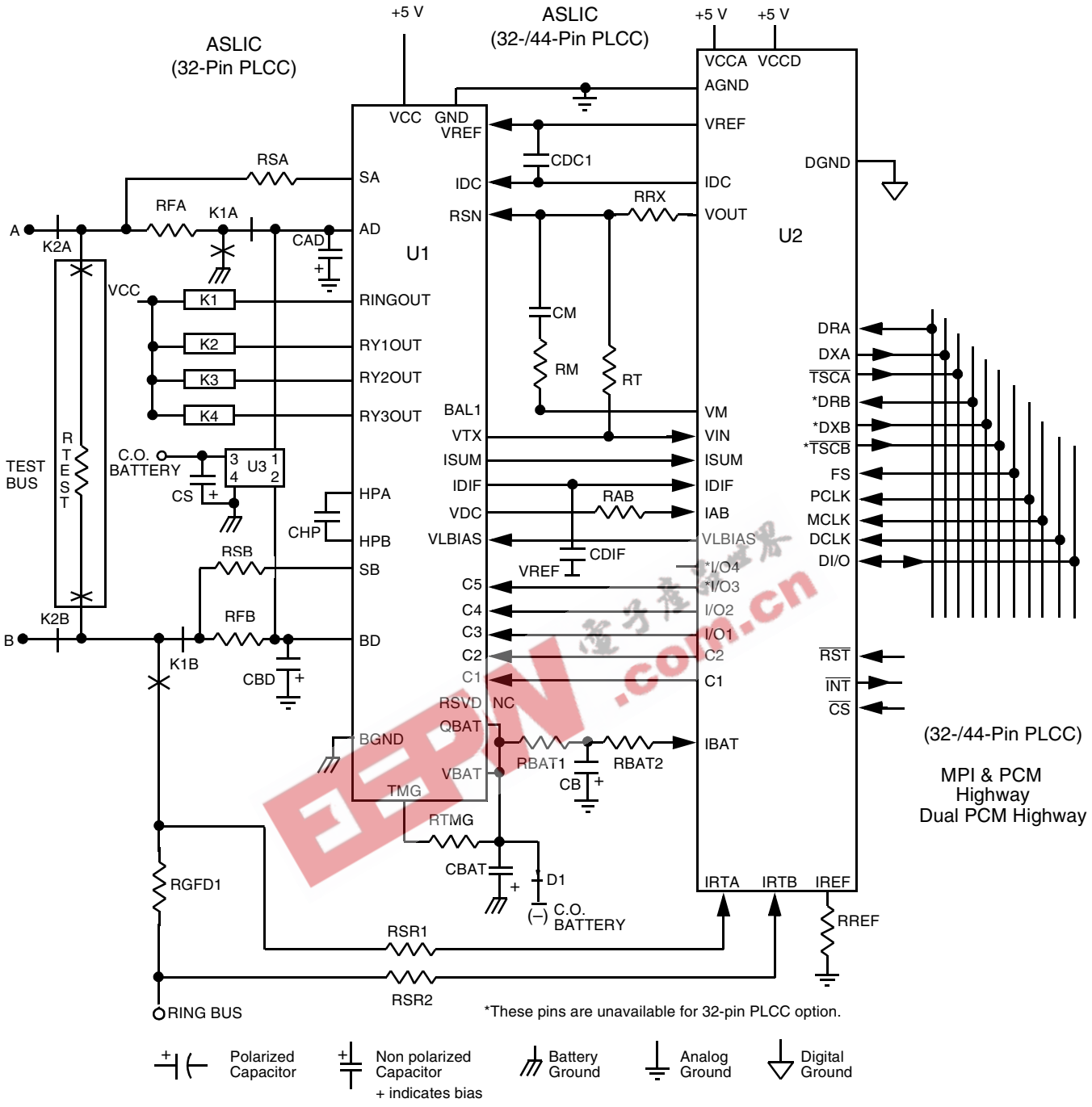


Table 10. User-Programmable Components

$Z_T = 63.5 \bullet (Z_{2WIN} - 2R_F)$	Z_T is connected between the VTX and RSN pins. The fuse resistors are R_F. Z_{2WIN} is the desired 2-wire AC input impedance. When computing Z_T, the internal current amplifier pole and any external stray capacitance between VTX and RSN must be taken into account.
$Z_{RX} = \frac{Z_L}{G_{42L}} \bullet \frac{254 \bullet Z_T}{Z_T + 63.5 \bullet (Z_L + 2R_F)}$	Z_{RX} is connected from VRX to RSN. Z_T is defined above, and G_{42L} is the desired receive gain.
Thermal Management Equations (Normal Active and Tip Open States)	
$R_{TMG} = \frac{V_{BAT} - VOFF}{I_{LOOP}}$	R_{TMG} is connected from TMG to VBAT and is used to reduce power dissipation within the ASLIC device in normal Active and Tip Open states.
$P_{RTMG} = \frac{(V_{BAT} - VOFF - (I_{LOOP} \bullet R_L))^2}{R_{TMG}}$	Power dissipated in the thermal management resistor, R_{TMG}, during normal Active and Tip Open states
$P_{SLIC} = V_{BAT} \bullet I_{LOOP} - P_{RTMG} - R_L \bullet (I_{LOOP})^2 + 0.12\ W$	Power dissipated in the ASLIC device while in normal Active and Tip Open states
Thermal Management equations (Polarity Reverse State) **Note: ASLIC device die temperature should not exceed 140°C.**	
$P_{SLIC} = V_{BAT} \bullet I_{LOOP} - (R_L \bullet (I_{LOOP})^2) + 0.12\ W$	Power dissipated in the ASLIC device while in the Polarity Reverse state
$T_{SLIC} = P_{SLIC} \bullet \theta_{jA} + T_{AMBIENT}$	Total die temperature
$ThetajA(\theta_{jA}) = 43°/watt$	Thermal impedance of the 32-pin plastic leaded chip carrier package

ASLIC/ASLAC DEVICES LINECARD SCHEMATIC



Notes:

1. *This application ckt is valid only to 2.2 V metering.*
2. *If the RSB sense resistor is moved so that it is exposed to the ringing voltage, see the discussion in the* Line Fault Alarm *section.*

Figure 7. ASLIC/ASLAC Typical Linecard Schematic

Table 11. ASLIC/ASLAC Devices Linecard Parts List

Item	Type	Value	Tol.	Rating	Comments
U1	ASLIC device				
U2	ASLAC device				
U3	TCM1060				Transient Voltage Suppressor, Texas Instruments
D1	Diode	100 mA		100 V	1N4002
RFA, RFB	Resistor	50 Ω	2%	2 W	Fusible protection resistors
RSA, RSB	Resistor	200 kΩ	2%	1/4 W	Sense resistors
RSR1, RSR2	Resistor	750 kΩ	2%	1/4 W	Matched to within 0.2% for initial tolerance and 0 to 70°C ambient temperature range. 17 mW typ
RGFD1	Resistor	510 Ω	2%	2 W	1.2 W typ
RRX*	Resistor	51.1 kΩ	1%	1/8 W	<1 mW
RT*	Resistor	51.1 kΩ	1%	1/8 W	<1mW
RBAT1, RBAT2	Resistor	365 kΩ	1%	1/8 W	<5 mW
RAB	Resistor	35.7 kΩ	1%	1/8 W	<1 mW
RREF	Resistor	7.87 kΩ	1%	1/8 W	<1 mW
RTMG *	Resistor	1600 Ω	5%	4 W	Application dependent
RM*	Resistor	3.16 kΩ	1%	1/8 W	Application dependent
RTEST	Resistor	3 kΩ	1%	5 W	Used only if ringing tests are required.
CDIF	Capacitor	6.8 nF	20%	5 V	Ceramic
CAD, CBD *	Capacitor	22 nF	10%	100 V	Ceramic, not voltage sensitive
CBAT	Capacitor	150 nF	20%	100 V	Ceramic, VBAT Typ.
CHP	Capacitor	220 nF	20%	100 V	Ceramic, VBAT Typ.
CB	Capacitor	100 nF	20%	100 V	Ceramic, 0.5 VBAT Typ
CDC1	Capacitor	1.0 µF	20%	5 V	Ceramic
CM*	Capacitor	1.8 nF	10%	5 V	Ceramic
CS *	Capacitor	100 nF	20%	100 V	Protector speed up capacitor
K1	Relay	5 V coil		≤200 mW	DPDT ring relay
K2	Relay	5 V coil		≤200 mW	DPDT (optional) line circuit test
K3, K4	Relay	5 V coil		≤200 mW	optional

Note:
** Value can be adjusted to suit application.*

PROGRAMMABLE FILTERS

General Description of CSD Coefficients

The filter functions are performed by a series of multiplications and accumulations. A multiplication is accomplished by repeatedly shifting the multiplicand and summing the result with the previous value at that summation node. The method used in the ASLAC device is known as Canonic Signed Digit (CSD) multiplication and splits each coefficient into a series of CSD coefficients.

Each programmable FIR filter section has the following general transfer function:

$$HF(z) = h_0 + h_1 z^{-1} + h_2 z^{-2} + \ldots + h_n z^{-n} \qquad \text{Equation (1)}$$

where the number of taps in the filter = n + 1.

The transfer function for IIR part of Z and B filters is:

$$Hl(Z) = \frac{1}{1 - h_{(n+1)} z^{-1}} \qquad \text{Equation (2)}$$

The values of the user-defined coefficients (h_i) are assigned via the MPI. Each of the coefficients (h_i) is defined in the following general equation:

$$h_i = B_1 2^{-M_1} + B_2 2^{-M_2} + \quad + \ldots + B_N 2^{-M_N} \qquad \text{Equation (3)}$$

where:

M_i = the number of shifts = $M_i \leq M_i + 1$

B_i = sign = ±1

N = number of CSD coefficients.

The value of h_i in Equation 3 represents a decimal number which is broken down into a sum of successive values of:

±1.0 multiplied by 2^{-0}, or 2^{-1}, or 2^{-2} … 2^{-7} …

or

±1.0 multiplied by 1, or 1/2, or 1/4 … 1/128 …

The limit on the negative powers of 2 is determined by the length of the registers in the ALU.

The coefficient h_i in Equation 3 can be considered to be a value made up of N binary 1s in a binary register where the left part represents whole numbers, the right part represents decimal fractions, and a decimal point separates them. The first binary 1 is shifted M_1 bits to the right of the decimal point; the second binary 1 is shifted M_2 bits to the right of the decimal point; the third binary 1 is shifted M_3 bits to the right of the decimal point, and so on.

Note that when M_1 is 0, the resulting value is a binary 1 in front of the decimal point, that is, no shift. If M_2 is also 0, the result is another binary 1 in front of the decimal point, giving a total value of binary 10 in front of the decimal point (i.e., a decimal value of 2.0). The value of N, therefore, determines the range of values the coefficient h_i can take (e.g., if N = 3 the maximum and minimum values are ±3, and if N = 4 the values are between ±4).

Detailed Description of ASLAC Device Coefficients

The CSD coding scheme in the ASLAC device uses a value called m_i, where m_i represents the distance shifted right of the decimal point for the first binary 1. m_2 represents the distance shifted to the right of the previous binary 1, and m_3 represents the number of shifts to the right of the second binary 1. Note that the range of values determined by N is unchanged. Equation 3 is now modified (in the case of N = 4) to:

$$h_i = B_1 2^{-M_1} + B_2 2^{-M_2} + B_3 2^{-M_3} + B_4 2^{-M_4} \qquad \text{Equation (4)}$$

$$h_i = C_1 2^{-m_1} + C_1 C_2 2^{-(m_1 + m_2)} + C_1 C_2 C_3 2^{-(m_1 + m_2 + m_3)} + C_1 C_2 C_3 C_4 2^{-(m_1 + m_2 + m_3 + m_4)} \qquad \text{Equation (5)}$$

$$h_i = C_1 2^{-m_1} \left\{ 1 + C_2 2^{-m_2} [1 + C_3 2^{-m_3} (1 + C_4 2^{-m_4})] \right\} \qquad \text{Equation (6)}$$

where:

$M_1 = m_1$ $B_1 = C_1$

$M_2 = m_1+m_2$ $B_2 = C_1 \bullet C_2$

$M_3 = m_1+m_2+m_3$ $B_3 = C_1 \bullet C_2 \bullet C_3$

$M_4 = m_1+m_2+m_3+m_4$ $B_4 = C_1 \bullet C_2 \bullet C_3 \bullet C_4$

In the ASLAC device, a coefficient, h_i, consists of N CSD coefficients, each being made up of 4 bits and formatted as $C_{xy}m_{xy}$, where C_{xy} is one bit (MSB) and m_{xy} is 3 bits. Each CSD coefficient is broken down as follows:

C_{xy} is the sign bit (0 = positive, 1 = negative).

m_{xy} is the 3-bit shift code. It is encoded as a binary number as follows:

000: 0 shifts

001: 1 shifts

010: 2 shifts

011: 3 shifts

100: 4 shifts

101: 5 shifts

110: 6 shifts

111: 7 shifts

y is the coefficient number (the i in h_i).

x is the position of this CSD coefficient within the h_i coefficient. The most significant binary 1 is represented by x = 1. The next most significant binary 1 is represented by x = 2, and so on.

Thus, $C_{13}m_{13}$ represents the sign and the relative shift position for the first (most significant) binary 1 in the 4th (h_3) coefficient.

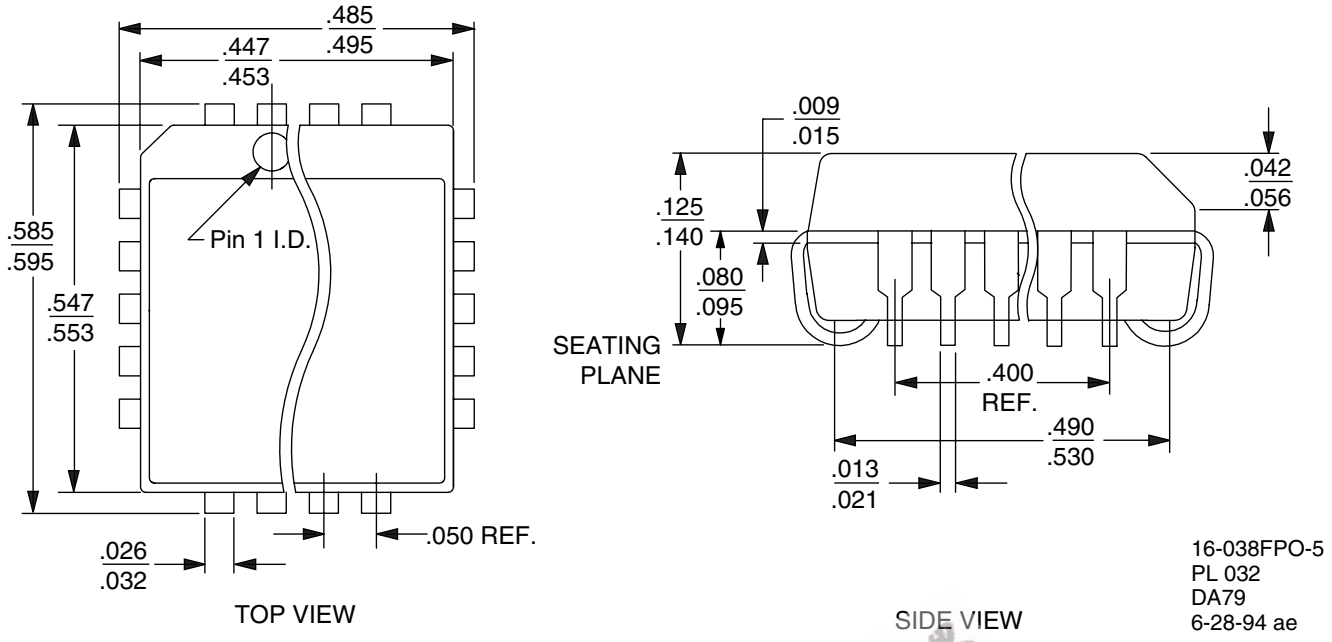
The number of CSD coefficients, N, is limited to 4 in the GR, GX, R, X, Z, and the IIR part of the B filter, and 3 for the FIR part of the B filter. Note also that the GX-filter coefficient equation is slightly different from the other filters.

$$h_{iGX} = 1 + h_i$$ Equation (7)

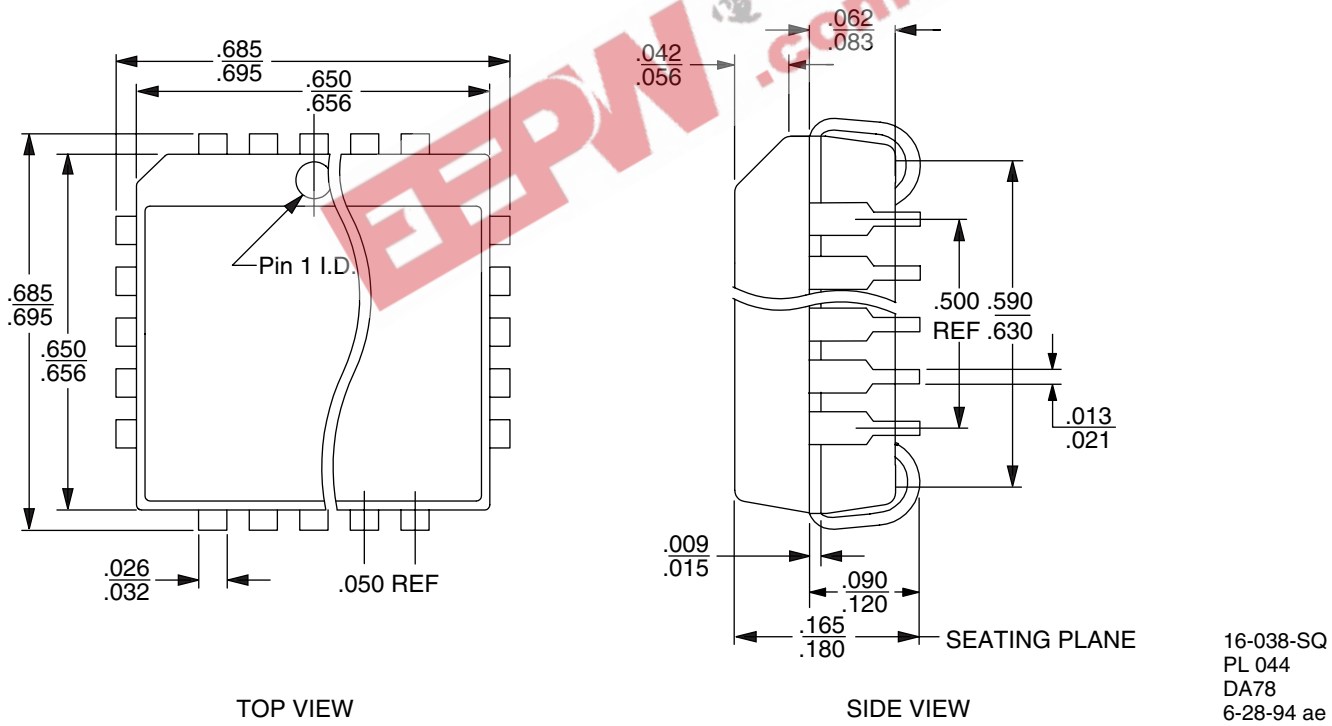
Please refer to the Am79213/Am79C203/031 Technical Reference, PID 21325A detailing the commands for complete details on programming the coefficients.

PHYSICAL DIMENSION

PL032



PL044



REVISION SUMMARY

Revision A to Revision B

- Fixed the figure numbering.
- Minor changes were made to the data sheet style and format to conform to Legerity standards.

Revision B to Revision C

- The physical dimension (PL032 and PL044) was added to the Physical Dimension section.
- Updated the Pin Description table to correct inconsistencies.
- Minor changes were made to the data sheet style and format to conform to Legerity standards.

Revision C to Revision D

- Page 26, Attenuation Distortion, The sentence “The attenuation of the signal in either path is nominally independent of the frequency” was deleted.

Notes:

Notes:

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