FINAL

Am7992B

Serial Interface Adapter (SIA)

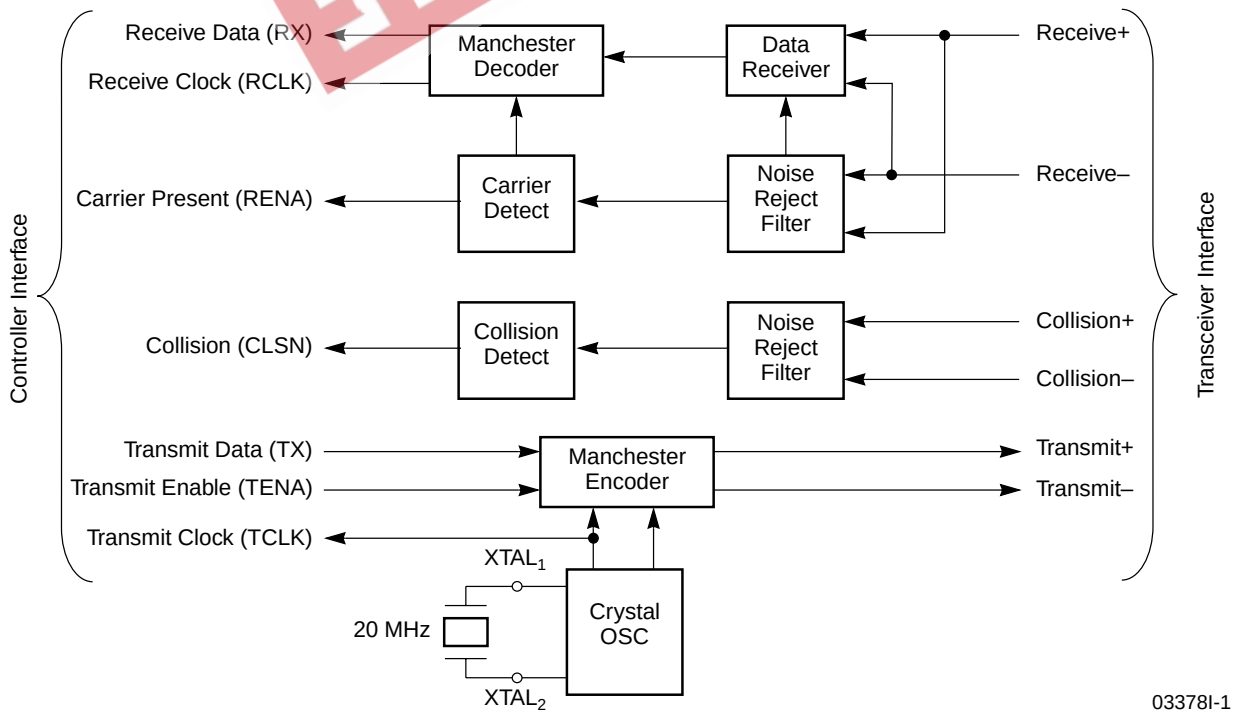
DISTINCTIVE CHARACTERISTICS

- **Compatible with IEEE 802.3/Ethernet/Cheapernet specifications**
- **Crystal/TTL oscillator-controlled Manchester encoder**
- **Manchester decoder acquires clock and data within four bit times with an accuracy of ±3 ns**
- **Guaranteed carrier and collision detection squelch threshold limits**
  - — Carrier/collision detected for inputs greater than –275 mV
  - — No carrier/collision for inputs less than –175 mV
- **Input signal conditioning rejects transient noise**
  - — Transients <10 ns for collision detector inputs
  - — Transients <20 ns for carrier detector inputs
- **Receiver decodes Manchester data with worst case ±19 ns of clock jitter (at 10 MHz)**
- **TTL-compatible host interface**
- **Transmit accuracy +0.01% (without adjustments)**

GENERAL DESCRIPTION

The Am7992B Serial Interface Adapter (SIA) is a Manchester encoder/decoder compatible with IEEE 802.3, Cheapernet, and Ethernet specifications. In an IEEE 802.3/Ethernet application, the Am7992B interfaces the Am7990 Local Area Network Controller for Ethernet (LANCE) to the Ethernet transceiver device, acquires clock and data within four bit times, and decodes Manchester data with worst case ±19 ns phase jitter at 10 MHz. SIA provides both guaranteed signal threshold limits and transient noise suppression circuitry in both data and collision paths to minimize false start conditions.

BLOCK DIAGRAM



03378I-1

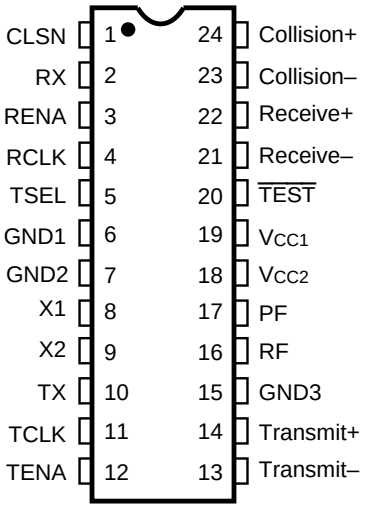
Publication# **03378** Rev: **I** Amendment/**0**
Issue Date: **May 1993**

RELATED PRODUCTS

Part No.	Description
Am7990	Local Area Network Controller for Ethernet (LANCE)
Am7996	IEEE 802.3/Ethernet/Cheapernet/Transceiver
Am79C900	Integrated Local Area Communications Controller™ (ILACC™)

CONNECTION DIAGRAMS

DIP



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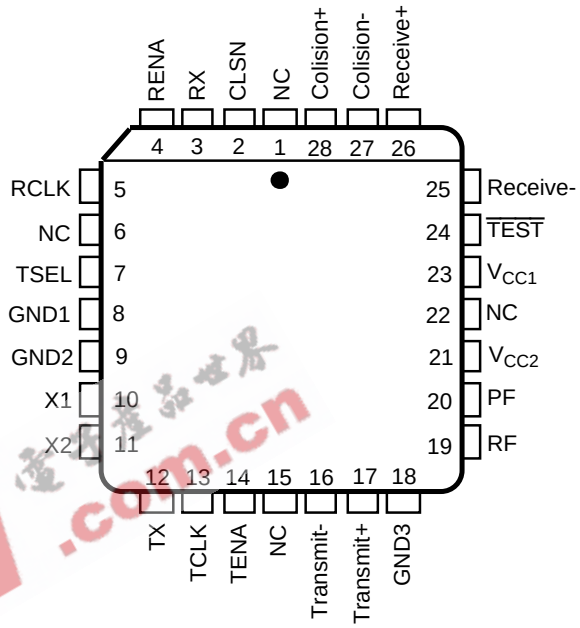
PLCC



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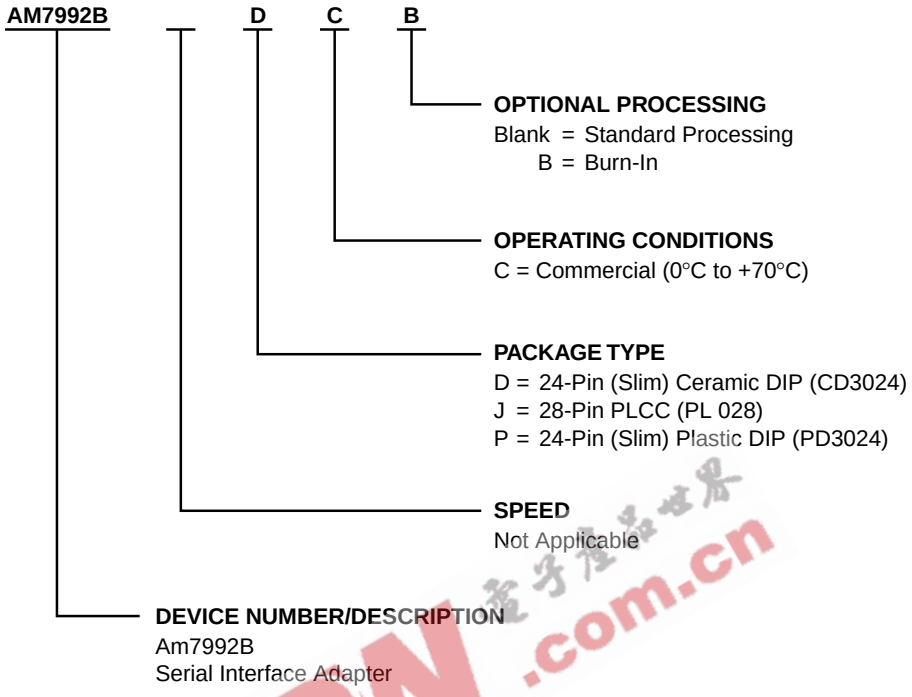
Note:
Pin 1 is marked for orientation.

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (valid combination) is formed by a combination of the elements below.



Valid Combinations	
AM7992B	DC, DCB, JC, JCTR, PC

Valid Combinations

Valid combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

PIN DESCRIPTION

CLSN

Collision (Output, TTL Active HIGH)

Signals at the Collision± terminals meeting threshold and pulse-width requirements will produce a logic HIGH at CLSN output. When no signal is present at Collision±, CLSN output will be LOW.

RX

Receive Data (Output)

A MOS/TTL output, recovered data. When there is no signal at Receive± and $\overline{\text{TEST}}$ is HIGH, RX is HIGH. RX is actuated with RCLK and remains active until RENA is deasserted at the end of the message. During reception, RX is synchronous with RCLK and changes after the rising edge of RCLK. When $\overline{\text{TEST}}$ is LOW, RX is enabled.

RENA

Receive Enable (Output, TTL Active HIGH)

When there is no signal at Receive+, RENA is LOW. Signals meeting threshold and pulse-width "on" requirements will produce a logic HIGH at RENA. When RENA is HIGH, Receive+ signals meeting threshold and pulse-width "off" requirements will produce a LOW at RENA.

RCLK

Receive Clock (Output)

A MOS/TTL output, recovered clock. When there is no signal at Receive± and $\overline{\text{TEST}}$ is HIGH, RCLK is LOW. RCLK is activated 1/4 bit time after the second negative Manchester preamble clock transition at Receive± and remains active until after an end of message. When $\overline{\text{TEST}}$ is LOW, RCLK is enabled and meets minimum pulse-width specifications.

TX

Transmit (Input)

TTL-compatible input. When TENA is HIGH, signals at TX meeting setup and hold time to TCLK will be encoded as normal Manchester at Transmit+ and Transmit–.

- TX HIGH: Transmit+ is negative with respect to Transmit– for first half of data bit cell.
- TX LOW: Transmit+ is positive with respect to Transmit– for first half of data bit cell.

TENA

Transmit Enable (Input)

TTL-compatible input. Active HIGH data encoder enable. Signals meeting setup and hold time to TCLK will allow encoding of Manchester data from TX to Transmit+ and Transmit–.

TCLK

Transmit Clock (Output)

MOS/TTL output. TCLK provides symmetrical HIGH and LOW clock signals at data rate for reference timing of data to be encoded. It also provides clock signals for the controller chip (Am7990—LANCE) and an internal timing reference for receive path voltage-controlled oscillators.

Transmit+, Transmit–

Transmit (Outputs)

A differential line output. This line pair is intended to operate into terminated transmission lines. For signals meeting setup and hold time to TCLK at TENA and TX, Manchester clock and data are outputted at Transmit+/Transmit–. When operating into a 78 Ω terminated transmission line, signaling meets the required output levels and skew for both Ethernet and IEEE 802.3 drop cables.

Receive+, Receive–

Receiver (Inputs)

A differential input. A pair of internally biased line receivers consisting of a carrier detect receiver with offset threshold and noise filtering to detect the line activity, and a data recovery receiver with no offset for Manchester data decoding.

Collision+, Collision–

Collision (Inputs)

A differential input. An internally biased line receiver input with offset threshold and noise filtering. Signals at Collision± have no effect on data-path functions.

TSEL

Transmit Mode Select (Output, Open Collector; Input, Sense Amplifier)

- TSEL LOW: Idle transmit state Transmit+ is positive with respect to Transmit–.
- TSEL HIGH: Idle transmit state Transmit+ and Transmit– are equal, providing "zero" differential to operate transformer-coupled loads.

When connected with an RC network, TSEL is held LOW during transmission. At the end of transmission the open collector output is disabled, allowing TSEL to rise and provide a smooth transmission from logic HIGH to "zero" differential idle. Delay and output return to zero are externally controlled by the RC network at TSEL and Transmit± load inductance.

X_1, X_2

Biased Crystal Oscillator (Input)

X_1 is the input and X_2 is the bypass port. When connected for crystal operation, the system clock that appears at TCLK is half the frequency of the crystal oscillator. X_1 may be driven from an external source of two times the data rate.

RF

Frequency Setting Voltage-Controlled Oscillator (V_{CO}) Loop Filter (Output)

This loop filter output is a reference voltage for the receive path phase detector. It also is a reference for timing noise immunity circuits in the collision and receive enable path. Nominal reference V_{CO} gain is 1.25 TCLK frequency MHz/V.

PF

Receive Path V_{CO} Phase-Locked Loop Filter (Input)

This loop filter input is the control for receive path loop damping. Frequency of the receive V_{CO} is internally limited to transmit frequency ±12%. Nominal receive V_{CO} gain is 0.25 reference V_{CO} gain MHz/V.

$\overline{TEST}$

Test Control (Input)

A static input that is connected to V_{CC} for Am7992B/Am7990 operation and to ground for testing of Receive± path threshold and RCLK output HIGH parameters. When $\overline{TEST}$ is grounded, RX is enabled and RCLK is enabled except during clock acquisition, when RCLK is HIGH.

GND1

High Current Ground

GND2

Logic Ground

GND3

Voltage-Controlled Oscillator Ground

V_{CC1}

High Current and Logic Supply

V_{CC2}

Voltage-Controlled Oscillator Supply

FUNCTIONAL DESCRIPTION

The Am7992B serial interface adapter (SIA) has three basic functions. It is a Manchester encoder/line driver in the transmit path, a Manchester decoder with noise filtering and quick lock-on characteristics in the receive path, and a signal detector/converter (10 MHz differential to TTL) in the collision path. In addition, the SIA provides the interface between the TTL logic environment of the Local Area Network Controller for Ethernet (LANCE) and the differential signaling environment in the transceiver cable.

Transmit Path

The transmit section encodes separate clock and NRZ data input signals meeting the setup and hold time to TCLK at TENA and TX into a standard Manchester II serial bit stream. The transmit outputs (Transmit+/ Transmit–) are designed to operate into terminated transmission lines. When operating into a 78 Ω terminated transmission line, signaling meets the required output levels and skew for IEEE 802.3/Ethernet/ Cheapernet.

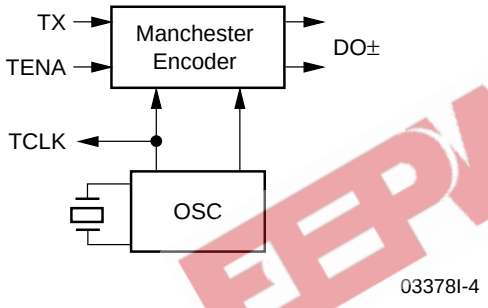


Figure 1. Transmit Section

Transmitter Timing and Operation

A 20 MHz fundamental mode crystal oscillator provides the basic timing reference in the SIA. It is divided by two to create the Transmit Clock reference (TCLK). Both 20 MHz and 10 MHz clocks are fed into the Manchester Encoder to generate the transitions in the encoded data stream. The 10 MHz clock, TCLK, is used by the SIA to internally synchronize Transmit (TX) data and Transmit Enable (TENA). TCLK is also used as a stable bit rate clock by the receive section of the SIA and by other devices in the system (the Am7990 LANCE uses TCLK to drive its internal state machine). The oscillator may use an external 0.005% crystal or an external TTL-level input as a reference, which will achieve a transmit accuracy of 0.01% (no external adjustments are required).

Transmission is enabled when TENA is activated. As long as TENA remains HIGH, signals at TX will be encoded as Manchester and will appear at Transmit+ and Transmit–. When TENA goes LOW, the differential transmit outputs go to one of two idle states determined by the circuit configuration of TSEL:

TSEL HIGH: The idle state of Transmit± yields "zero" differential to operate transformer-coupled loads (see Figure 2, Transmitter Timing—End of Transmission waveform diagram and Typical Performance Curve diagram).

TSEL LOW: In this idle state, Transmit+ is positive to Transmit– (logical HIGH) (see figures and diagrams as referenced above).

The End of Transmission—Return to Zero is determined by the external RX network at TSEL and by the load at Transmit±.

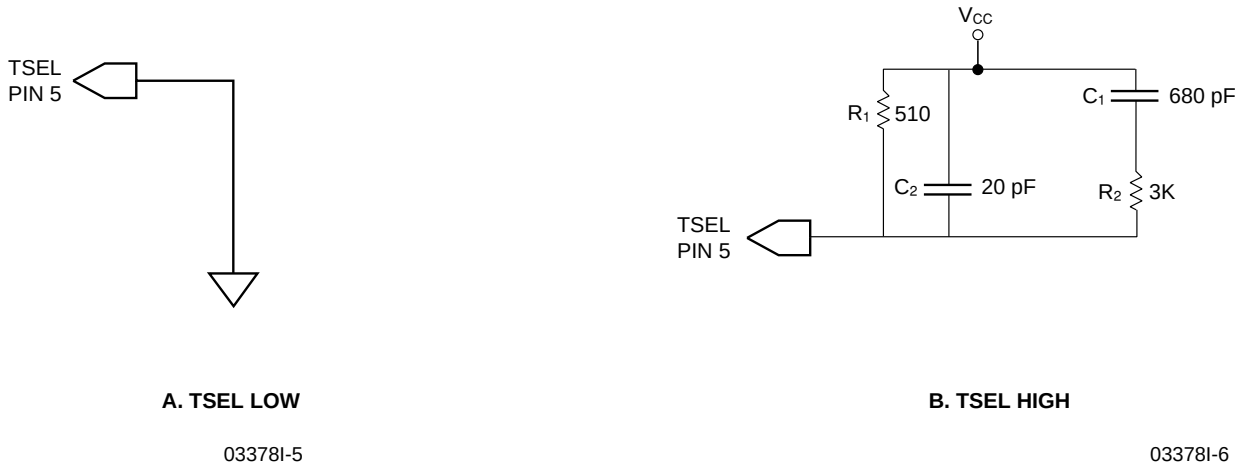


Figure 2. Transmit Mode Select (TSEL) Connection

Figure 3. TTL Clock Driver Circuit for X_1

SIA Oscillator

Specification for External Crystal

When using a crystal to drive the Am7992B oscillator, the following crystal specification should be used to ensure a transmit accuracy of 0.01%:

	Limit			Unit
	Min	Nominal	Max	
Resonant Frequency Error with C_L = 50 pF	–50	0	+50	PPM
Change in Resonant Frequency Temperature with C_L = 50 pF	–40		+40	PPM
Parallel Resonant Frequency with C_L = 50 pF		20		MHz
Motional Crystal Capacitance, C_1		0.022		pF

Some crystal manufacturers have generated crystals to this specification. One such manufacturer is Reeves-Hoffman. Their ordering part number for this crystal is RH#04-20423-312. Another manufacturer is Epson—Part #MA 506-200M-50 pF, which is a surface-mounted crystal.

Specification for External TTL Level

When driving the oscillator from an external clock source, X_2 must be left floating (unconnected). An external clock having the following characteristics must be used to ensure less than +0.5 ns jitter at Transmit+ (see the X_1 Driven from External Source waveform diagram and the TTL Clock Driver Circuit for X_1, Figure 3):

- Clock Frequency: 20 MHz ±0.01%
- Rise/Fall Time (t_R/t_F): <4 ns, monotonic
- X_1 HIGH/LOW Time (t_{HIGH}/t_{LOW}): > 20 ns
- X_1 Falling Edge-to-Falling Edge Jitter: < ±0.2 ns at 1.5 V input

Receiver Path

The principle functions of the receiver are to signal the LANCE that there is information on the receive pair and to separate the incoming Manchester-encoded data stream into clock and NRZ data.

The receiver section (see Figures 4 and 5) consists of two parallel paths. The receive data path is a zero threshold, wide bandwidth line receiver. The carrier path is an offset threshold bandpass-detecting line receiver. Both receivers share common bias networks to allow operation over an input common mode range of 0 V to 5.5 V.

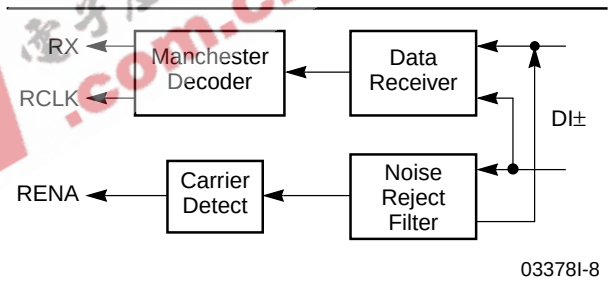


Figure 4. Receiver

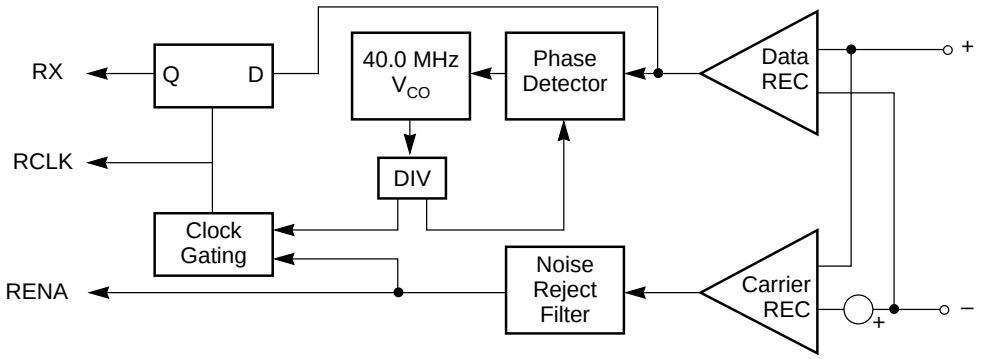


Figure 5. Receiver Section Detail

Input Signal Conditioning

The Carrier Receiver detects the presence of an incoming data packet by discerning and rejecting noise from expected Manchester data. It also controls the stop and start of the phase-locked loop during clock acquisition. In the Am7992B, clock acquisition requires a valid Manchester bit pattern of 1010 to lock on the incoming message (see Receive Timing—Start of Reception Clock Acquisition waveform diagram).

Transient noise pulses less than 20 ns wide are rejected by the Carrier Receiver as noise and DC inputs more positive than –175 mV are also suppressed. Carrier is detected for input signal wider than 45 ns with amplitude more negative than –275 mV. When input amplitude and pulse-width conditions are met at Receive±, RENA is asserted and a clock acquisition cycle is initiated.

Clock Acquisition

When there is no activity at Receive± (receiver is idle), the receive oscillator is phase locked to TCLK. The first negative clock transition (first valid Manchester "0") after RENA is asserted interrupts the receive oscillator and presets the INTRCLK (internal clock) to the HIGH state. The oscillator is then restarted at the second Manchester "0" (bit time 4) and is phase locked to it. As a result, the SIA acquires the clock from the incoming Manchester bit stream in four bit times with a "1010" Manchester bit pattern. The 10 MHz INTRCLK and INTPLLCLK are derived from the internal oscillator, which runs at four times the data rate (40.0 MHz). The three clocks generated internally are utilized in the following manner:

- **INTRCLK:** After clock acquisition, INTRCLK strobes the incoming data at 1/4 bit time. Receive data path sets the input to the data decode register (Figure 5).
- **INTPLLCLK:** At clock acquisition, INTPLLCLK is phase locked to the incoming Manchester clock transition at bit cell center (BCC). The transition at BCC is compared to INTPLLCLK and phase correction is applied to maintain INTRCLK at 1/4 bit time in the Manchester cell.
- **INTCARR:** From start to end of a message, INTCARR is active and establishes RENA turn-off synchronously with RCLK rising edge. Internal carrier goes active when there is a negative transition that is more negative than –275 mV and has a pulse width greater or equal to 45 ns. Internal carrier goes inactive typically 155 ns after the last positive transition at Receive±.

When $\overline{\text{TEST}}$ is strapped LOW, RCLK and RX are enabled 1/4 bit time after clock acquisition in bit cell 5. RX is at HIGH state when the receiver is idle and $\overline{\text{TEST}}$ is strapped HIGH (no RLCK). RX, however, is undefined when clock is acquired and may remain HIGH or change to LOW state whenever RCLK is enabled. At the 1/4 bit time of clock transition in bit cell 5, RCLK makes its first external transition. It also strobes the incoming fifth bit Manchester "1." RX may make a transition after the RCLK rising edge in bit cell 5, but its state is still undefined. The Manchester "1" at bit 5 is clocked to RX output at 1/4 bit time in bit cell 6.

PLL Tracking

After clock acquisition, the INTPLLCLK is compared to the incoming transitions at BCC and the resulting phase error is applied to a correction circuit. This circuit ensures that INTPLLCLK remains locked on the received signal. Individual bit cell phase corrections of the V_{CO} are limited to 10% of the phase difference between BCC and INTPLLCLK. Hence, input data jitter is reduced in RCLK by 10 to 1.

Carrier Tracking and End of Message

The carrier receiver monitors Receive± input after RENA is asserted for an end of message. INTCARR deasserts typically 155 ns to 165 ns after the incoming message transitions positive. This initiates the end of reception cycle. INTCARR is strobed at 3/4 bit time by the falling edge of INTRCLK. The time delay from the

last rising edge of the message to INTCARR deassert allows the last bit to be strobed by RCLK and transferred by the LANCE without an extra bit at the end of the message. When RENA deasserts (see Receive Timing—End of Reception waveform diagrams), a RENA hold-off timer inhibits RENA assertion for at least 120 ns.

Data Decoding

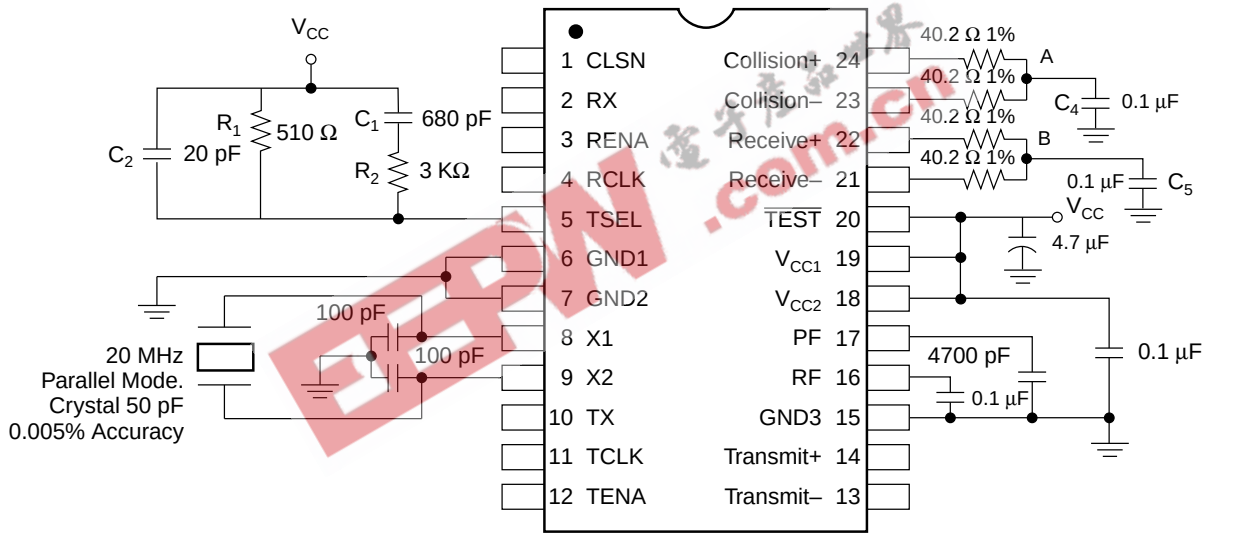
The data receiver is a comparator with clocked output to minimize noise sensitivity to the Receive± inputs. Input error (VIRD) is less than ±35 mV to minimize sensitivity to input rise and fall time. RCLK strobes the data receiver output at 1/4 bit time to determine the value of the Manchester bit and clocks the data out at RX on the following RCLK. The data receiver also generates the signal used for phase detector comparison to the internal Am7992B V_{CO}.

Differential I/O Terminations

The differential input for the Manchester data (Receive±) is externally terminated by two 40.2-ohm ±1% resistors and one optional common-mode bypass capacitor. The differential input impedance, Z_{IDF} and the common-mode input, Z_{ICM}, are specified so that the Ethernet specification for cable termination impedance is met using standard 1% resistor terminators. The Collision± differential inputs are terminated in exactly the same way as the receive inputs (see Figure 6).

Collision Detection

A transceiver detects collisions on the network and generates a 10 MHz signal at the Collision± inputs. This collision signal passes through an input stage that detects signal levels and pulse duration. When the signal is detected by the Am7992B, it sets the CLSN line HIGH. This condition continues for approximately 160 ns after the last LOW-to-HIGH transition on Collision±.



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Notes:

1. *Connect R1, R2, C1, C2 for 0 differential nontransmit. Connect to ground for logic 1 differential nontransmit.*
2. *Pin 20 shown for normal device operation.*
3. *The inclusion of C4 and C5 is necessary to reduce the common-mode loading on certain transceivers that are direct coupled.*
4. *C2 reduces the amount of noise from the power supply and crosstalk from RCLK that can be coupled from TSEL through to the transmit± outputs.*

Figure 6. External Component Diagram

Jitter Tolerance Definition and Test

The Receive Timing—Start of Reception Clock Acquisition waveform diagram shows the internal timing relationships implemented for decoding Manchester data in the Am7992B. The Am7992B utilizes a clock capture circuit to align its internal data strobe with an incoming bit stream. The clock acquisition circuitry requires four valid bits with the values 1010. Clock is phase locked to the negative transition at BCC of the second “0” in the pattern.

Since data is strobed at 1/4 bit time, Manchester transitions that shift from their nominal placement through 1/4 bit time will result in improperly decoded data. For IEEE 802.3/Ethernet, this results in the loss of a message. With this as the criterion for an error, a definition of “jitter handling” is:

> That peak deviation from nominal input transition approaching or crossing 1/4 bit cell position for which the Am7992B will properly decode data.

Four events of signal are needed to adequately test the ability of the Am7992B to decode data properly from the Manchester bit stream. For each of the four events, two time points within a received message are tested (See Input Jitter Timing Waveforms):

1. Jitter tolerance at clock acquisition, the measure of clock capture (case 1–4).
2. Jitter tolerance within a message after the analogue PLL has reduced clock acquisition error to a minimum (case 5–8).

The four events to test are shown in the Input Jitter Timing Waveform diagram. They are:

1. BCC jitter for a 01-bit pattern
2. BCC jitter for a 10-bit pattern
3. BCB jitter for an 11-bit pattern
4. BCB jitter for an X0-bit pattern

The test signals utilized to jitter the input data are artificial in that they may not be realizable on networks (examples are cases 2, 3, and 4 at clock acquisition). However, each pattern relates to setup and hold time measurements for the data decode register (Figure 5).

Receive+ and Receive– are driven with the inputs shown to produce the zero crossing distortion at the differential inputs for the applicable test. Cases 4 and 8 require only a single zero to implement when tested at the end of message.

Levels used to test jitter are within the common-mode and differential-mode ranges of the receive inputs and also are available from automatic test equipment. It is assumed that the incoming message is asynchronous with the local TCLK frequency for the Am7992B. This ensures that proper clock acquisition has been established with random phase and frequency error in incoming messages. An additional condition placed on the jitter tolerance test is that it must meet all test requirements within 10 ms after power is applied. This forces the Am7992B crystal oscillator to start and lock the analog PLL to within acceptable limits for receiving from a cold start.

Case 1 of the test corresponds to the expected Manchester data at clock acquisition, and average values for clock leading jitter tolerance are 21.5 ns. For cases 5 through 8, average values are 24.4 ns. Cases 5 through 8 are jittered at bit times 55 or 56 as applicable. The Am7992B, then, has on average 0.6 ns static phase error for the noise-free case.

APPLICATION

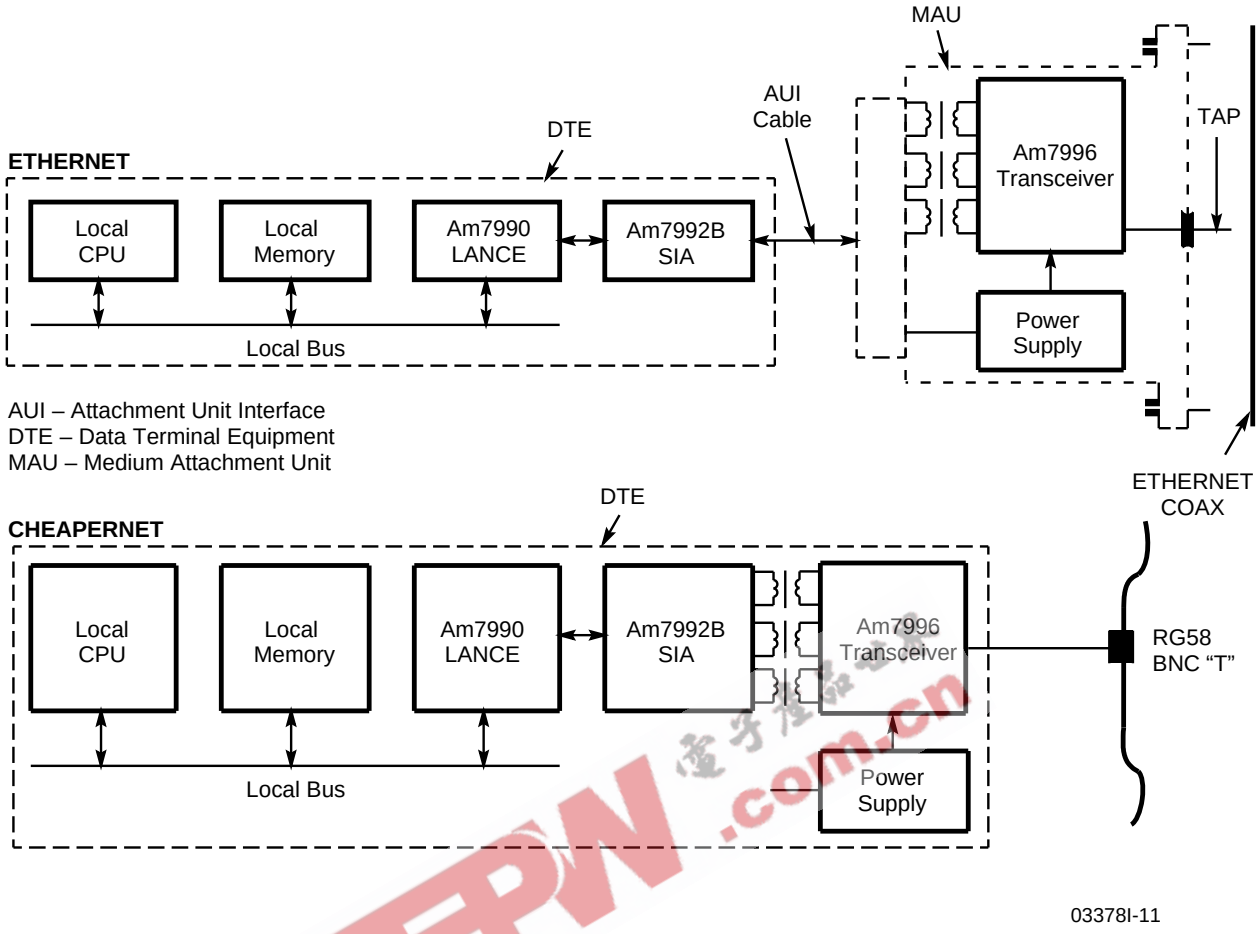


Figure 7. Typical ETHERNET Node

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . 0°C to +70°C

Supply Voltage Continuous . . . . . +7.0 V

DC Voltage Applied to Outputs . . . –0.5 V to V_{CC} Max

DC Input Voltage (Logic Inputs) . . . . . +5.5 V

DC Input Voltage (Receive±/Collision±) . . . . . –6 V to +16 V

Transmit± Output Current . . . . . –50 mA to +25 mA

DC Output Current, Into Outputs . . . . . 100 mA

DC Input Current (Logic Inputs) . . . . . ±30 mA

Transmit± Applied Voltage . . . . . 0 V to +16 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_C) . . . . . 0°C to +70°C

Supply Voltage (V_{CC}) . . . . . +5.0 V ±10%

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Com'l Min	Com'l Max	Unit
V_{OH}	Output HIGH Voltage RX, RENA, CLSN, TCLK, RCLK	I_{OH} = –1.0 mA, V_{CC} = Min		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA, V_{CC} = Min			0.5	V
	RCLK, TSEL, TCLK, RENA, RX, CLSN	I_{OL} = 1 mA, V_{CC} = Min			0.4	V
V_{OD}	Differential Output Voltage TX+ > TX– for V_O	R_L = 78 Ω		550	770	mV
	(Transmit+) – (Transmit–) TX+ < TX– for $\overline{V_O}$			–550	–770	mV
$V_{OD\ OFF}$	Transmit Differential Output Idle Voltage	V_{CC} = Min, R_L = 78 Ω	(Note 1)	–20	20	mV
$I_{OD\ OFF}$	Transmit Differential Output Idle Current	TSEL = HIGH	(Note 2)	–0.5	0.5	mA
V_{CMT}	Transmit Output Common-Mode Voltage	R_L = 78 Ω, V_{CC} = Min		0	5	V
V_{ODI}	Transmit Differential Output Voltage Imbalance $\lvert\lvert V_O\rvert - \lvert\overline{V_O}\rvert\rvert$		(Note 1)		20	mV
V_{IH}	Input HIGH Voltage TX, TENA			2.0		V
I_{IH}	Input HIGH Current TX, TENA, $\overline{TEST}$	V_{CC} = Max, V_{IN} = 2.7 V			+50	µA
V_{IL}	Input LOW Current TX, TENA				0.8	V
I_{IL}	Input LOW Current TX, TENA, $\overline{TEST}$	V_{CC} = Max, V_{IN} = 0.4 V			–400	µA
V_{IRD}	Differential Input Threshold (Receive Data)	V_{CM} = 0 V, (Note 4)	Ceramic Package	–35	+35	mV
			Plastic Package	–65	+65	mV
V_{IRVD}	Differential Mode Input Voltage Range (Receive ±/Collision ±)	(Note 3)		–1.5	+1.5	V
V_{IRVC}	Receive ± and Collision ± Common Mode Voltage	(Note 2)		0	5.5	V
V_{IDC}	Differential Input Threshold to Detect Carrier	V_{CM} = 0 V (Note 4)		–175	–275	mV
I_{CC}	Power Supply Current	V_{CC} = Max (Note 5)			180	mA
V_{IB}	Input Breakdown Voltage (TX, TENA, $\overline{TEST}$)	I_I = 1 mA, V_{CC} = Max		5.5		V
V_{IC}	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min			–1.2	V
V_{ODP}	Undershoot Voltage on Transmit Return to Zero (End of Message)	(Note 3)			–100	mV
I_{SC}	Short Circuit Current RCLK, RX, TCLK, CLSN, RENA	V_{CC} = Max (Note 6)		–40	–150	mA
R_{IDF}	Differential Input Resistance	V_{CC} = 0 to Max (Note 3)		6		kΩ
R_{ICM}	Common Mode Input Resistance	V_{CC} = 0 to Max (Note 3)		1.5		kΩ
V_{ICM}	Receive and Collision Input Bias Voltage	I_{IN} = 0, V_{CC} = Max		1.5	4.2	V
I_{ILD}	Receive and Collision Input LOW Current	V_{IN} = –1 V, V_{CC} = Max			–1.64	mA
I_{IHD}	Receive and Collision Input HIGH Current	V_{IN} = 6 V, V_{CC} = Min			+1.10	mA
I_{IHZ}	Receive and Collision Input HIGH Current Power Off	V_{CC} = 0, V_{IN} = +6 V			1.86	mA
I_{IHX}	Oscillator (X1) Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max			+800	µA
I_{ILX}	Oscillator (X1) Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max			–1.2	mA
V_{IHX}	Oscillator (X1) Input HIGH Voltage	(Note 3)		2.0		V
V_{ILX}	Oscillator (X1) Input LOW Voltage	(Note 3)			0.8	V

Note:

See notes following Switching Characteristics table.

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified

No.	Parameters	Description	Test Conditions	Min	Max	Unit
Receiver Specification						
1	t_{RCT}	RCLK Cycle Time	(Note 8)	85	118	ns
2	t_{RCH}	RCLK HIGH Time		38		ns
3	t_{RCL}	RCLK LOW Time		38		ns
4	t_{RCR}	RCLK Rise Time			8	ns
5	t_{RCF}	RCLK Fall Time			8	ns
6	t_{RDR}	RX Rise Time			8	ns
7	t_{RDF}	RX Fall Time			8	ns
8	t_{RDH}	RX Hold Time (RCLK ↑ to RX Change)		5		ns
9	t_{RDS}	RX Prop Delay (RCLK ↑ to RX Stable)			25	ns
10	t_{DPH}	RENA Turn-On Delay (V_{IDC} Max on Receive ± to $RENA_H$)			80	ns
11	t_{DPO}	RENA Turn-On Delay (V_{IDC} Min on Receive ± to $RENA_L$)	(Note 9)		300	ns
12	t_{DPL}	RENA LOW Time	(Note 10)	120		ns
13	t_{RPWR}	Receive ± Input Pulse Width to Reject (|Input| > |V_{IDC} Max|)	(Note 4)		20	ns
14	t_{RPWO}	Receive ± Input Pulse Width to Turn-On (|Input| > |V_{IDC} Max|)		45		ns
15	t_{RLT}	Decoder Acquisition Time			450	ns
16	t_{REDH}	RENA Hold Time (RCLK ↑ to $RENA_L$)		40	80	ns
17	t_{RPWN}	Receive ± Input Pulse Width to Not Turn-Off INTCARR			165	ns
Collision Specification						
18	t_{CPWR}	Collision ± Input Pulse Width to Not Turn-On CLSN (|Input| > |V_{IDC} Min|)	(Note 4)		10	ns
19	t_{CPWO}	Collision ± Input Pulse Width to Turn-On CLSN (|Input| > |V_{IDC} Max|)		26		ns
20	t_{CPWE}	Collision ± Input Pulse Width to Turn-Off CLSN (|Input| > |V_{IDC} Max|)		160		ns
21	t_{CPWN}	Collision ± Input Pulse Width to Not Turn-Off CLSN (|Input| < |V_{IDC} Max|)			80	ns
22	t_{CPH}	CLSN Turn-On Delay (V_{IDC} Max on Collision ± to $CLSN_H$)			50	ns
23	t_{CPO}	CLSN Turn-Off Delay (V_{IDC} Max on Collision ± to $CLSN_L$)			160	ns

SWITCHING CHARACTERISTICS (continued)

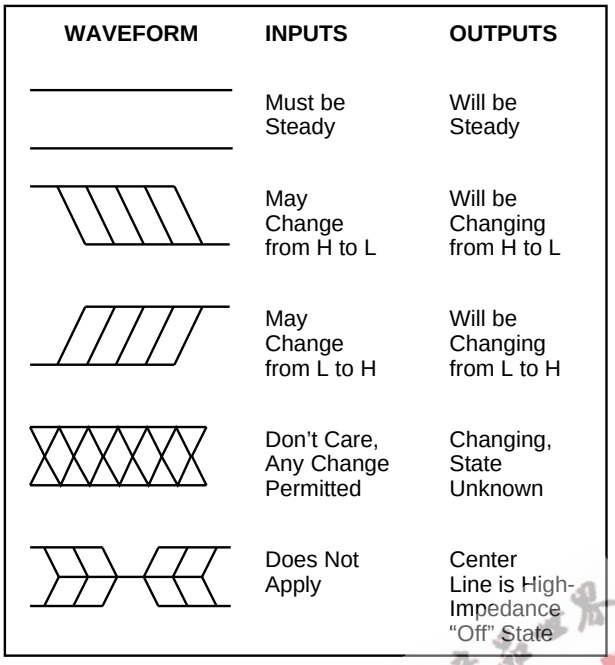
No.	Parameters	Description	Test Conditions	Min	Max	Unit
Transmitter Specification						
24	t_{TCL}	TCLK LOW Time	(Note 11)	45		ns
25	t_{TCH}	TCLK HIGH Time		45		ns
26	t_{TCR}	TCLK Rise Time			8	ns
27	t_{TCF}	TCLK Rise Time			8	ns
28	t_{TDS}, t_{TES}	TX and TENA Setup Time to TCLK	(Note 1)	5		ns
29	t_{TDH}, t_{TEH}	TX and TENA Hold Time to TCLK		5		ns
30	t_{TOCE}	Transmit ± Output, (Bit Cell Center to Edge)		49.5	50.5	ns
31	t_{OD}	TCLK HIGH to Transmit ± Output			100	ns
32	t_{TOR}	Transmit ± Output Rise Time	20% – 80%		4	ns
33	t_{TOF}	Transmit ± Output Fall Time			4	ns
34	t_{XTCH}	X1 to TCLK Propagation Delay for HIGH	(Notes 7 & 12)	5	18	ns
35	t_{XTCL}	X1 to TCLK Propagation Delay for LOW		5	18	ns
36	t_{EJ1}	Clock Acquisition Jitter Tolerance	V_{CC} = 5.0 V (Note 1)	16	21.5	ns
37	t_{EJ51}	Jitter Tolerance After 50 Bit Times	V_{CC} = 5.0 V (Note 1)	19	24.4	ns

**Min = 4.5 V, Max = 5.5 V, T_{OSC} = 50 ns; in production test, all differential input test conditions are done single-ended, non-V_{IRD} levels are forces on DUT for waveform swing (levels chosen are due to tester limitations) and a distortion-free preamble is applied to Receive± inputs.*

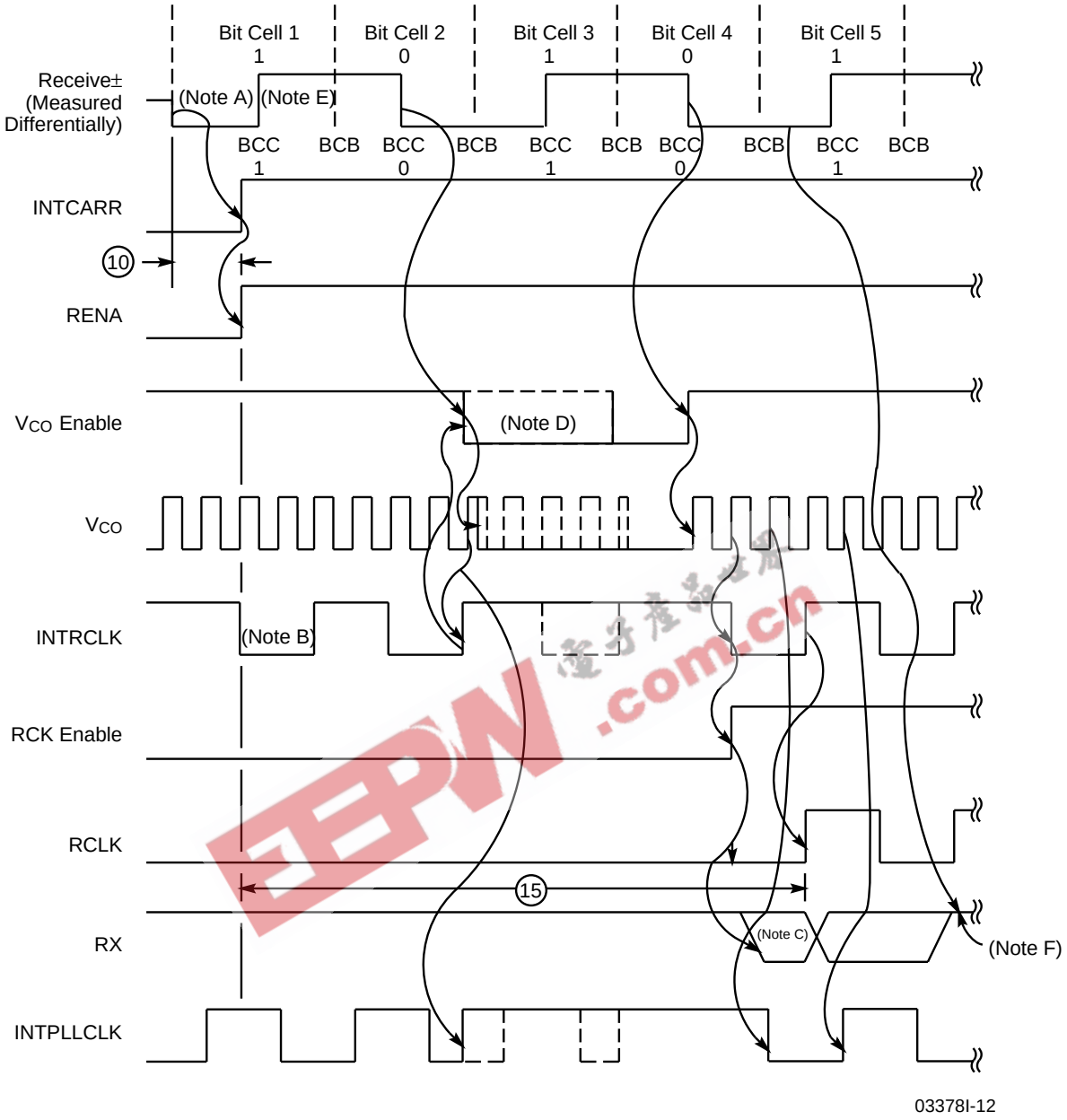
Notes:

1. *Tested but to values in excess of limits. Test accuracy not sufficient to allow screening guardbands.*
2. *Correlated to other tested parameter: I_{OD} OFF = V_{OD} OFF/R_L.*
3. *Not tested.*
4. *Test done by monitoring output functionally.*
5. *Receive, Collision and Transmit functions are inactive: X1 driven by 20 MHz.*
6. *Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.*
7. *TCLK changes state on X1 rising edge, but initial state of TCLK is not defined. When TENA is High, TX data is Manchester encoded on the falling edge of X1 after the rising edge of TCLK.*
8. *Assumes 50 pF capacitance loading on RCLK and RX.*
9. *Test is done only for last BIT = 1, which is worst case.*
10. *Test done from 0.8 V of falling to 2.0 V of rising edge.*
11. *Test correlated to T_{TCH}.*
12. *Measured from 50% point of X1 driving the input in production test.*

KEY TO SWITCHING WAVEFORMS



SWITCHING WAVEFORMS



Notes:

A. Minimum Width > 45 ns.

B. RCLK = INTRCLK when $\overline{\text{TEST}}$ LOW.

C. RX undefined until bit time 5 (1st decoded bit).

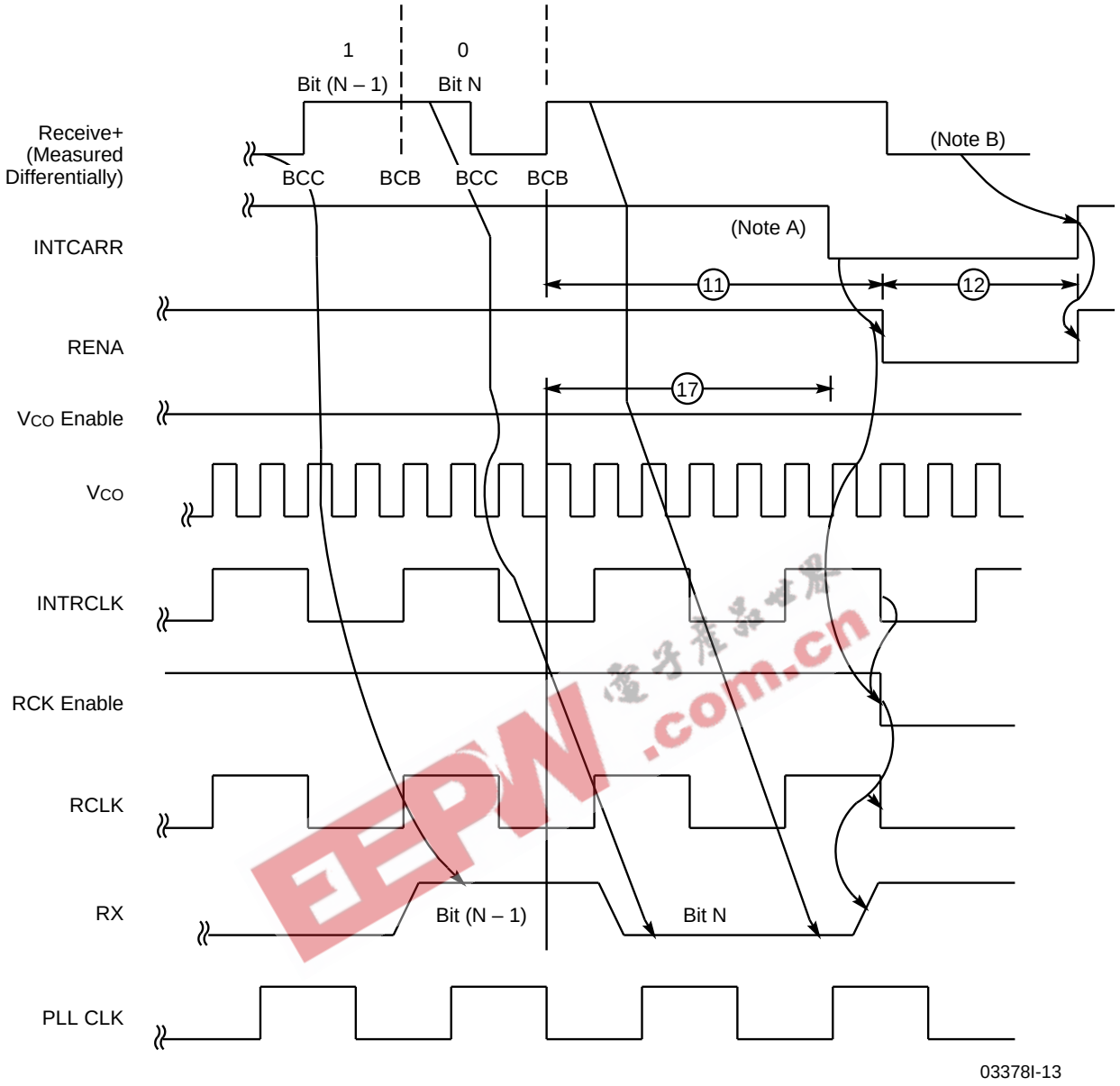
D. Oscillator Interrupt may occur at 2nd INTRCLK after Bit 2 Clock Transition.

E. Timing Diagram does not include Internal Propagation Delays.

F. First valid data at RX (Bit 5).

Receive Timing – Start of Reception Clock Acquisition

SWITCHING WAVEFORMS



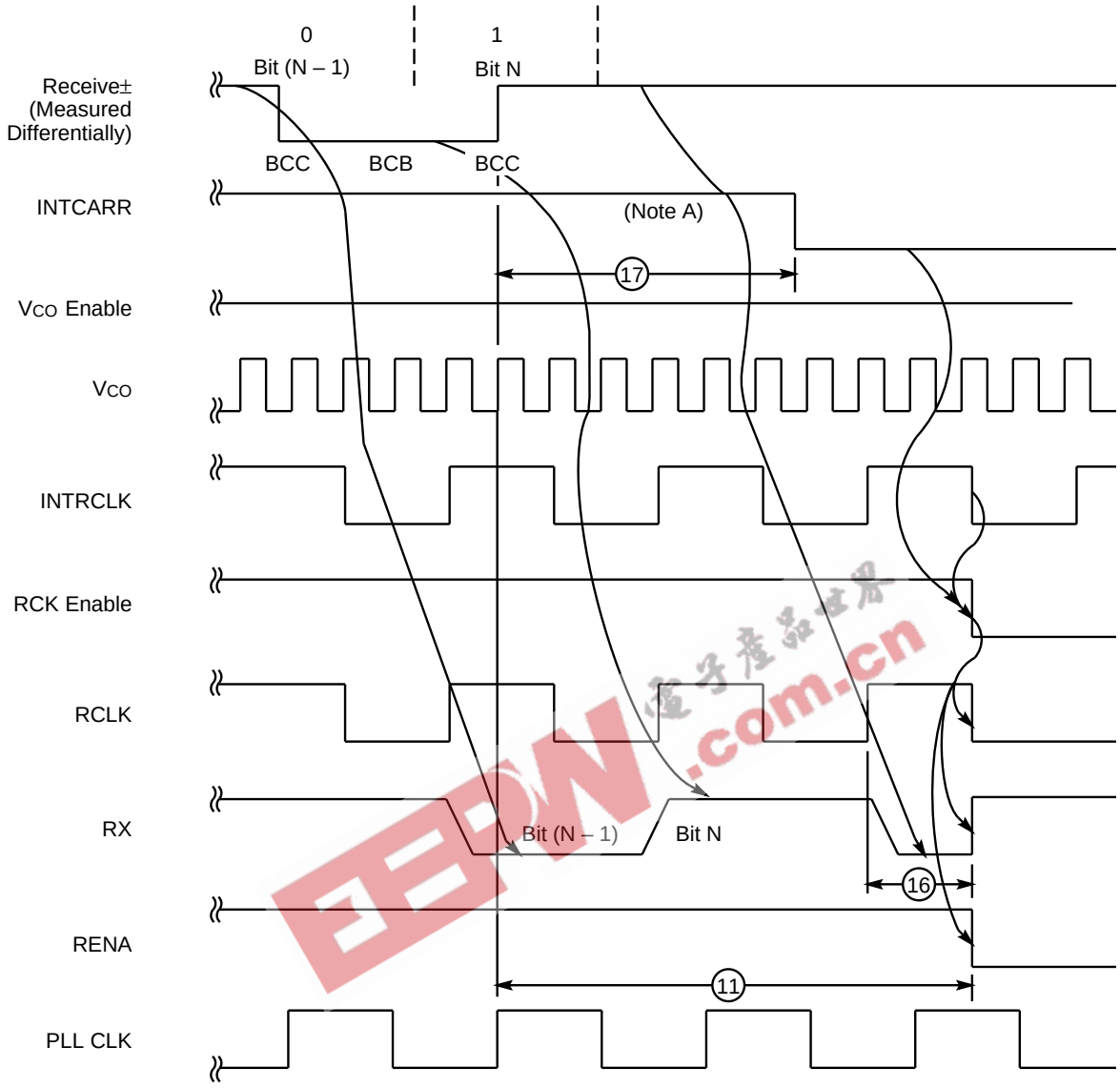
Notes:

A. INTCARR deasserts 1.55 bit times after last Receive± Rising Edge.

B. Start of Next Packet.

Receive Timing – End of Reception (Last Bit = 0)

SWITCHING WAVEFORMS

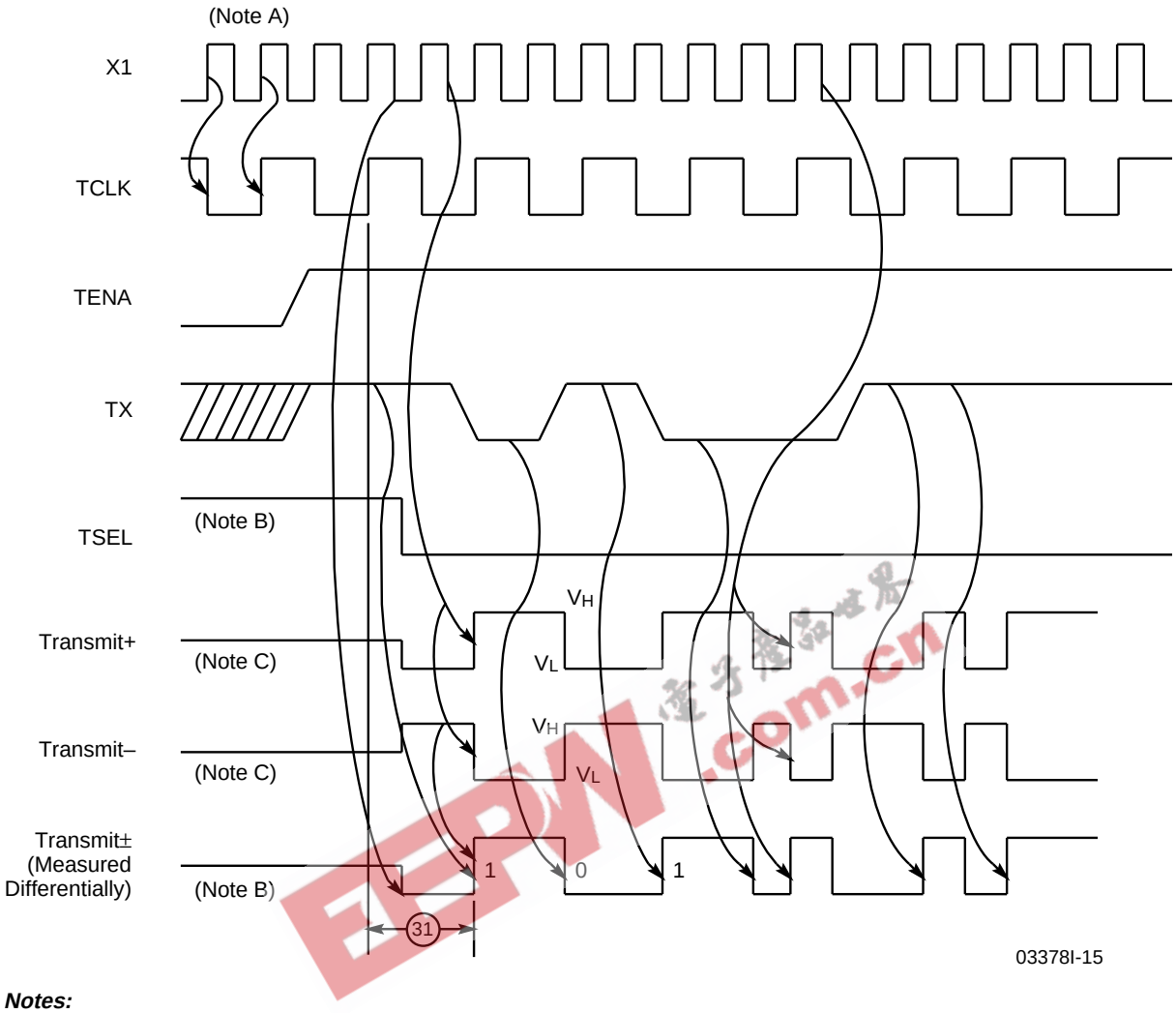


Note:

A. INTCARR deasserts 1.55 bit times after last Receive± Rising Edge.

Receive Timing – End of Reception (Last Bit = 1)

SWITCHING WAVEFORMS



Notes:

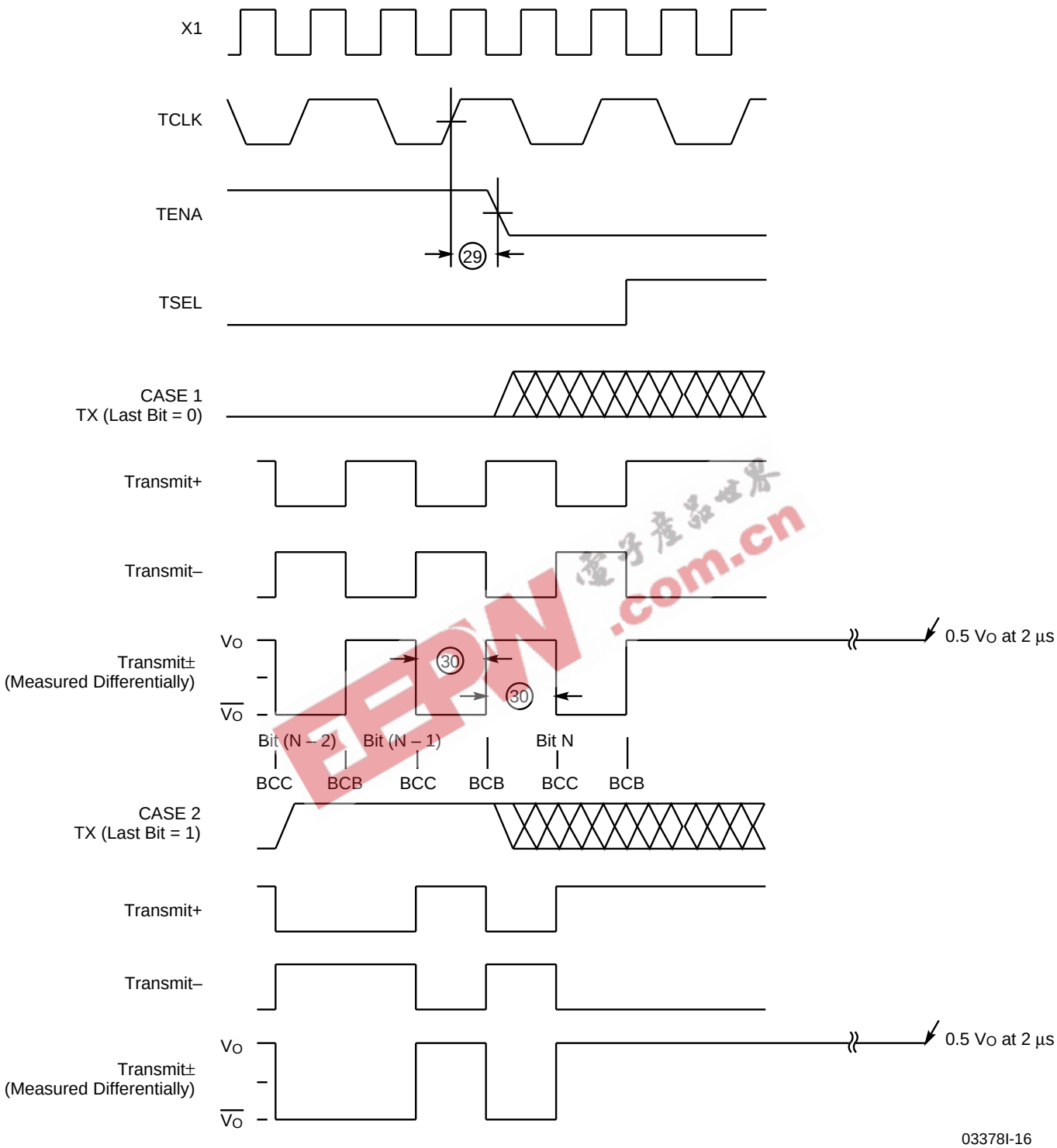
A. X1 20 MHz Sine Wave from Crystal Oscillator or driven with X1 driven from External Source Waveform.

B. TSEL connected as shown in Figure 2B. For Figure 2A, Transmit+ is HIGH when TENA is LOW.

C. When Idle Transmit± Zero Differential is 1/2 (V_H + V_L).

Transmit Timing – Start of Packet

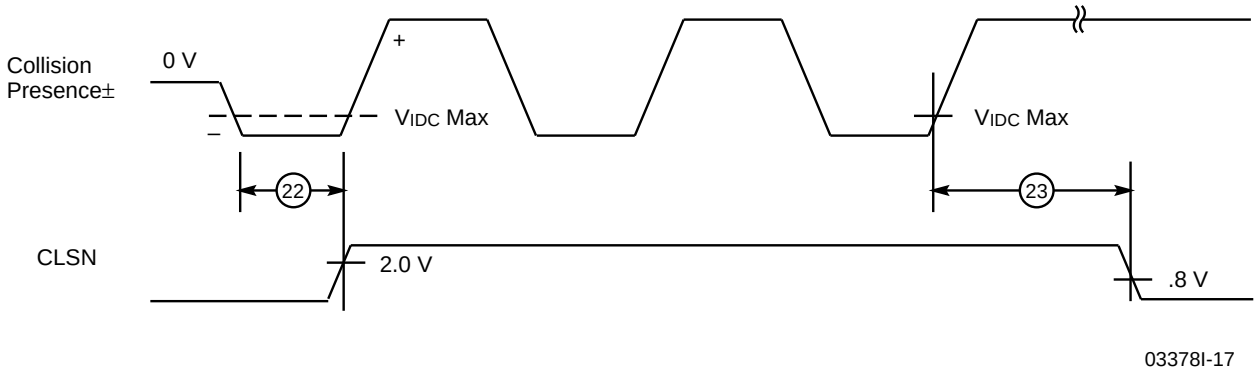
SWITCHING WAVEFORMS



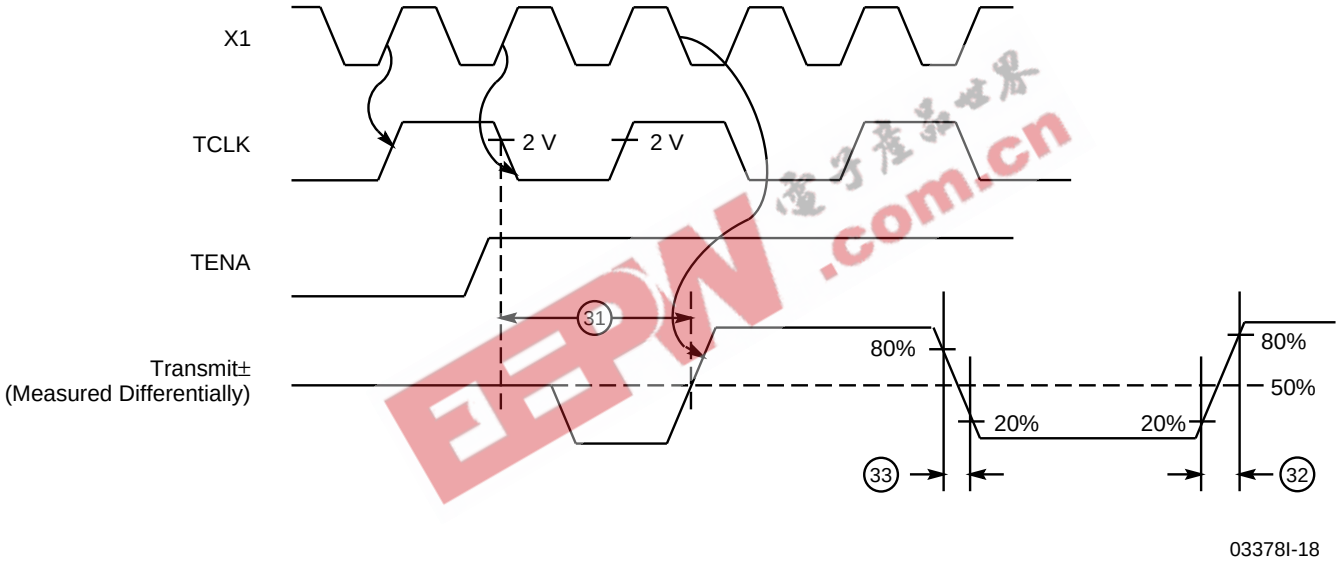
Transmit Timing – End of Transmission*

**TSEL Components (see Figure 2B).*
See Typical Performance Curve for Response at End of Transmission with Inductive Loads.

SWITCHING WAVEFORMS

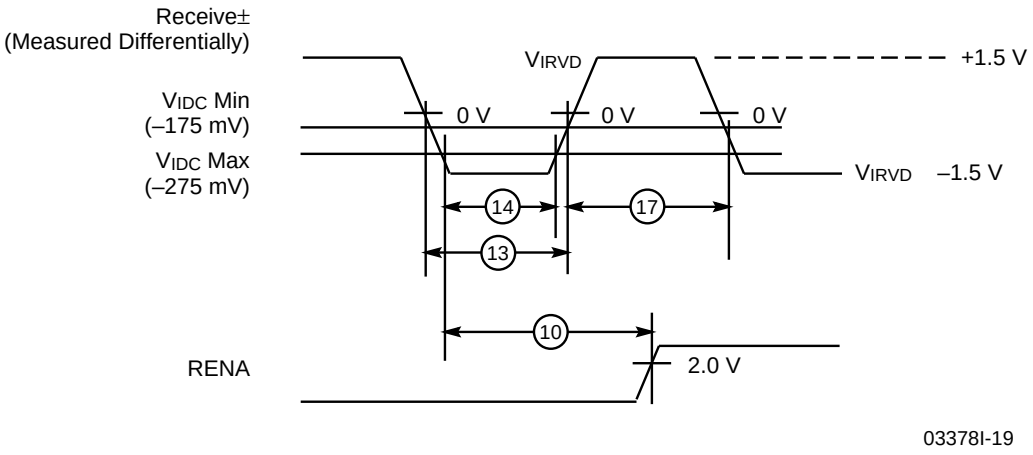


Collision Timing

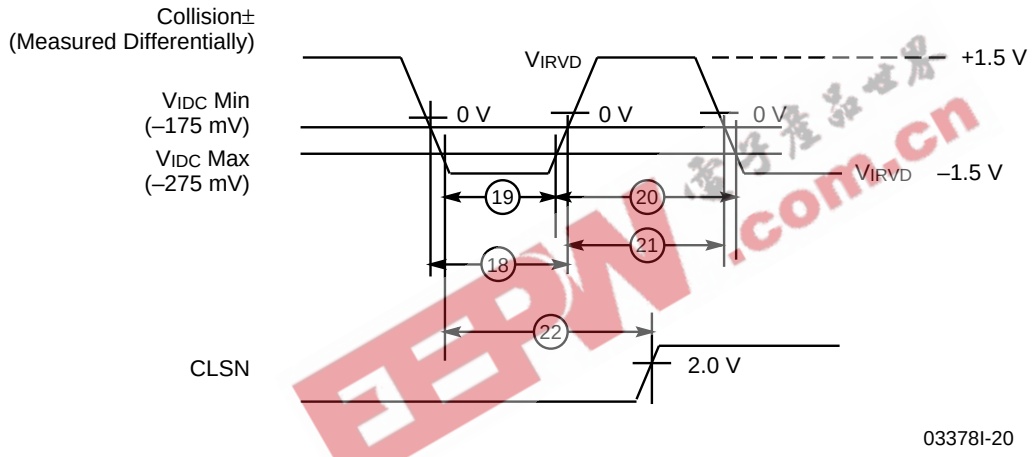


Transmit Timing (at start of packet)

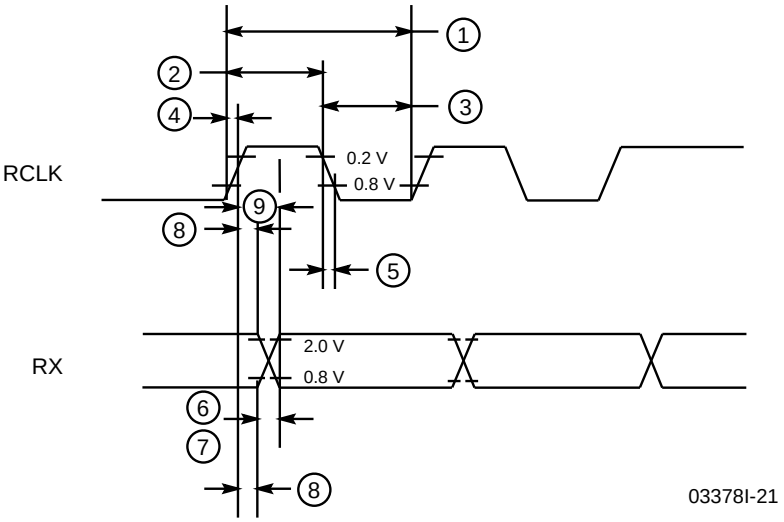
SWITCHING WAVEFORMS



Receive± Input Pulse Width Timing

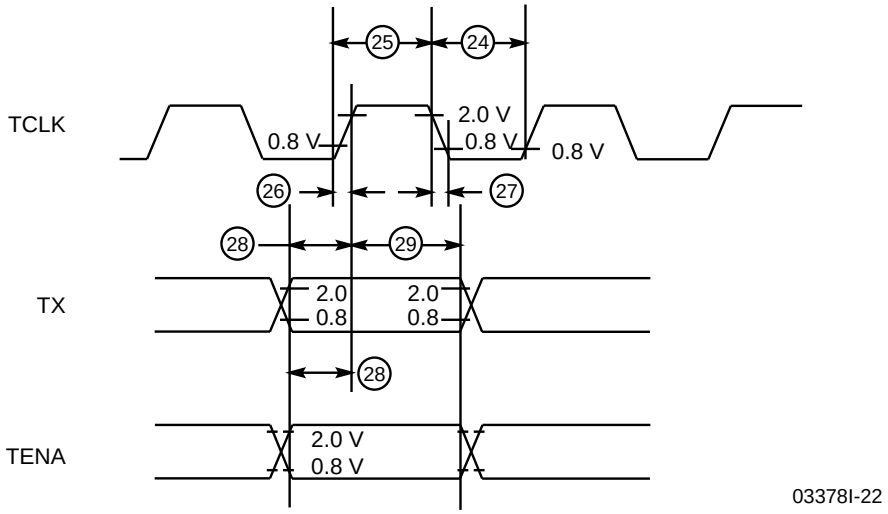


Collision± Input Pulse Width Timing

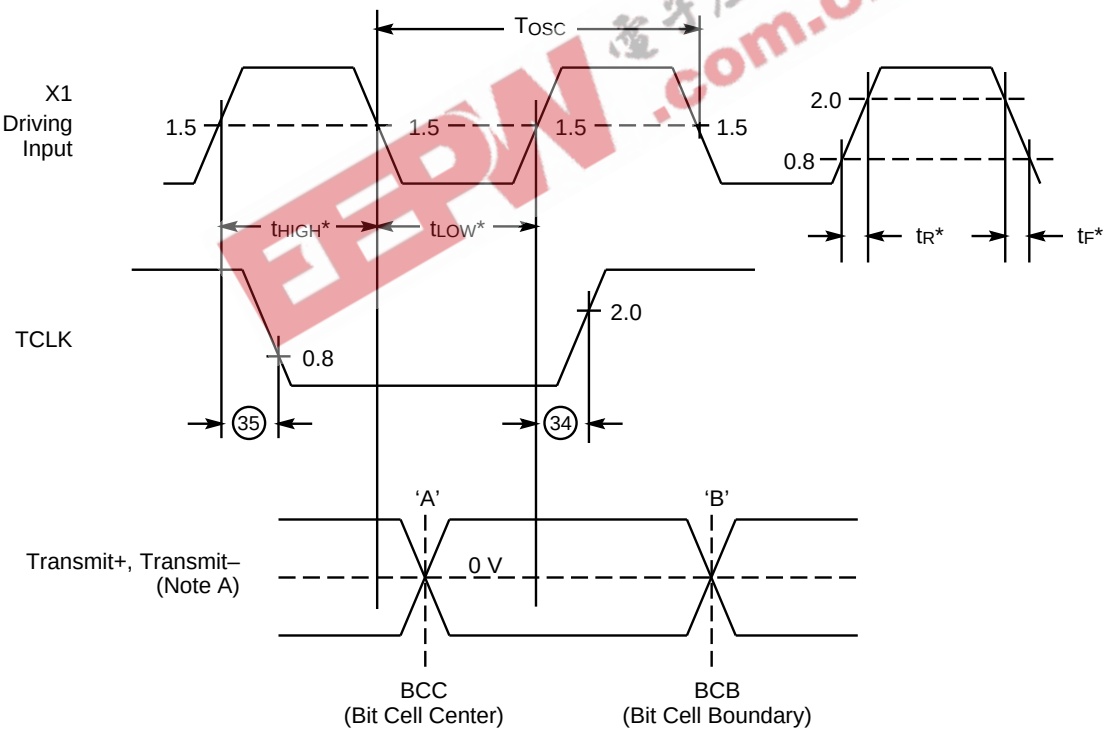


RCLK and RX Timing

SWITCHING WAVEFORMS



TCLK and TX Timing



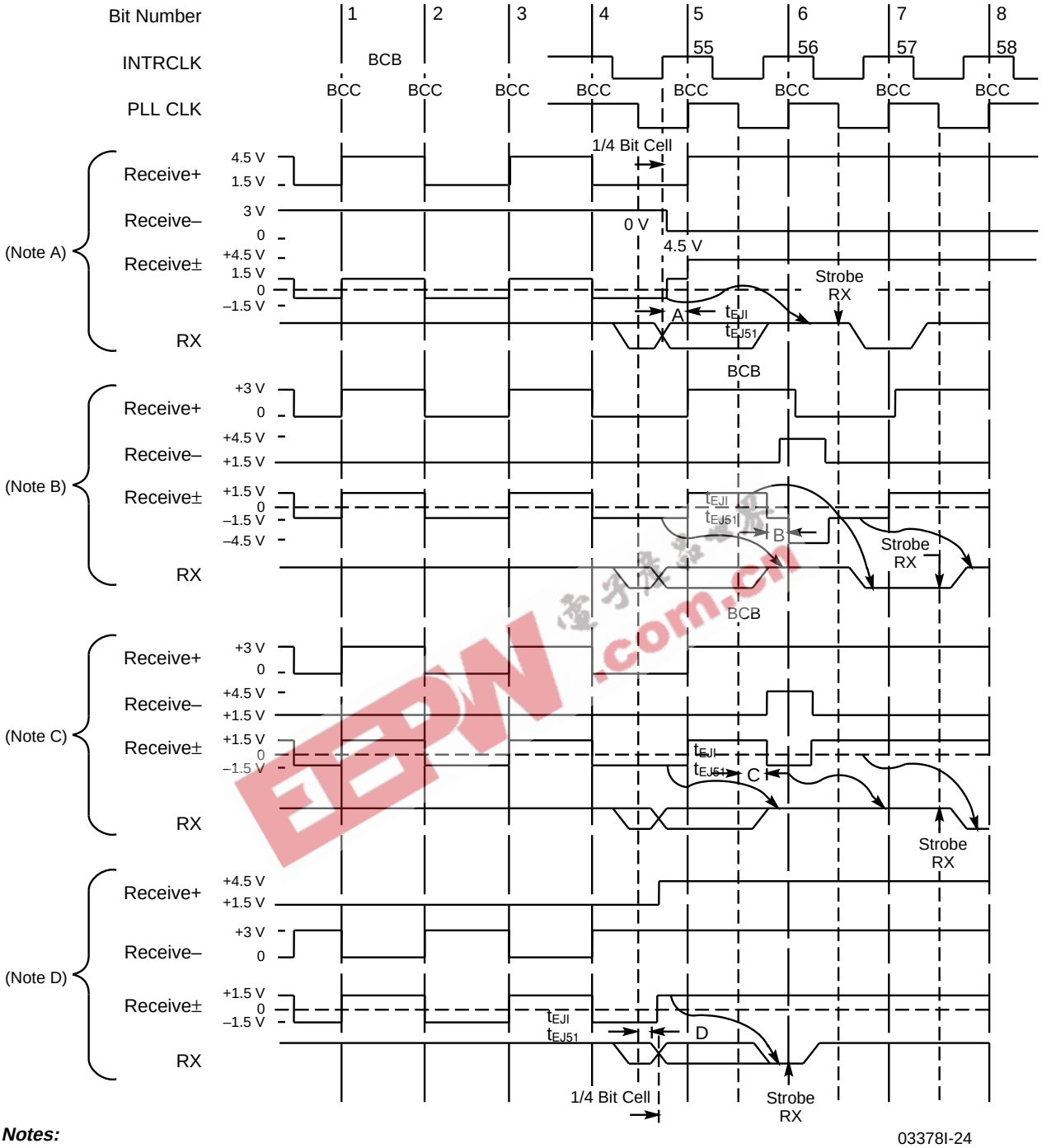
Note:

A. Encode Manchester clock transition (BCC) at Point 'A' and bit cell edge (BCB) at point 'B'.

**See Specification for External TTL Level in Functional Description section.*

X1 Driven from External Source

SWITCHING WAVEFORMS



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Notes:

A. ***Case 1, 5 Data Bit Pattern 0, 1***
Rising clock edge moved toward 1/4 bit cell RCLK data strobe. Case 1 uses bit 5, Case 5 uses bit 55.

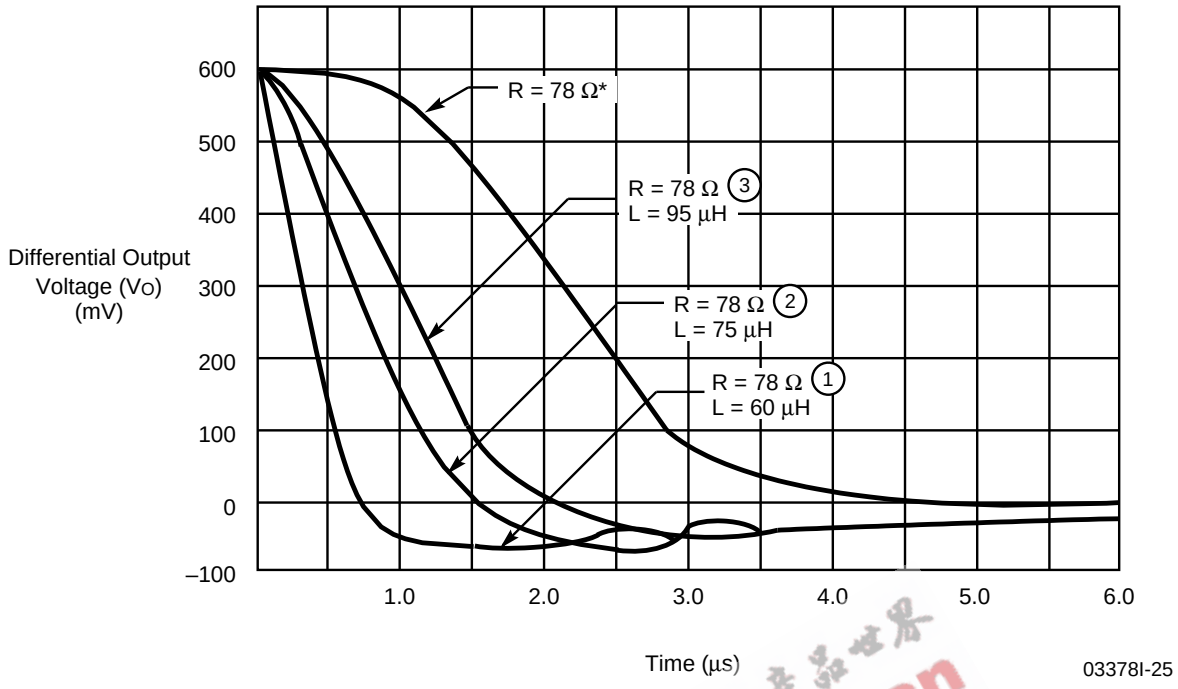
B. ***Case 2, 6 Data Bit Pattern 1, 0***
Falling clock edge moved toward 1/4 bit cell RCLK data strobe. Case 2 uses bit 6, Case 6 uses bit 56.

C. ***Case 3, 7 Data Bit Pattern 1, 1***
Falling bit cell edge moved toward 1/4 bit cell RCLK data strobe. Case 3 uses bit 6, Case 7 uses bit 56.

D. ***Case 4, 8 Data Bit Pattern X, 0***
Rising bit cell edge moved toward 1/4 bit cell RCLK data strobe. Case 4 uses bit 5, Case 8 uses bit 55.

Input Jitter Timing

TYPICAL PERFORMANCE CURVE

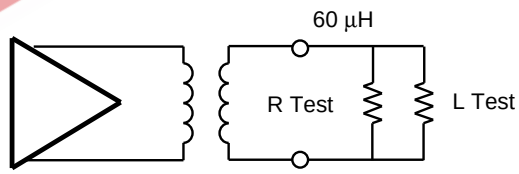


End of Transmission – Differential Output Voltage*

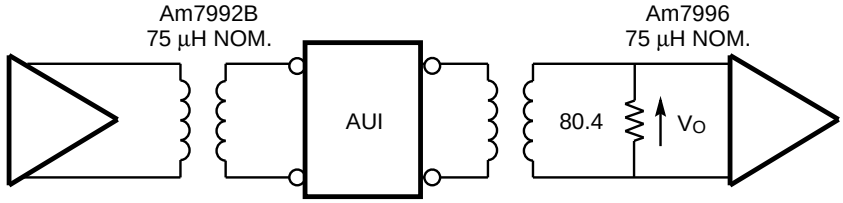
**Equivalent Load:*

Notes:

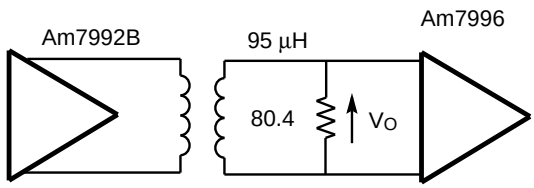
1. *802.3 Test Load:*



2. *802.3 10BASE5 Network Connection:*



3. *802.3 10BASE2 Network Connection:*



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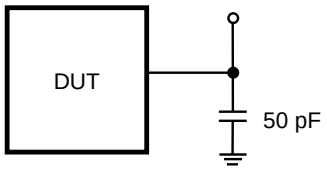
SWITCHING TEST CIRCUITS



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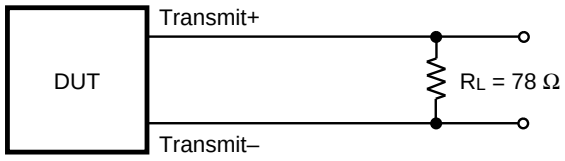
A. Test Load for RX, RENA, RCLK, TCLK, CLSN



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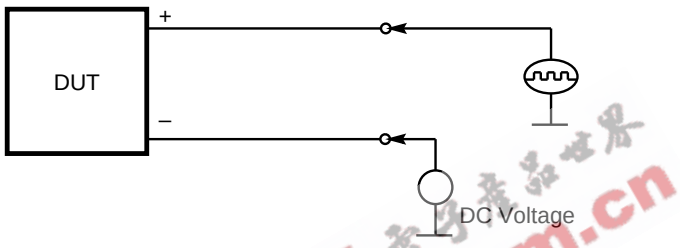
B. Transmit± Output



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C. Receive± and Collision± Input