

# Am9128

## 2048x8 Static RAM



### DISTINCTIVE CHARACTERISTICS

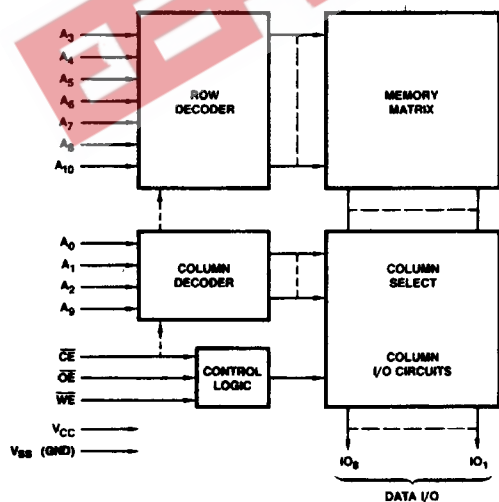
- Logic voltage levels compatible with TTL
- Three-state output buffers and common I/O
- I<sub>CC</sub> Max., as low as 100 mA
- t<sub>AA</sub>/t<sub>ACS</sub> as low as 70 ns
- Power-Down mode (I<sub>SB</sub> as low as 15 mA)

### GENERAL DESCRIPTION

The Am9128 is a 16,384-bit Static Random Access Read-write Memory organized as 2048 words of 8 bits. It uses fully static circuitry, requiring no clocks or refresh to operate. Directly TTL-compatible inputs and outputs and operation from a single +5 V supply simplify system

designs. Common data I/O pins using three-state outputs are provided. The Am9128 is available in an industry-standard 24-pin DIP package with 0.6-inch pin row spacing. The Am9128 uses the JEDEC standard pinout for byte-wide memories (compatible to 16K EPROMs).

### BLOCK DIAGRAM



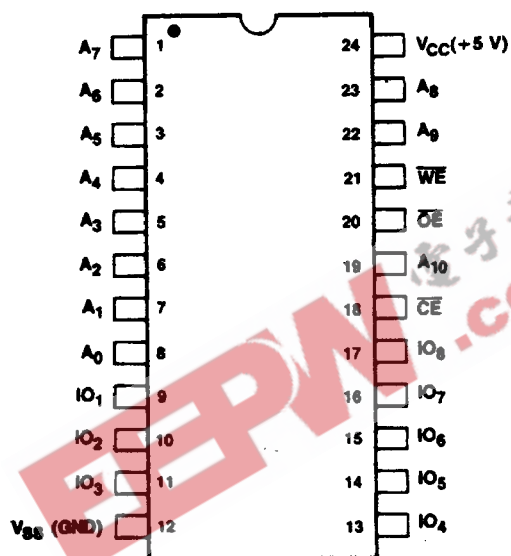
BD000281

### PRODUCT SELECTOR GUIDE

| Part Number                    | Am9128-70     | Am9128-90 | Am9128-10 | Am9128-12 | Am9128-15 | Am9128-20 |
|--------------------------------|---------------|-----------|-----------|-----------|-----------|-----------|
| Maximum Access Time (ns)       | 70            | 90        | 100       | 120       | 150       | 200       |
| Maximum Operating Current (mA) | 0 to 70°C     | 140       | N/A       | 120       | N/A       | 140       |
|                                | -55° to 125°C | N/A       | 180       | N/A       | 150       | 150       |
| Maximum Standby Current (mA)   | 0° to 70°C    | 30        | N/A       | 15        | N/A       | 30        |
|                                | -55° to 125°C | N/A       | 30        | N/A       | 30        | 30        |

**CONNECTION DIAGRAMS**  
Top View

DIPs



CD000121

Note: Pin 1 is marked for orientation.

**METALLIZATION AND PAD LAYOUT**

**4**

| Address Designators |                 |
|---------------------|-----------------|
| External            | Internal        |
| A <sub>3</sub>      | AX <sub>0</sub> |
| A <sub>4</sub>      | AX <sub>1</sub> |
| A <sub>5</sub>      | AX <sub>2</sub> |
| A <sub>6</sub>      | AX <sub>3</sub> |
| A <sub>7</sub>      | AX <sub>4</sub> |
| A <sub>8</sub>      | AX <sub>5</sub> |
| A <sub>10</sub>     | AX <sub>6</sub> |
| A <sub>0</sub>      | AY <sub>0</sub> |
| A <sub>1</sub>      | AY <sub>1</sub> |
| A <sub>2</sub>      | AY <sub>2</sub> |
| A <sub>9</sub>      | AY <sub>3</sub> |



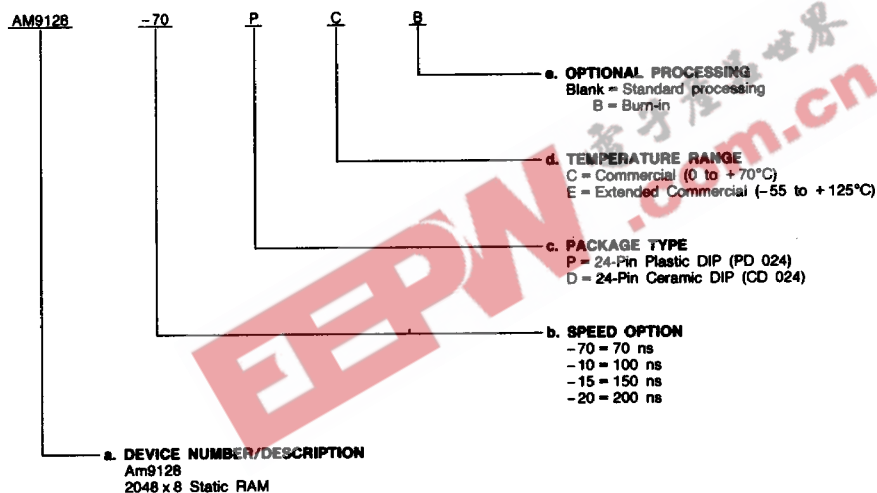
DIE SIZE: 0.162" x 0.240"

## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Package Type
- d. Temperature Range
- e. Optional Processing



| Valid Combinations |                         |
|--------------------|-------------------------|
| AM9128-70          | PC, DC, DCB, DE,<br>DEB |
| AM9128-10          |                         |
| AM9128-15          |                         |
| AM9128-20          |                         |

#### Valid Combinations

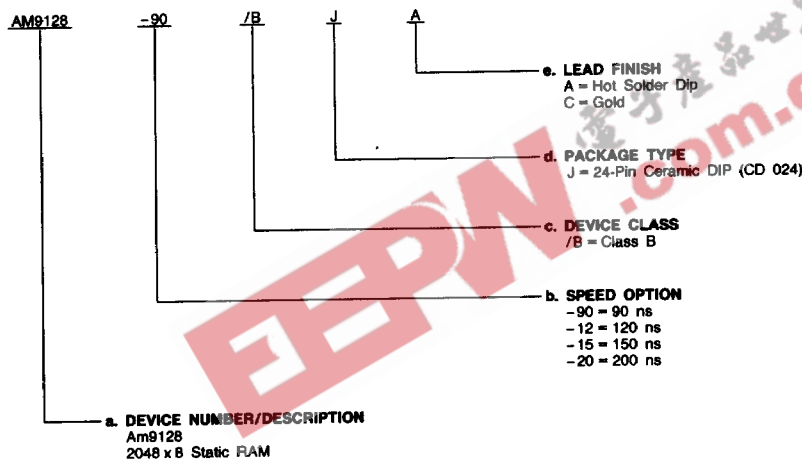
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

## ORDERING INFORMATION

### APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Device Class
- d. Package Type
- e. Lead Finish



| Valid Combinations |            |
|--------------------|------------|
| AM9128-90          | /BJA, /BJC |
| AM9128-12          |            |
| AM9128-15          |            |
| AM9128-20          |            |

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

4

#### Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11

## PIN DESCRIPTION

#### A<sub>0</sub> - A<sub>10</sub> Addresses (Input)

The 10-bit field presented at the address inputs selects one of the 2048 memory locations to be read from — or written into — via the data lines.

#### I/O<sub>1</sub> - I/O<sub>8</sub> Data In/Out Port (Input/Output)

If WE is LOW, the data represented on the I/O lines can be written into the selected memory location. If WE is HIGH, the I/O lines represent the data read from the selected memory location.

#### $\overline{CE}$ Chip Enable (Input, Active LOW)

Read and Write cycles can be executed only when  $\overline{CE}$  is LOW.

#### WE Write Enable (Input, Active LOW)

Data is written into the memory if WE is LOW and read from the memory if WE is HIGH.

#### $\overline{OE}$ Output Enable (Input, Active LOW)

Read cycles can be executed only when  $\overline{OE}$  is LOW.

### ABSOLUTE MAXIMUM RATINGS (Note 11)

|   |                  |
|---|------------------|
| Storage Temperature .....                       | -65 to +150°C    |
| Ambient Temperature with<br>Power Applied ..... | -55 to +125°C    |
| Supply Voltage .....                            | -0.5 V to +7.0 V |
| Signal Voltage with<br>Respect to Ground .....  | -3.0 V to +7.0 V |
| Power Dissipation .....                         | 1.0 W            |
| DC Output Current .....                         | 10 mA            |

\*Maximum ratings are to be for system design reference, parameters given may not be 100% tested by AMD.

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

### OPERATING RANGES (Note 3)

|   |                  |
|---|------------------|
| Commercial (C) Devices                            |                  |
| Ambient Temperature (T <sub>A</sub> ) .....       | 0 to +70°C       |
| Supply Voltage (V <sub>CC</sub> ) .....           | +4.5 V to +5.5 V |
| Military* (M) and Extended Commercial (E) Devices |                  |
| Case Temperature (T <sub>A</sub> ) .....          | -55 to +125°C    |
| Supply Voltage (V <sub>CC</sub> ) .....           | +4.5 V to +5.5 V |

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted) (Note 3)

| Parameter Symbol | Parameter Description                        | Test Conditions   | Am9128-90<br>Am9128-10 |                       | Am9128-15 |                       | Am9128-70<br>Am9128-12<br>Am9128-20 |                       | Unit |
|------------------|--|---|------------------------|-----------------------|-----------|-----------------------|-------------------------------------|-----------------------|------|
|                  |  |   | Min.                   | Max.                  | Min.      | Max.                  | Min.                                | Max.                  |      |
| I <sub>OH</sub>  | Output HIGH Current                          | V <sub>OH</sub> = 2.4 V   | -2                     |                       | -2        |                       | -2                                  |                       | mA   |
| I <sub>OL</sub>  | Output LOW Current                           | V <sub>OL</sub> = 0.4 V   | 4                      |                       | 4         |                       | 4                                   |                       | mA   |
| V <sub>IH</sub>  | Input HIGH Voltage                           |   | 2.0                    | V <sub>CC</sub> + 1.0 | 2.0       | V <sub>CC</sub> + 1.0 | 2.0                                 | V <sub>CC</sub> + 1.0 | V    |
| V <sub>IL</sub>  | Input LOW Voltage                            |   | -0.5                   | 0.8                   | -0.5      | 0.8                   | -0.5                                | 0.8                   | V    |
| I <sub>Ix</sub>  | Input Load Current                           | V <sub>SS</sub> < V <sub>I</sub> < V <sub>CC</sub>                                    |                        | 10                    |           | 10                    |                                     | 10                    | μA   |
| I <sub>OZ</sub>  | Output Leakage Current                       | V <sub>SS</sub> < V <sub>O</sub> < V <sub>CC</sub><br>Output Disabled                 |                        | 10                    |           | 10                    |                                     | 10                    | μA   |
| C <sub>IN</sub>  | Input Capacitance<br>(Note 12)               | Test Frequency = 1.0 MHz,<br>T <sub>A</sub> = 25°C,<br>All pins at 0                  |                        | 6                     |           | 6                     |                                     | 6                     | pF   |
| C <sub>I/O</sub> | Input/Output Capacitance<br>(Note 12)        |   |                        | 7                     |           | 7                     |                                     | 7                     |      |
| I <sub>CC</sub>  | V <sub>CC</sub> Operating Supply Current     | Max. V <sub>CC</sub> , $\overline{CE} < V_{IL}$<br>Outputs Open                       |                        | 120                   |           | 100                   | 140                                 |                       | mA   |
| I <sub>SB</sub>  | Automatic $\overline{CE}$ Power Down Current | Max. V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$                                    | COM'L                  | 15                    |           | 15                    | 30                                  |                       | mA   |
|                  |  |   | MIL/E-COM'L            | 30                    |           | 30                    | 30                                  |                       |      |
| I <sub>PO</sub>  | Peak Power On Current<br>(Note 12)           | V <sub>CC</sub> = GND to V <sub>CC</sub> Max.<br>$\overline{CE} \geq V_{IH}$ (Note 2) | COM'L                  | 15                    |           | 15                    | 30                                  |                       | mA   |
|                  |  |   | MIL/E-COM'L            | 30                    |           | 30                    | 30                                  |                       |      |

- Notes:
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
  - A pull up resistor to V<sub>CC</sub> on the  $\overline{CE}$  input is required during power up to keep the device deselected, otherwise I<sub>PO</sub> will exceed values given.
  - For test and correlation purposes, ambient temperature is defined as the "Instant-on" case temperature.
  - At any given temperature and voltage condition, t<sub>HZ</sub> is less than t<sub>LZ</sub>.
  - $\overline{WE}$  is HIGH for read cycle.
  - Device is continuously selected,  $\overline{CE} = V_{IL}$ .
  - Address valid prior to or coincident with  $\overline{CE}$  transition LOW.
  - $\overline{CE} = V_{IL}$ .
  - C<sub>L</sub> = 30 pF.
  - Transition is measured from 1.5 V on the input to V<sub>OH</sub> - 500 mV and V<sub>OL</sub> + 500 mV on the outputs using the load shown in Switching Test Circuits. C<sub>L</sub> = 5 pF.
  - The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling, and use to avoid exposure to excessive voltages.
  - The parameter is guaranteed by characterization, but is not tested.

**SWITCHING CHARACTERISTICS** over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted.)

Am9128-70, -90, -10

| No.                | Parameter Symbol | Parameter Description                                  | Am9128-70     |      | Am9128-90 |      | Am9128-10 |      | Unit |
|--------------------|------------------|--|---------------|------|-----------|------|-----------|------|------|
|                    |                  |  | Min.          | Max. | Min.      | Max. | Min.      | Max. |      |
| <b>READ CYCLE</b>  |                  |  |               |      |           |      |           |      |      |
| 1                  | t <sub>RC</sub>  | Read Cycle Time  | 70            |      | 90        |      | 100       |      | ns   |
| 2                  | t <sub>ACC</sub> | Address Access Time (Note 9)                           |               | 70   |           | 90   |           | 100  | ns   |
| 3                  | t <sub>ACS</sub> | Chip Select Access Time (Note 9)                       |               | 70   |           | 90   |           | 100  | ns   |
| 4                  | t <sub>OE</sub>  | Output Enable Time (Note 9)                            | COM'L         | 40   |           | N/A  |           | 50   | ns   |
|                    |                  |  | MIL           |      | N/A       |      | 50        | N/A  |      |
| 5                  | t <sub>OH</sub>  | Output Hold Time from Address Change                   | 5             |      | 5         |      | 5         |      | ns   |
| 6                  | t <sub>CLZ</sub> | Output in Low-Z from $\overline{CE}$ (Notes 4, 10, 12) | 5             |      | 5         |      | 5         |      | ns   |
| 7                  | t <sub>CHZ</sub> | Output in Hi-Z from $\overline{CE}$ (Notes 4, 10, 12)  |               | 35   |           | 40   |           | 40   | ns   |
| 8                  | t <sub>OLZ</sub> | Output in Low-Z from $\overline{OE}$ (Notes 4, 10, 12) | 5             |      | 5         |      | 5         |      | ns   |
| 9                  | t <sub>OHZ</sub> | Output in Hi-Z from $\overline{OE}$ (Notes 4, 10, 12)  |               | 30   |           | 35   |           | 35   | ns   |
| 10                 | t <sub>PU</sub>  | Chip Selection to Power-Up Time (Note 12)              | 0             |      | 0         |      | 0         |      | ns   |
| 11                 | t <sub>PD</sub>  | Chip Deselection to Power-Down Time (Note 12)          |               | 40   |           | 45   |           | 50   | ns   |
| <b>WRITE CYCLE</b> |                  |  |               |      |           |      |           |      |      |
| 12                 | t <sub>WC</sub>  | Write Cycle Time                                       | 70            |      | 90        |      | 100       |      | ns   |
| 13                 | t <sub>OW</sub>  | Chip Selection to End of Write (Note 1)                | 0 to +70°C    | 60   |           | N/A  |           | 90   | ns   |
|                    |                  |  | -55 to -125°C | N/A  |           | 80   |           | N/A  |      |
| 14                 | t <sub>AS</sub>  | Address Setup Time                                     | 5             |      | 10        |      | 10        |      | ns   |
| 15                 | t <sub>WP</sub>  | Write Pulse Width (Note 1)                             | 40            |      | 55        |      | 60        |      | ns   |
| 16                 | t <sub>WR</sub>  | Write Recovery Time                                    | 5             |      | 5         |      | 5         |      | ns   |
| 17                 | t <sub>DS</sub>  | Data Setup Time  | 30            |      | 35        |      | 40        |      | ns   |
| 18                 | t <sub>DH</sub>  | Data Hold Time   | 5             |      | 5         |      | 5         |      | ns   |
| 19                 | t <sub>WLZ</sub> | Output in Low-Z from $\overline{WE}$ (Notes 4, 10, 12) | 5             |      | 5         |      | 5         |      | ns   |
| 20                 | t <sub>WHZ</sub> | Output in Hi-Z from $\overline{WE}$ (Notes 4, 10, 12)  |               | 30   |           | 35   |           | 35   | ns   |
| 21                 | t <sub>AW</sub>  | Address to End of Write                                | 65            |      | 80        |      | 80        |      | ns   |

Notes: See notes following DC Characteristics table.

4

### SWITCHING CHARACTERISTICS (Cont'd.)

Am9128-12, -15, -20

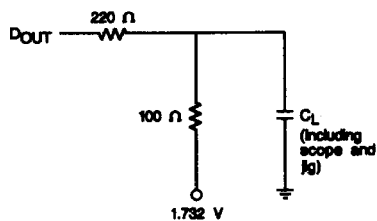
| No.                | Parameter Symbol | Parameter Description                         | Am9128-12 |      | Am9128-15 |      | Am9128-20 |      | Unit |
|--------------------|------------------|---|-----------|------|-----------|------|-----------|------|------|
|                    |                  |   | Min.      | Max. | Min.      | Max. | Min.      | Max. |      |
| <b>READ CYCLE</b>  |                  |   |           |      |           |      |           |      |      |
| 1                  | $t_{RC}$         | Read Cycle Time                               | 120       |      | 150       |      | 200       |      | ns   |
| 2                  | $t_{ACC}$        | Address Access Time (Note 9)                  |           | 120  |           | 150  |           | 200  | ns   |
| 3                  | $t_{ACS}$        | Chip Select Access Time (Note 9)              |           | 120  |           | 150  |           | 200  | ns   |
| 4                  | $t_{OE}$         | Output Enable Time (Note 9)                   | COM'L     |      | N/A       |      | 80        |      | ns   |
|                    |                  |   | MIL       |      | 70        |      | 70        |      |      |
| 5                  | $t_{OH}$         | Output Hold Time from Address Change          | 5         |      | 5         |      | 5         |      | ns   |
| 6                  | $t_{CLZ}$        | Output in Low-Z from CE (Notes 4, 10, 12)     | 5         |      | 5         |      | 5         |      | ns   |
| 7                  | $t_{CHZ}$        | Output in Hi-Z from CE (Notes 4, 10, 12)      |           | 50   |           | 55   |           | 55   | ns   |
| 8                  | $t_{OLZ}$        | Output in Low-Z from OE (Notes 4, 10, 12)     | 5         |      | 5         |      | 5         |      | ns   |
| 9                  | $t_{OHZ}$        | Output in Hi-Z from OE (Notes 4, 10, 12)      |           | 45   |           | 50   |           | 50   | ns   |
| 10                 | $t_{PU}$         | Chip Selection to Power-Up Time (Note 12)     | 0         |      | 0         |      | 0         |      | ns   |
| 11                 | $t_{PD}$         | Chip Deselection to Power-Down Time (Note 12) |           | 55   |           | 60   |           | 60   | ns   |
| <b>WRITE CYCLE</b> |                  |   |           |      |           |      |           |      |      |
| 12                 | $t_{WC}$         | Write Cycle Time                              | 120       |      | 150       |      | 200       |      | ns   |
| 13                 | $t_{OW}$         | Chip Selection to End of Write (Note 1)       | COM'L     |      | N/A       |      | 150       |      | ns   |
|                    |                  |   | MIL       |      | 105       |      | 160       |      |      |
| 14                 | $t_{AS}$         | Address Setup Time                            | 10        |      | 20        |      | 20        |      | ns   |
| 15                 | $t_{WP}$         | Write Pulse Width (Note 1)                    | 70        |      | 85        |      | 100       |      | ns   |
| 16                 | $t_{WR}$         | Write Recovery Time                           | 5         |      | 5         |      | 5         |      | ns   |
| 17                 | $t_{DS}$         | Data Setup Time                               | 45        |      | 50        |      | 60        |      | ns   |
| 18                 | $t_{DH}$         | Data Hold Time                                | 5         |      | 5         |      | 5         |      | ns   |
| 19                 | $t_{WLZ}$        | Output in Low-Z from WE (Notes 4, 10, 12)     | 5         |      | 5         |      | 5         |      | ns   |
| 20                 | $t_{WHZ}$        | Output in Hi-Z from WE (Notes 4, 10, 12)      |           | 50   |           | 50   |           | 50   | ns   |
| 21                 | $t_{AW}$         | Address to End of Write                       | 105       |      | 120       |      | 120       |      | ns   |

Notes: See notes following DC Characteristics table.

#### SWITCHING TEST CONDITIONS

|                                |             |
|--------------------------------|-------------|
| Input Pulse Levels             | .4 to 2.4 V |
| Input Rise and Fall Times      | 10 ns       |
| Input Timing Reference Levels  | 1.4 V       |
| Output Timing Reference Levels | 1.4 V       |

#### SWITCHING TEST CIRCUIT



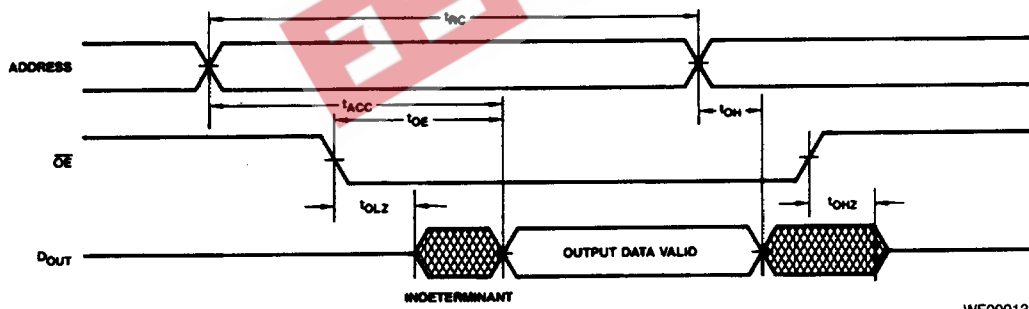
TC003700

## SWITCHING WAVEFORMS

### KEY TO SWITCHING WAVEFORMS

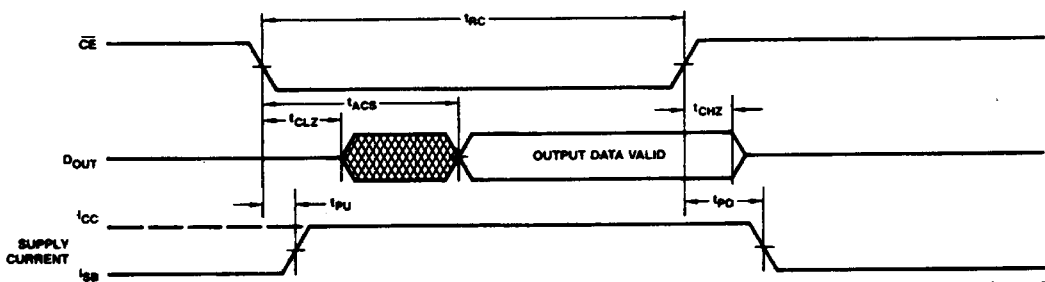
| WAVEFORM | INPUTS                           | OUTPUTS                                   |
|----------|----------------------------------|---|
| —        | MUST BE STEADY                   | WILL BE STEADY                            |
| / / / /  | MAY CHANGE FROM H TO L           | WILL BE CHANGING FROM H TO L              |
| \ \ \ \  | MAY CHANGE FROM L TO H           | WILL BE CHANGING FROM L TO H              |
| X X X X  | DON'T CARE; ANY CHANGE PERMITTED | CHANGING; STATE UNKNOWN                   |
| / / \ \  | DOES NOT APPLY                   | CENTER LINE IS HIGH IMPEDANCE "OFF" STATE |

KS000010



WF000130

**Read Cycle No. 1 (Notes 5, 6)**



WF000140

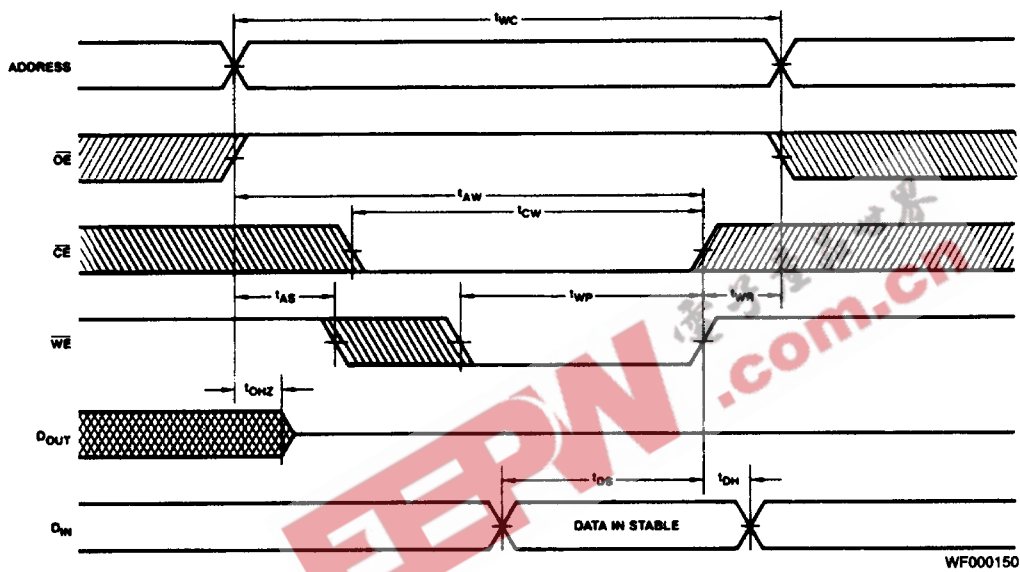
**Read Cycle No. 2 (Notes 5, 7, 8)**

Notes: See notes following DC Characteristics table.

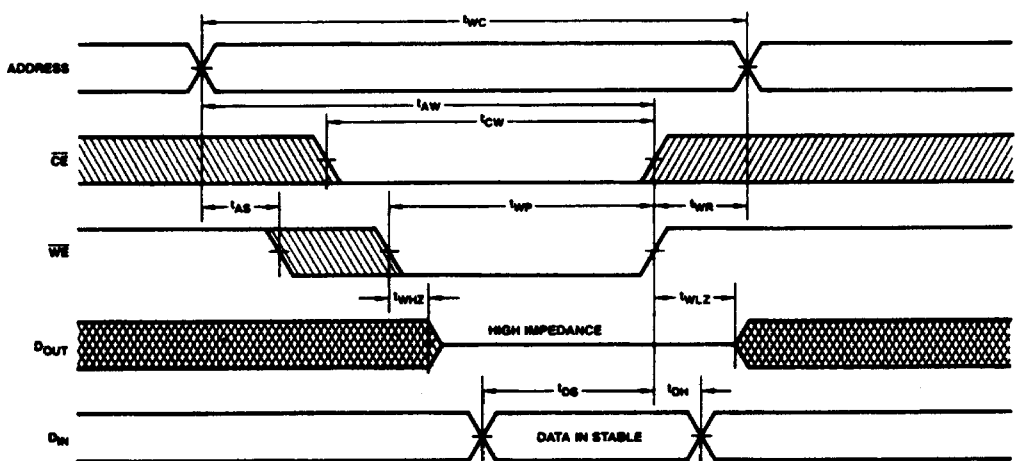
4



SWITCHING WAVEFORMS (Cont'd.)



Write Cycle No. 1

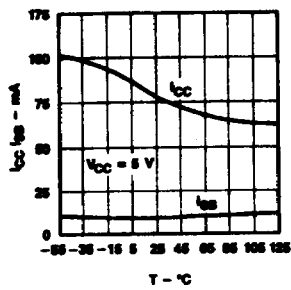


Write Cycle No. 2 (Notes 7, 8)

Notes: See notes following DC Characteristics table.

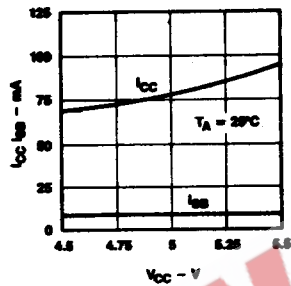
### TYPICAL PERFORMANCE CURVES

Supply Current Versus Ambient Temperature



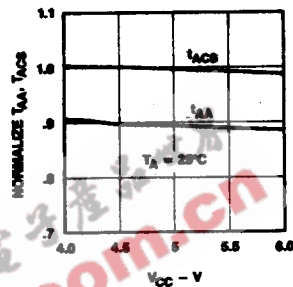
OP000640

Supply Current Versus Supply Voltage



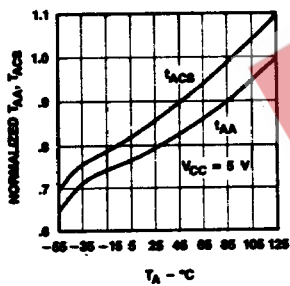
OP000650

Normalized Access Time Versus Supply Voltage



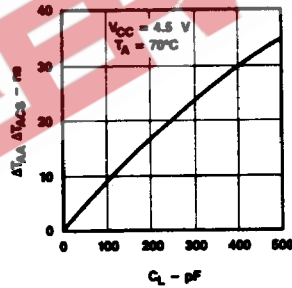
OP000660

Normalized Access Time Versus Ambient Temperature



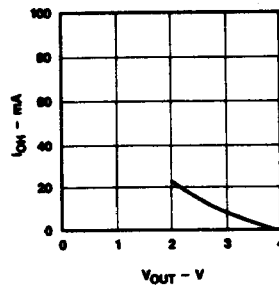
OP000670

Access Time Change Versus Output Loading



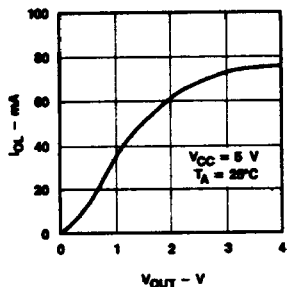
OP000680

Output Source Current Versus Output Voltage



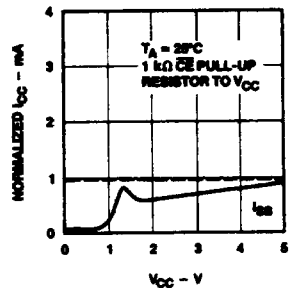
OP000690

Output Sink Current Versus Output Voltage



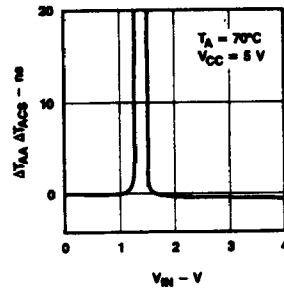
OP000700

Typical Power-On Current Versus Power Supply



OP000710

Access Time Change Versus Input Voltage



OP000720