



LC78856M, 78856V

Built-in Digital Filter D/A Converters for Digital Audio

Preliminary

Overview

The LC78856M and LC78856V are $\Sigma\Delta$ -type digital-audio D/A converter circuits with built-in digital filters.

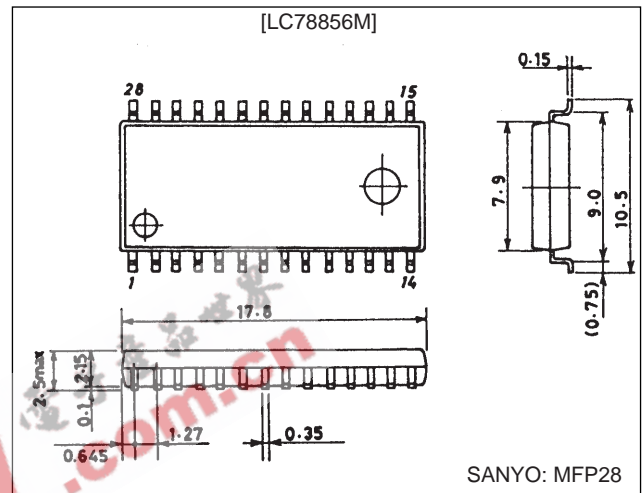
Features

- 8× oversampling digital filter
- Digital de-emphasis (supports $f_s = 44.1$ kHz)
- Soft muting
- Double speed support
- Support for a 384fs system clock
- PWM outputs
- 5 V single-voltage power supply
- Si-gate CMOS process

Package Dimensions

unit: mm

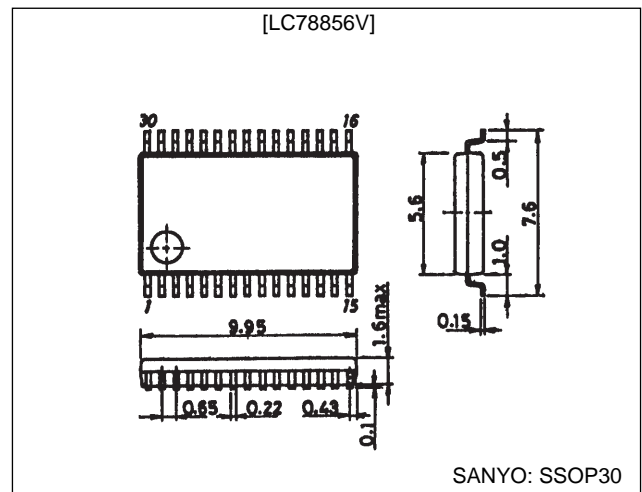
3091A-MFP28



SANYO: MFP28

unit: mm

3191-SSOP30



SANYO: SSOP30

Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{DD \text{ max}}$		-0.3 to +7.0	V
Maximum input voltage	$V_{IN \text{ max}}$		-0.3 to $V_{DD} + 0.3$	V
Maximum output voltage	$V_{OUT \text{ max}}$		-0.3 to $V_{DD} + 0.3$	V
Operating temperature	T_{opr}		-30 to +75	$^\circ\text{C}$
Storage temperature	T_{stg}		-40 to +125	$^\circ\text{C}$

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Allowable Operating Ranges at $T_a = -30$ to $+75^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}		3.0		5.5	V
Input voltage	V_{IN}		0		V_{DD}	V

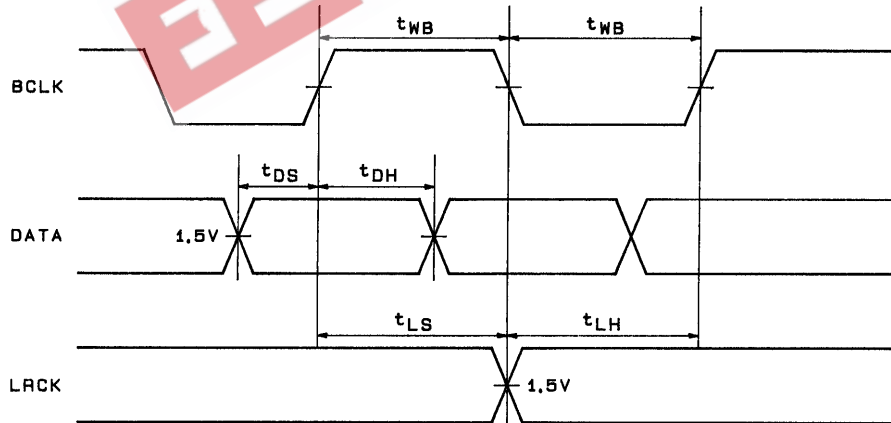
DC Characteristics at $T_a = -30$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5 V, $V_{SS} = 0$ V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input high-level voltage (1)	V_{IH1}	The XIN pin	$0.7 V_{DD}$			V
Input low-level voltage (1)	V_{IL1}	The XIN pin			$0.3 V_{DD}$	V
Input high-level voltage (2)	V_{IH2}	Pins other than the XIN pin	2.2			V
Input low-level voltage (2)	V_{IL2}	Pins other than the XIN pin			0.8	V
Output high-level voltage	V_{OH}	$I_{OH} = -1 \mu\text{A}$	$V_{DD} - 0.1$			V
Output low-level voltage	V_{OL}	$I_{OL} = 1 \mu\text{A}$			0.1	V
Power dissipation	P_d	$V_{DD} = 5.0$ V		140	200	mW

DC Characteristics at $T_a = -30$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5 V, $V_{SS} = 0$ V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Oscillator frequency	f_X			16.9	18.5	MHz
BCLK frequency	f_{BCK}				2.4	MHz
BCLK pulse width	t_{WB}		100			ns
Data setup time	t_{DS}		20			ns
Data hold time	t_{DH}		20			ns
LRCK setup time	t_{LS}		50			ns
LRCK hold time	t_{LH}		50			ns

Timing Chart

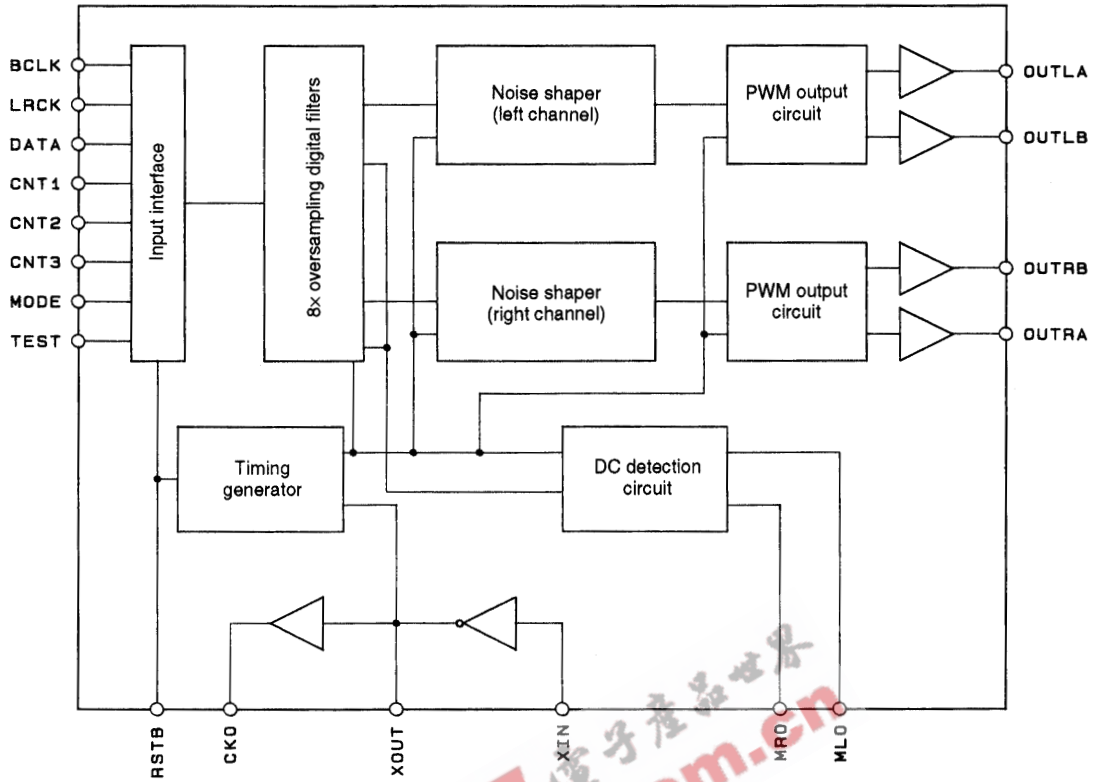


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Analog Characteristics at $T_a = 25^\circ\text{C}$, $V_{DD} = 5.0$ V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Total harmonic distortion	THD + N	$f = 1$ kHz, 0 dB		0.005		%
Signal-to-noise ratio	S/N	JIS-A		100		dB
Crosstalk	CT	$f = 1$ kHz, 0 dB		98		dB
Dynamic range	DR	JIS-A		94		dB

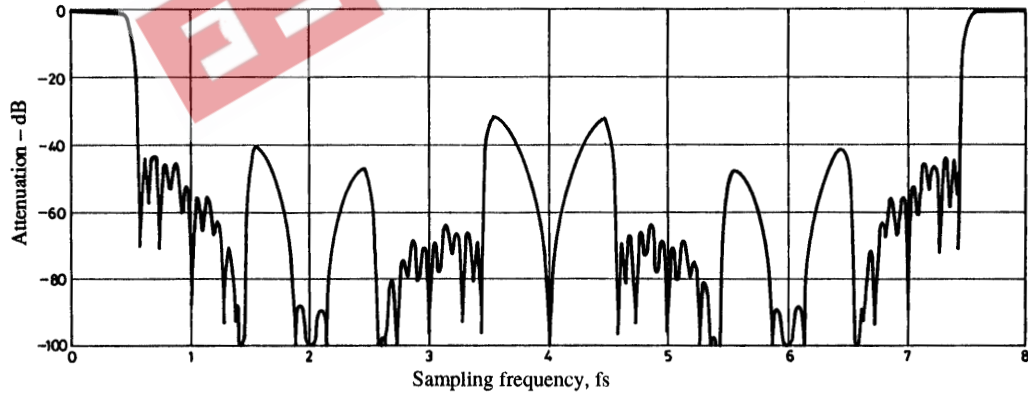
Block Diagram



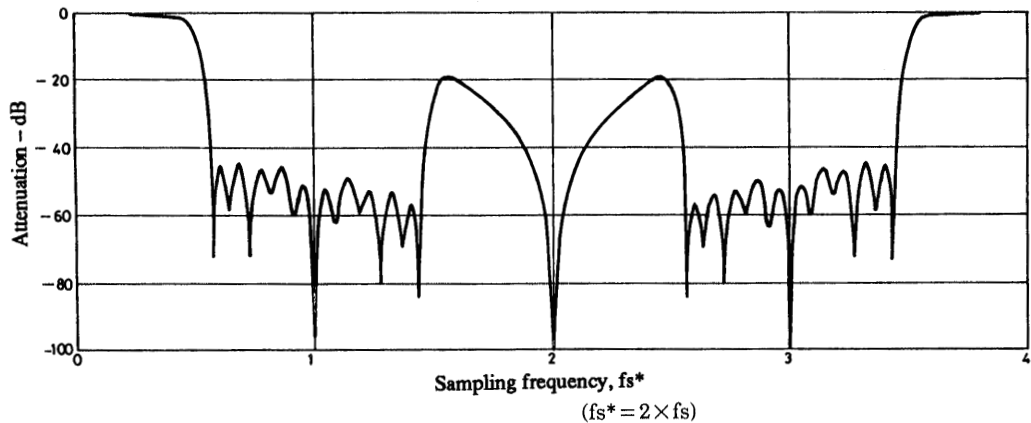
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Filter Characteristics

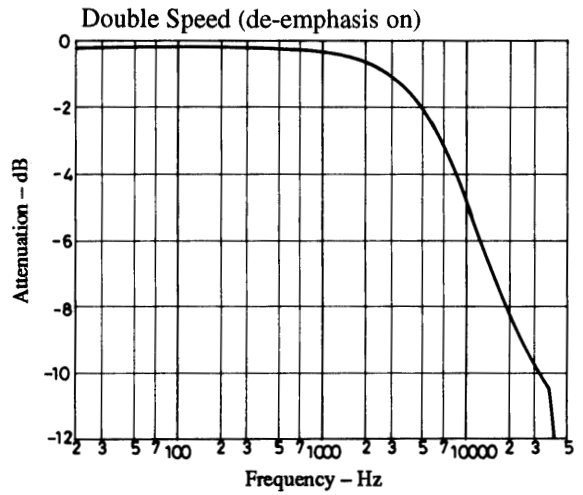
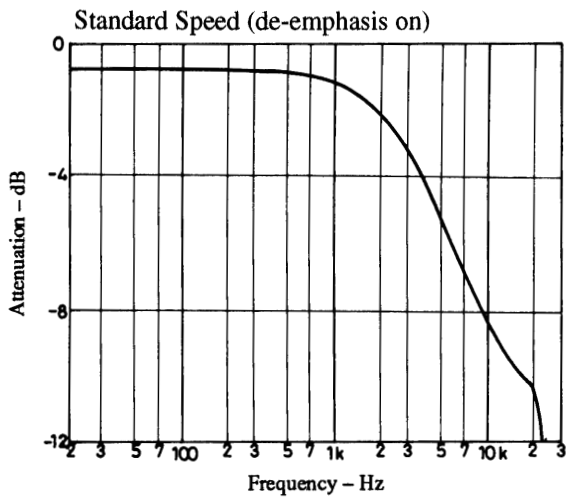
Standard Speed (de-emphasis off)



Double Speed (de-emphasis off)



LC78856M, 78856V

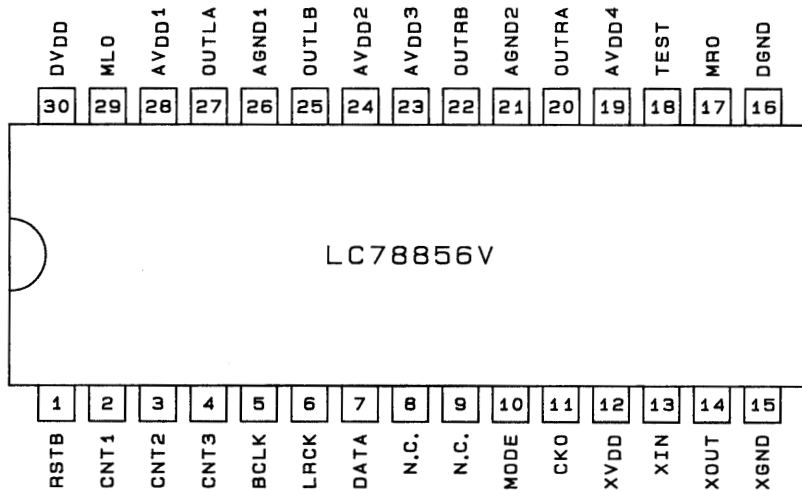


Pin Assignments



Top view

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Top view

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Pin Functions

SSOP	MFP	Symbol	Function
1	1	RSTB	Reset input (A low-level input resets the LSI internal circuits.)
2	2	CNT1	Emphasis on/off switching input
3	3	CNT2	Standard speed/double speed switching input
4	4	CNT3	Soft mute input
5	5	BCLK	Bit clock input
6	6	LRCK	LR clock input
7	7	DATA	Digital audio data input
10	8	MODE	Input format setting
11	9	CKO	Clock output
12	10	XV _{DD}	Oscillator amplifier power supply
13	11	XIN	Oscillator amplifier input
14	12	XOUT	Oscillator amplifier output
15	13	XGND	Oscillator amplifier ground
16	14	DGND	Digital system ground
17	15	MRO	Right channel mute signal output
18	16	TEST	Test pin (Must be tied low in normal operation.)
19	17	AV _{DD4}	Analog system power supply
20	18	OUTRA	Right channel output A
21	19	AGND2	Analog system ground
22	20	OUTRB	Right channel output B
23	21	AV _{DD3}	Analog system power supply
24	22	AV _{DD2}	Analog system power supply
25	23	OUTLB	Left channel output B
26	24	AGND1	Analog system ground
27	25	OUTLA	Left channel output A
28	26	AV _{DD1}	Analog system power supply
29	27	MLO	Left channel mute signal output
30	28	DV _{DD}	Digital system power supply

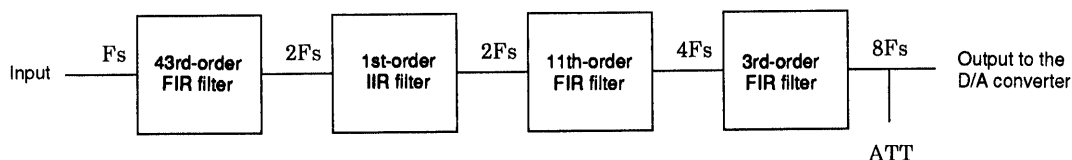
Operating Description

The LC78856M and LC78856V internal circuits can be roughly divided into the digital filter block and the 1-bit D/A converter block.

[Digital Filter Block]

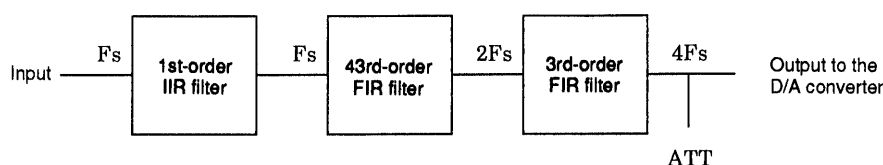
1. Standard Speed

The LC78856M and LC78856V implements 8× oversampling using three FIR filters: a 43rd-order filter, an 11th-order filter, and a 3rd-order filter. A 1st-order IIR filter is used for de-emphasis.



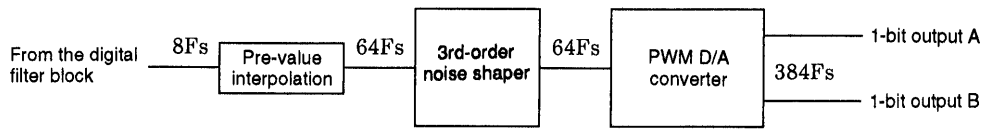
2. Double Speed

Double-speed playback is used, for example, for dubbing CDs to audio tape at double speed. Here, the same frequency is used for XIN, but BCLK, LRCK and DATA are input at twice the rates used in standard-speed playback. After de-emphasis is applied with a 1st-order IIR filter, the signal is 4× oversampled using a 43rd-order FIR filter and a 3rd-order FIR filter.



3. One-Bit D/A Converter Block

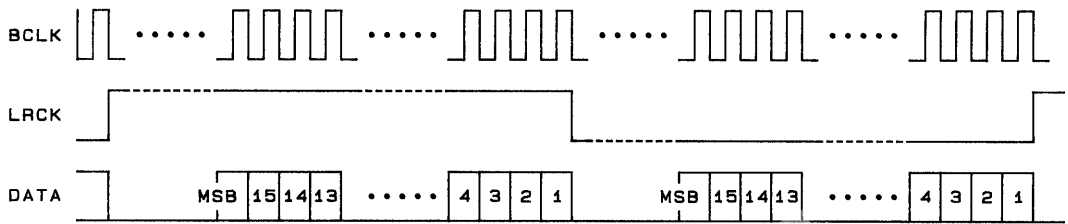
The 1-bit D/A converter accepts 8fs data input and outputs a 384fs 1-bit data stream.



LC78856M/V Inputs

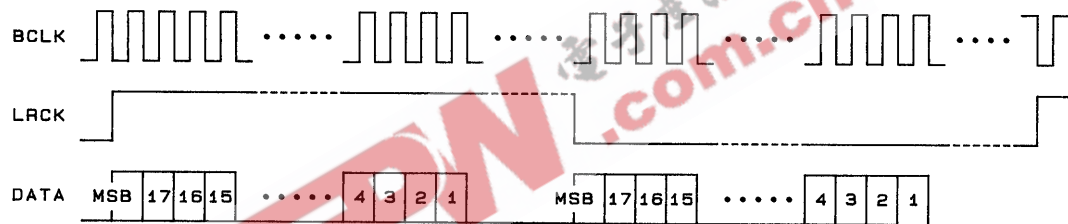
1. Input Data Format

- Format 1 (MODE = high)



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- Format 2 (MODE = low)



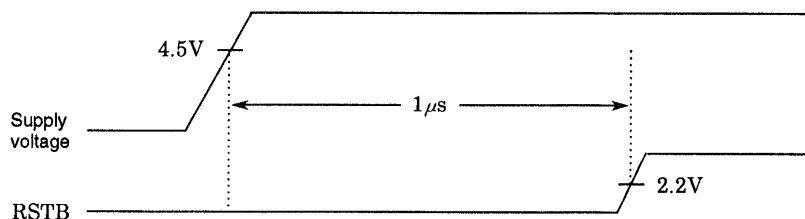
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2. Control Signals (CNT1 to CNT3)

Symbol	Function	L	H
CNT1	Emphasis switching	Off	On
CNT2	Standard speed/double speed	Standard speed	Double speed
CNT3	Soft mute	Off	On

3. Initialization

The LC78856M and LC78856V requires initialization when power is first applied and when settings are changed. The LC78856M and LC78856V is initialized by setting the RSTB pin low. The length of the low-level period must extend 1 μ s beyond the point where the XIN input is applied. When RSTB is low, all digital filter and noise shaper internal data is set to 0, and the D/A converter outputs an analog 0.



LC78856M/V Outputs

1. CKO

CKO outputs a clock signal with the same frequency as the signal input to the XIN pin.

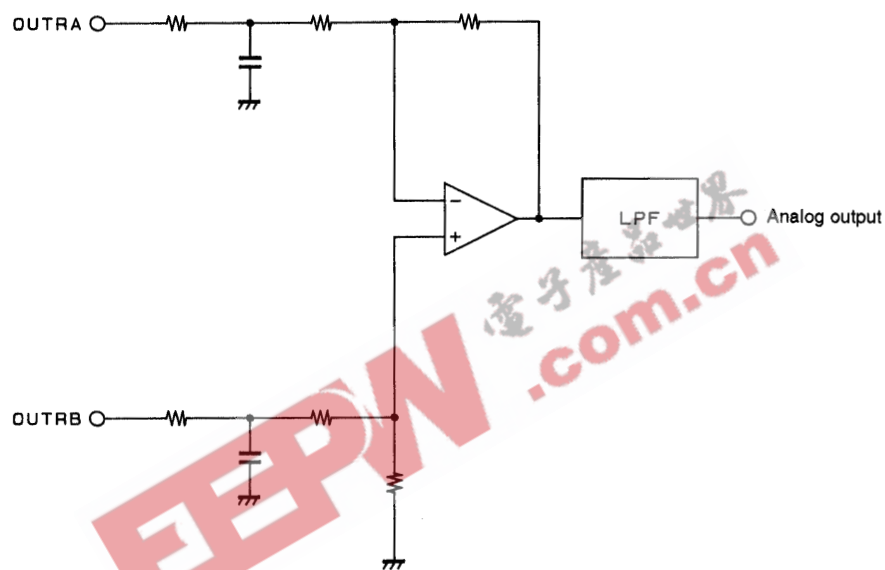
2. MLO, MRO

These pins output a high level when either the attenuator coefficient has become 0, or when the corresponding channel data has been 0 for 2^{13} or more cycles.

3. OUTLA, OUTLB, OUTRA, OUTRB

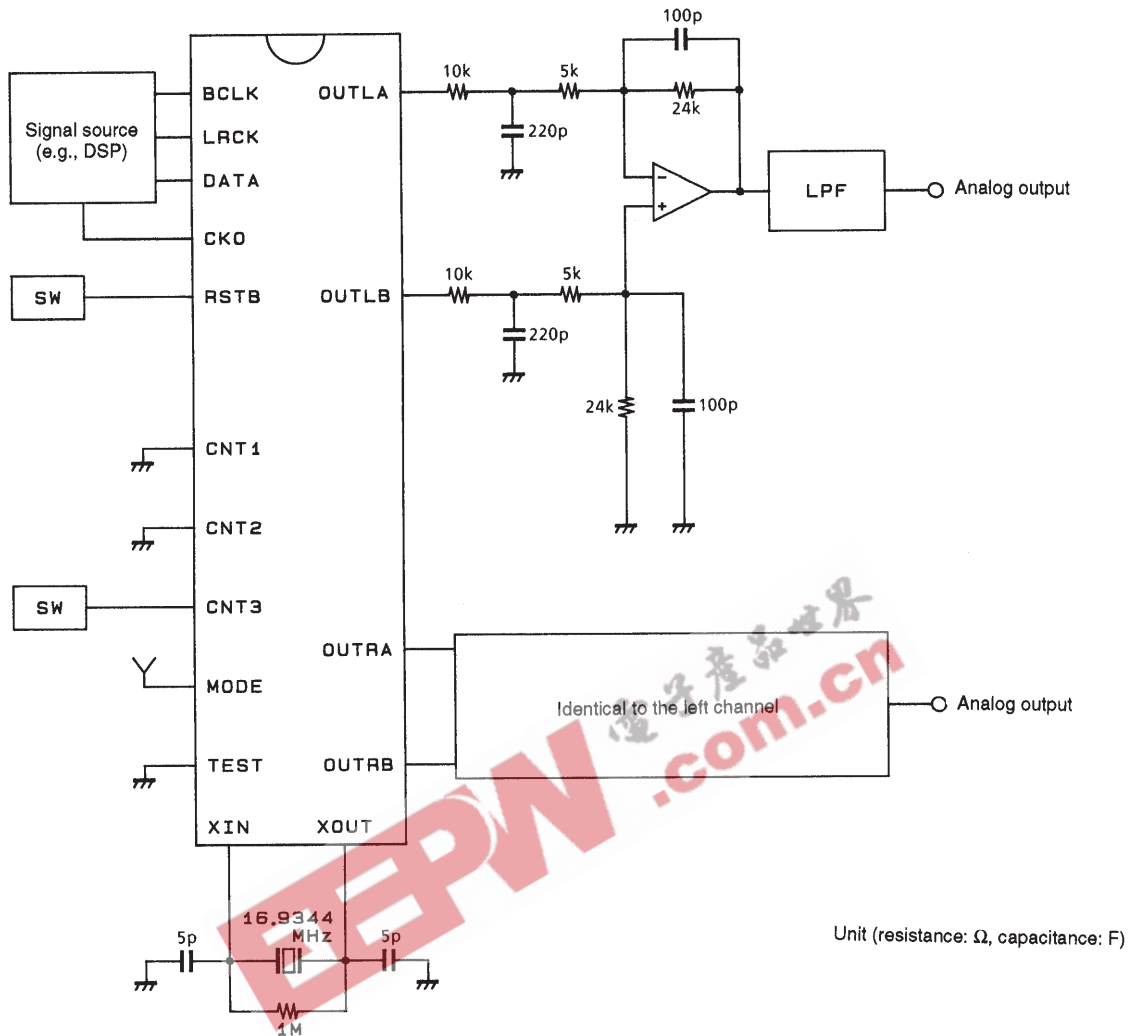
These four pins produce outputs in synchronization with the XIN clock. High-precision analog signals can be acquired by differentially amplifying the output signals and passing that result through an LPF. The figure below shows a sample circuit structure.

Sample Output Circuit Structure



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Sample Application Circuit



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