

**SANYO**

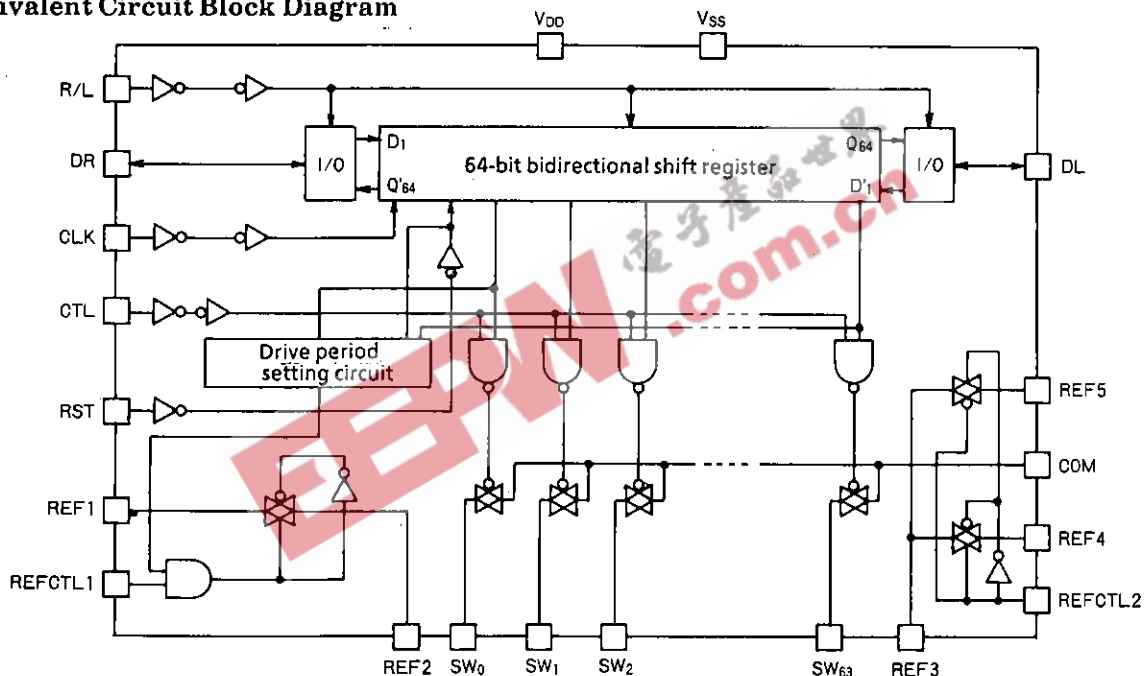
No.3256

**LC7938C**a-Si Contact Type  
Image Sensor-Use Driver**Features**

- High-speed silicon gate CMOS device
- On-chip high-speed shiftable (5MHz max.) 64-bit bidirectional shift register, 64-bit sensor driver analog switch
- On-chip CTL signal (CTL) to turn OFF 64-bit sensor driver analog switch
- On-chip noise cancel analog switch

**Package**

Available in chip form, Chip size : 1.67mm×6.63mm, Number of pads : 80

**Equivalent Circuit Block Diagram****Electrical Characteristics**

The Electrical Characteristics shown below are for the LC7938C placed in our standard ceramic package.

**Absolute Maximum Ratings at Ta = 25°C**

Parameter	Symbol	Conditions	Limits	unit
Maximum Supply Voltage	V <sub>CC</sub> max		-0.3 to +7.0	V
Input Voltage	V <sub>IN</sub>		-0.3 to V <sub>DD</sub> +0.3	V
Output Voltage	V <sub>OUT</sub>		-0.3 to V <sub>DD</sub> +0.3	V
Operating Temperature	T <sub>opr</sub>	(Junction temperature)	-25 to +85	°C
Storage Temperature	T <sub>stg</sub>		-40 to +125	°C

Note) The die bond temperature and other parameters are listed in the common specification for quality assurance prepared separately.

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1250TA, TS No.3256-1/6

LC7938C

Allowable Operating Conditions at  $T_a = 25 \pm 2^\circ\text{C}$ ,  $V_{SS} = 0\text{V}$

Parameter	Symbol	Applicable Pad Name	Conditions	Limits			unit
				min	typ	max	
Supply Voltage	$V_{DD}$			4.5	5.0	5.5	V
Input 'H'-Level Voltage	$V_{IH}$	CLK,DR,DL, RST,R/L,CTR,		$0.7V_{DD}$		$V_{DD}$	V
Input 'L'-Level Voltage	$V_{IL}$	REFCTL1, REFCTL2		0		$0.3V_{DD}$	V
Operating Frequency	$f_{CLK}$	CLK	Duty = $1/2 \pm 10\%$			5.0	MHz
Clock Pulse Width	$f_{\phi WH}$	CLK		100			ns
Data Setup Time	$t_{DS}$	CLK,DR,DL		50			ns
Data Hold Time	$t_{DH}$			50			ns
Reset Pulse Width	$f_{RW}$	RST		125			ns
Reset OFF Time	$t_{RS}$	RST,CLK		125			ns
Maximum Clock Rise/Fall Time	$t_r, t_f$	CLK	Duty = $1/2 \pm 10\%$			150	ns

Electrical Characteristics at  $T_a = 25 \pm 2^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $5.5\text{V}$ ,  $V_{SS} = 0\text{V}$

Parameter	Symbol	Applicable Pad Name	Conditions	Limits			unit
				min	typ	max	
Output 'H'-Level Voltage	$V_{OH}$	DR,DL	$I_{OH} = -0.3\text{mA}$	$V_{DD} - 0.3$		$V_{DD}$	V
Output 'L'-Level Voltage	$V_{OL}$		$I_{OL} = 0.3\text{mA}$	0		0.3	V
Analog SW ON Resistance	$R_{ON(1)}$	SW <sub>0</sub> to SW <sub>63</sub> to COM	COM = 0V, $V_{DD} = 5\text{V}$ , SW <sub>0</sub> to SW <sub>63</sub> = 0.2V		1.0		k $\Omega$
	$R_{ON(2)}$		COM = 0.2V, $V_{DD} = 5\text{V}$ , SW <sub>0</sub> to SW <sub>63</sub> = 0V		1.0		k $\Omega$
	$R_{ON(3)}$	REF1 to REF2	REF1 = 0V, $V_{DD} = 5\text{V}$ , REF2 = 0.2V		1.0		k $\Omega$
	$R_{ON(4)}$		REF1 = 0.2V, $V_{DD} = 5\text{V}$ , REF2 = 0V		1.0		k $\Omega$
	$R_{ON(5)}$	REF3 to REF4	REF3 = 0V, $V_{DD} = 5\text{V}$ , REF4 = 0.2V		200		$\Omega$
	$R_{ON(6)}$		REF3 = 0.2V, $V_{DD} = 5\text{V}$ , REF4 = 0V		200		$\Omega$
	$R_{ON(7)}$	REF3 to REF5	REF3 = 0V, $V_{DD} = 5\text{V}$ , REF5 = 0.2V		200		$\Omega$
	$R_{ON(8)}$		REF3 = 0.2V, $V_{DD} = 5\text{V}$ , REF5 = 0V		200		$\Omega$

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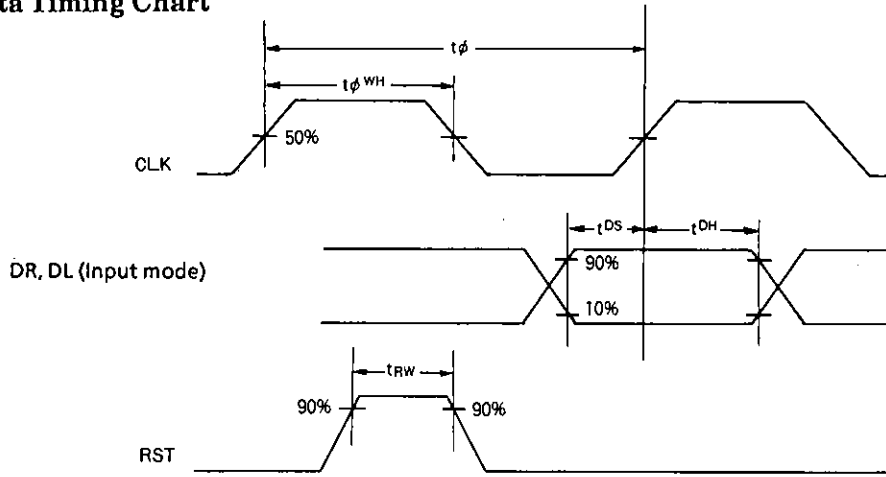
Parameter	Symbol	Applicable Pad Name	Conditions	Limits			unit
				min	typ	max	
Input/Output OFF Leakage Current	I <sub>OFF(1)</sub>	SW <sub>0</sub> to SW <sub>63</sub> COM	Analog SW OFF, COM = 0V, SW <sub>0</sub> to SW <sub>63</sub> = V <sub>DD</sub> , sum of individual pole leakage currents V <sub>DD</sub> = 5V, T <sub>a</sub> = 60°C			1.0	μA
	I <sub>OFF(2)</sub>					1.0	μA
Input Capacitance	C1	SW <sub>0</sub> to SW <sub>63</sub>			(1.5)		pF
	C2	COM				(150)	pF
Operating Current Dissipation	I <sub>DD</sub>	V <sub>DD</sub>	All outputs open, f = 1MHz			1	mA

( ): "Design to" value

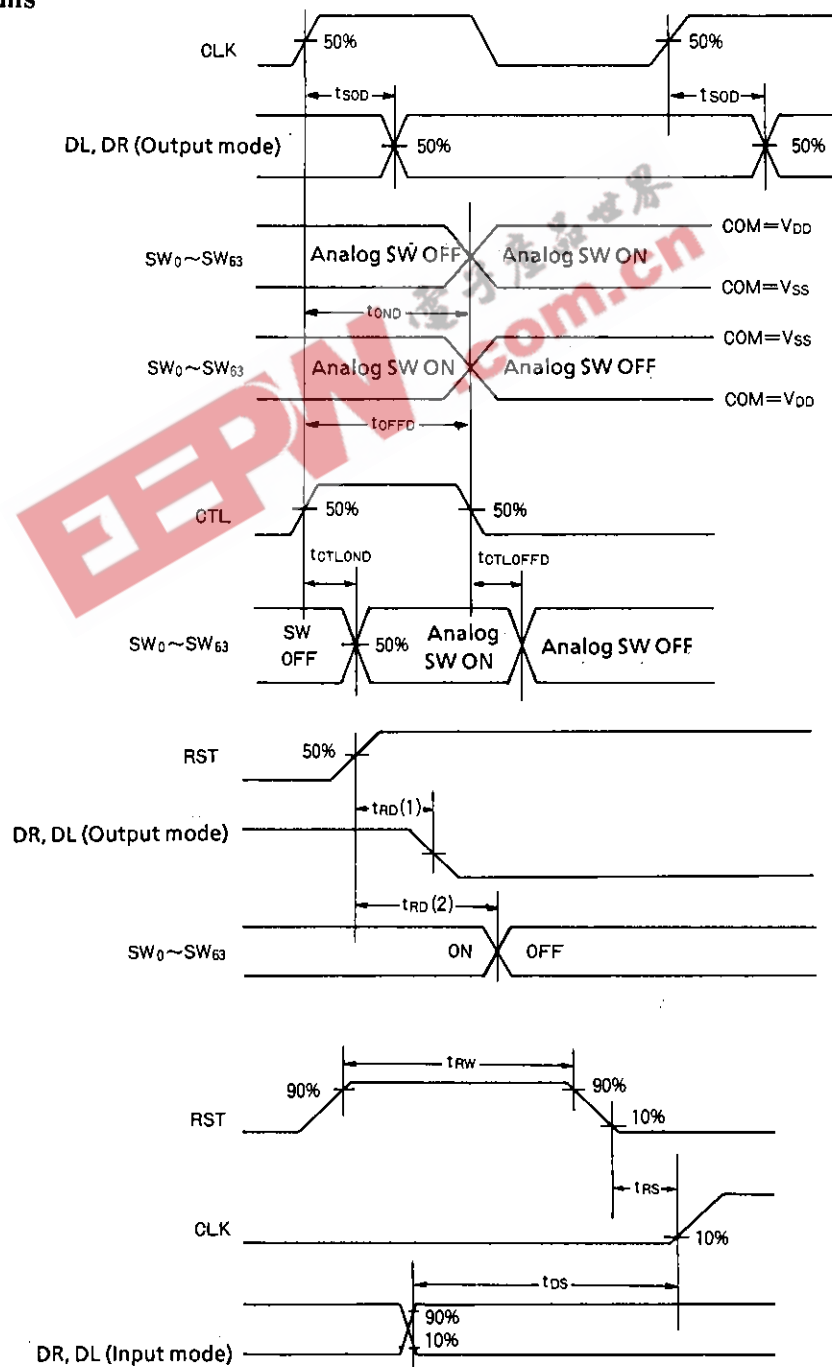
Switching Characteristics at T<sub>a</sub> = 25 ± 2°C, V<sub>DD</sub> = 4.5 to 5.5V, V<sub>SS</sub> = 0V

Parameter	Symbol	Applicable Pad Name	Conditions	Limits			unit
				min	typ	max	
Analog SW Turn-ON Delay Time	t <sub>OND</sub>	CLK → SW <sub>0</sub> to SW <sub>63</sub>	CTL = V <sub>DD</sub> , RST = V <sub>SS</sub> ,			150	ns
Analog SW Turn-OFF Delay Time	t <sub>OFFD</sub>	CLK → SW <sub>0</sub> to SW <sub>63</sub>	C <sub>L</sub> = 20pF, R <sub>L</sub> = 1kΩ			150	ns
Data Output Delay Time	t <sub>SOD</sub>	CLK → DR, DL	C <sub>L</sub> = 20pF			200	ns
Reset Signal Delay Time	t <sub>RD(1)</sub>	RST → DR, DL	C <sub>L</sub> = 20pF			200	ns
	t <sub>RD(2)</sub>	RST → SW <sub>0</sub> to SW <sub>63</sub>	CTL = V <sub>DD</sub> , C <sub>L</sub> = 20pF, R <sub>L</sub> = 1kΩ			200	ns
Control Signal Delay Time	t <sub>CTL-OND(1)</sub>	CTL → SW <sub>0</sub> to SW <sub>63</sub>	C <sub>L</sub> = 20pF, R <sub>L</sub> = 1kΩ			120	ns
	t <sub>CTL-OND(2)</sub>	REFCTL1 → REF1 (REF2)				120	ns
	t <sub>CTL-OND(3)</sub>	REFCTL2 → REF3 (REF4) (REF5)	C <sub>L</sub> = 20pF, R <sub>L</sub> = 200Ω			120	ns
	t <sub>CTL-OFFD(1)</sub>	CTL → SW <sub>0</sub> to SW <sub>63</sub>	C <sub>L</sub> = 20pF, R <sub>L</sub> = 1kΩ			120	ns
	t <sub>CTL-OFFD(2)</sub>	REFCTL1 → REF1 (REF2)				120	ns
	t <sub>CTL-OFFD(3)</sub>	REFCTL2 → REF3 (REF4) (REF5)	C <sub>L</sub> = 20pF, R <sub>L</sub> = 200Ω			120	ns
Maximum Clock Rise/Fall Time	t <sub>r</sub> , t <sub>f</sub>	CLK	Duty = 1/2 ± 10%	150			ns

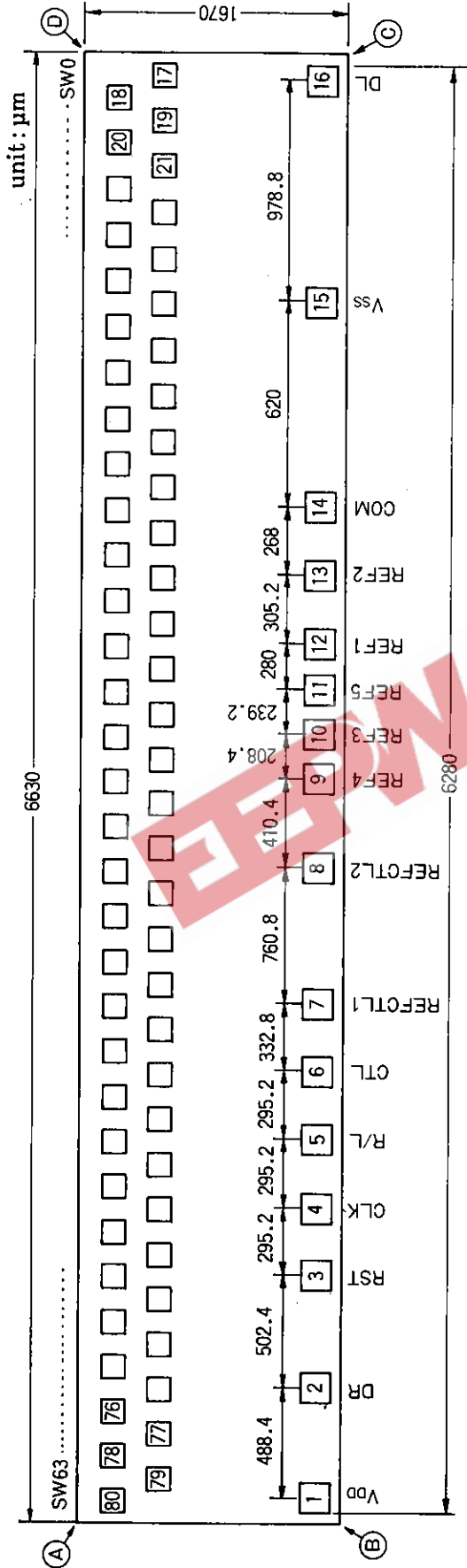
Input Data Timing Chart



Switching Waveforms



Pad Layout



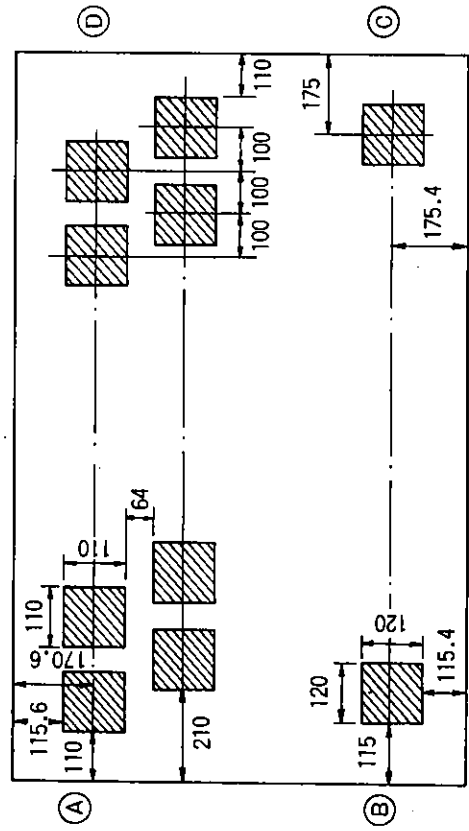
Chip size : CVD opening :  $5.63\text{mm} \times 1.67\text{mm}$

Pad size : SW63 :  $110\mu\text{m} \times 110\mu\text{m}$

VDD, DR, RST, CLK, R/L, CTL, REFCTL1, REFCTL2 }  $120\mu\text{m} \times 120\mu\text{m}$

REF4, REF3, REF5, REF1, REF2, COM, VSS, DL }

Chip thickness :  $480\mu\text{m} \pm 20\mu\text{m}$



# LC7938C

## LC7938C Pad Coordinates

Pad No.	Signal Name	X Coordinate $\mu\text{m}$	Y Coordinate $\mu\text{m}$	Pad No.	Signal Name	X Coordinate $\mu\text{m}$	Y Coordinate $\mu\text{m}$
1	VDD	-659.6	3140	41	SW39	490.4	-750
2	DR	-659.6	2651.6	42	38	664.4	-650
3	RST	-659.6	2149.2	43	37	490.4	-550
4	CLK	-659.6	1854	44	36	664.4	-450
5	R/L	-659.6	1558.8	45	35	490.4	-350
6	CTL	-659.6	1263.6	46	34	664.4	-250
7	REFCTL1	-659.6	930.8	47	33	490.4	-150
8	REFCTL2	-659.6	170	48	32	664.4	-50
9	REF4	-659.6	-240.4	49	31	490.4	50
10	REF3	-659.6	-448.8	50	30	664.4	150
11	REF5	-659.6	-688	51	29	490.4	250
12	REF1	-659.6	-968	52	28	664.4	350
13	REF2	-659.6	-1273.2	53	27	490.4	450
14	COM	-659.6	-1541.2	54	26	664.4	550
15	Vss	-659.6	-2161.2	55	25	490.4	650
16	DL	-659.6	-3140	56	24	664.4	750
17	SW63	490.4	-3150	57	23	490.4	850
18	62	664.4	-3050	58	22	664.4	950
19	61	490.4	-2950	59	21	490.4	1050
20	60	664.4	-2850	60	20	664.4	1150
21	59	490.4	-2750	61	19	490.4	1250
22	58	664.4	-2650	62	18	664.4	1350
23	57	490.4	-2550	63	17	490.4	1450
24	56	664.4	-2450	64	16	664.4	1550
25	55	490.4	-2350	65	15	490.4	1650
26	54	664.4	-2250	66	14	664.4	1750
27	53	490.4	-2150	67	13	490.4	1850
28	52	664.4	-2050	68	12	664.4	1950
29	51	490.4	-1950	69	11	490.4	2050
30	50	664.4	-1850	70	10	664.4	2150
31	49	490.4	-1750	71	9	490.4	2250
32	48	664.4	-1650	72	8	664.4	2350
33	47	490.4	-1550	73	7	490.4	2450
34	46	664.4	-1450	74	6	664.4	2550
35	45	490.4	-1350	75	5	490.4	2650
36	44	664.4	-1250	76	4	664.4	2750
37	43	490.4	-1150	77	3	490.4	2850
38	42	664.4	-1050	78	2	664.4	2950
39	41	490.4	-950	79	1	490.4	3050
40	40	664.4	-850	80	0	664.4	3150

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