Ordering number : EN3256

CMOS LSI

SANYO No.3256

LC7938C

a-Si Contact Type Image Sensor-Use Driver

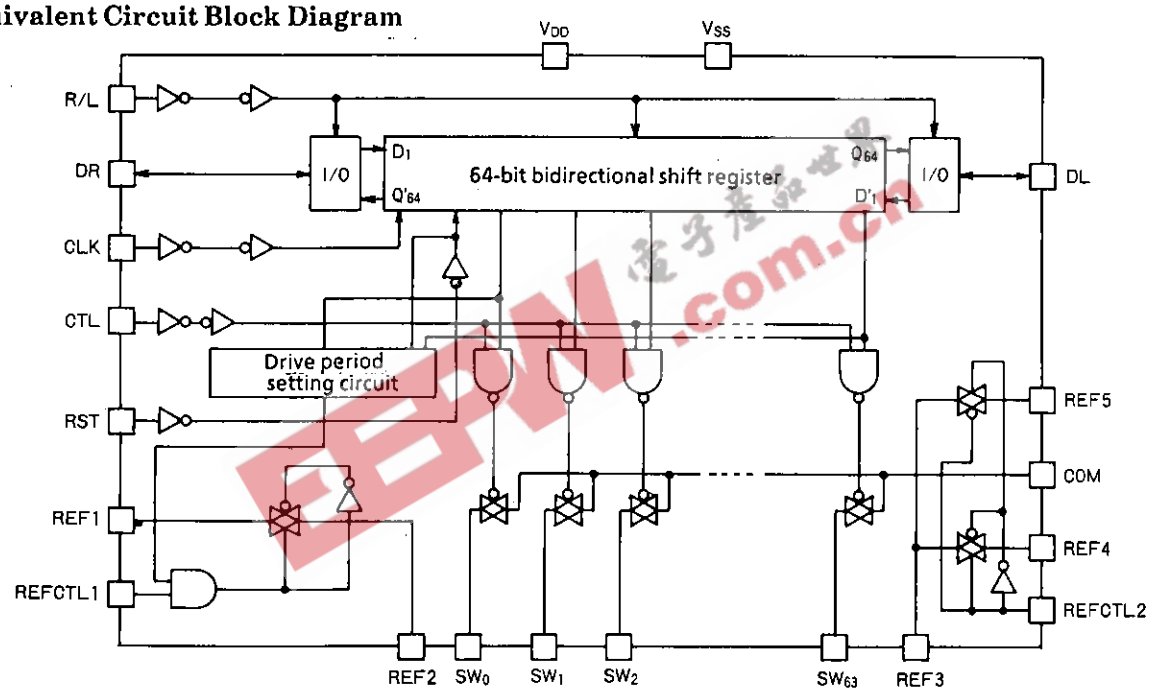
Features

- High-speed silicon gate CMOS device
- On-chip high-speed shiftable (5MHz max.) 64-bit bidirectional shift register, 64-bit sensor driver analog switch
- On-chip CTL signal (CTL) to turn OFF 64-bit sensor driver analog switch
- On-chip noise cancel analog switch

Package

Available in chip form, Chip size : 1.67mm×6.63mm, Number of pads : 80

Equivalent Circuit Block Diagram



Electrical Characteristics

The Electrical Characteristics shown below are for the LC7938C placed in our standard ceramic package.

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Limits	unit
Maximum Supply Voltage	V_{CC} max		−0.3 to +7.0	V
Input Voltage	V_{IN}		−0.3 to V_{DD}+0.3	V
Output Voltage	V_{OUT}		−0.3 to V_{DD}+0.3	V
Operating Temperature	**Topr**	(Junction temperature)	−25 to +85	°C
Storage Temperature	Tstg		−40 to +125	°C

Note) The die bond temperature and other parameters are listed in the common specification for quality assurance prepared separately.

Allowable Operating Conditions at Ta = 25 ± 2°C, V_{SS} = 0V

Parameter	Symbol	Applicable Pad Name	Conditions	Limits			unit
				min	typ	max	
Supply Voltage	V_{DD}			4.5	5.0	5.5	V
Input 'H'-Level Voltage	V_{IH}	CLK,DR,DL, RST,R/L,CTR, REFCTL1, REFCTL2		0.7V_{DD}		V_{DD}	V
Input 'L'-Level Voltage	V_{IL}			0		0.3V_{DD}	V
Operating Frequency	f_{CLK}	CLK	Duty = 1/2 ± 10%			5.0	MHz
Clock Pulse Width	$f_{\phi WH}$	CLK		100			ns
Data Setup Time	t_{DS}	CLK,DR,DL		50			ns
Data Hold Time	t_{DH}			50			ns
Reset Pulse Width	f_{RW}	RST		125			ns
Reset OFF Time	t_{RS}	RST,CLK		125			ns
Maximum Clock Rise/Fall Time	t_r, t_f	CLK	Duty = 1/2 ± 10%			150	ns

Electrical Characteristics at Ta = 25 ± 2°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V

Parameter	Symbol	Applicable Pad Name	Conditions	Limits			unit
				min	typ	max	
Output 'H'-Level Voltage	V_{OH}	DR,DL	I_{OH} = −0.3mA	V_{DD} −0.3		V_{DD}	V
Output 'L'-Level Voltage	V_{OL}		I_{OL} = 0.3mA	0		0.3	V
Analog SW ON Resistance	$R_{ON(1)}$	SW_0 to SW_{63} to COM	COM = 0V, V_{DD} = 5V, SW_0 to SW_{63} = 0.2V		1.0		kΩ
	$R_{ON(2)}$		COM = 0.2V, V_{DD} = 5V, SW_0 to SW_{63} = 0V		1.0		kΩ
	$R_{ON(3)}$	REF1 to REF2	REF1 = 0V, V_{DD} = 5V, REF2 = 0.2V		1.0		kΩ
	$R_{ON(4)}$		REF1 = 0.2V, V_{DD} = 5V, REF2 = 0V		1.0		kΩ
	$R_{ON(5)}$	REF3 to REF4	REF3 = 0V, V_{DD} = 5V, REF4 = 0.2V		200		Ω
	$R_{ON(6)}$		REF3 = 0.2V, V_{DD} = 5V, REF4 = 0V		200		Ω
	$R_{ON(7)}$	REF3 to REF5	REF3 = 0V, V_{DD} = 5V, REF5 = 0.2V		200		Ω
	$R_{ON(8)}$		REF3 = 0.2V, V_{DD} = 5V, REF5 = 0V		200		Ω

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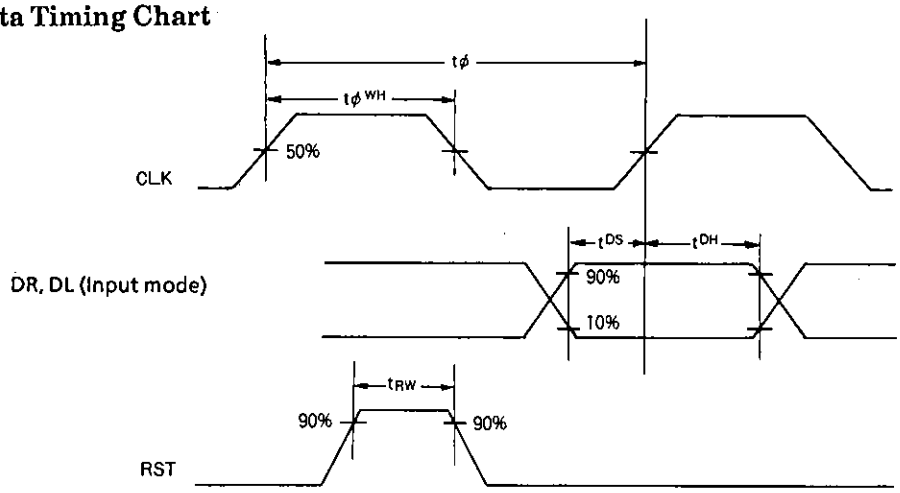
Parameter	Symbol	Applicable Pad Name	Conditions	Limits			unit
				min	typ	max	
Input/Output OFF Leakage Current	$I_{OFF(1)}$	SW_0 to SW_{63} COM	Analog SW OFF, COM=0V, SW_0 to SW_{63} = V_{DD}, sum of individual pole leakage currents V_{DD}=5V, Ta=60°C			1.0	µA
	$I_{OFF(2)}$					1.0	µA
Input Capacitance	C1	SW_0 to SW_{63}			(1.5)		pF
	C2	COM				(150)	pF
Operating Current Dissipation	I_{DD}	V_{DD}	All outputs open, f=1MHz			1	mA

( ): "Design to" value

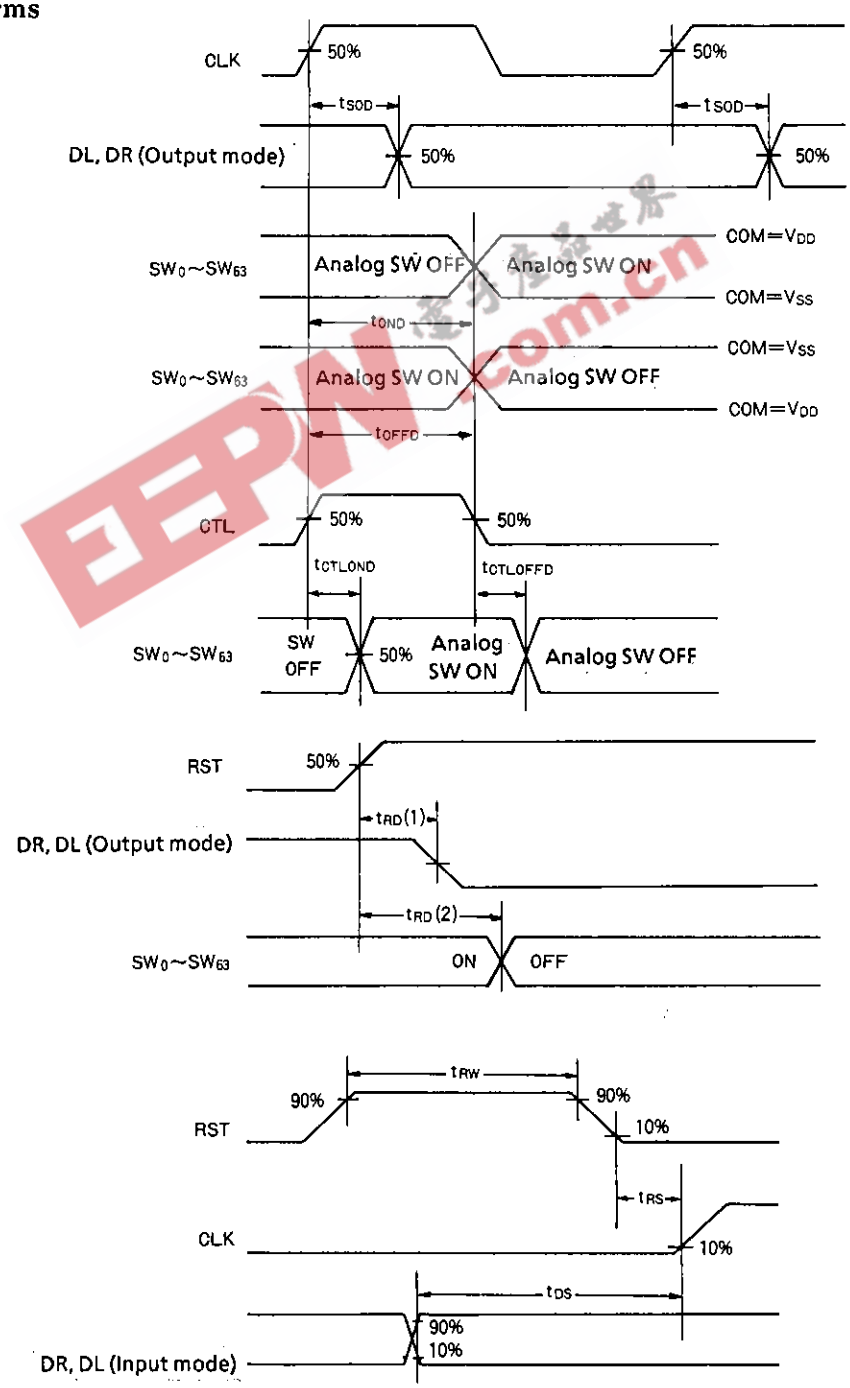
Switching Characteristics at Ta=25±2°C, V_{DD}=4.5 to 5.5V, V_{SS}=0V

Parameter	Symbol	Applicable Pad Name	Conditions	Limits			unit
				min	typ	max	
Analog SW Turn-ON Delay Time	t_{OND}	CLK→SW_0 to SW_{63}	CTL=V_{DD}, RST=V_{SS}, C_L=20pF, R_L=1kΩ			150	ns
Analog SW Turn-OFF Delay Time	t_{OFFD}	CLK→SW_0 to SW_{63}				150	ns
Data Output Delay Time	t_{SOD}	CLK→DR,DL	C_L=20pF			200	ns
Reset Signal Delay Time	$t_{RD(1)}$	RST→DR,DL	C_L=20pF			200	ns
	$t_{RD(2)}$	RST→SW_0 to SW_{63}	CTL=V_{DD}, C_L=20pF, R_L=1kΩ			200	ns
Control Signal Delay Time	$t_{CTL-OND(1)}$	CTL→SW_0 to SW_{63}	C_L=20pF, R_L=1kΩ			120	ns
	$t_{CTL-OND(2)}$	REFCTL1→REF1 (REF2)				120	ns
	$t_{CTL-OND(3)}$	REFCTL2→REF3 (REF4) (REF5)	C_L=20pF, R_L=200Ω			120	ns
	$t_{CTL-OFFD(1)}$	CTL→SW_0 to SW_{63}	C_L=20pF, R_L=1kΩ			120	ns
	$t_{CTL-OFFD(2)}$	REFCTL1→REF1 (REF2)				120	ns
	$t_{CTL-OFFD(3)}$	REFCTL2→REF3 (REF4) (REF5)	C_L=20pF, R_L=200Ω			120	ns
Maximum Clock Rise/Fall Time	t_r, t_f	CLK	Duty=1/2±10%	150			ns

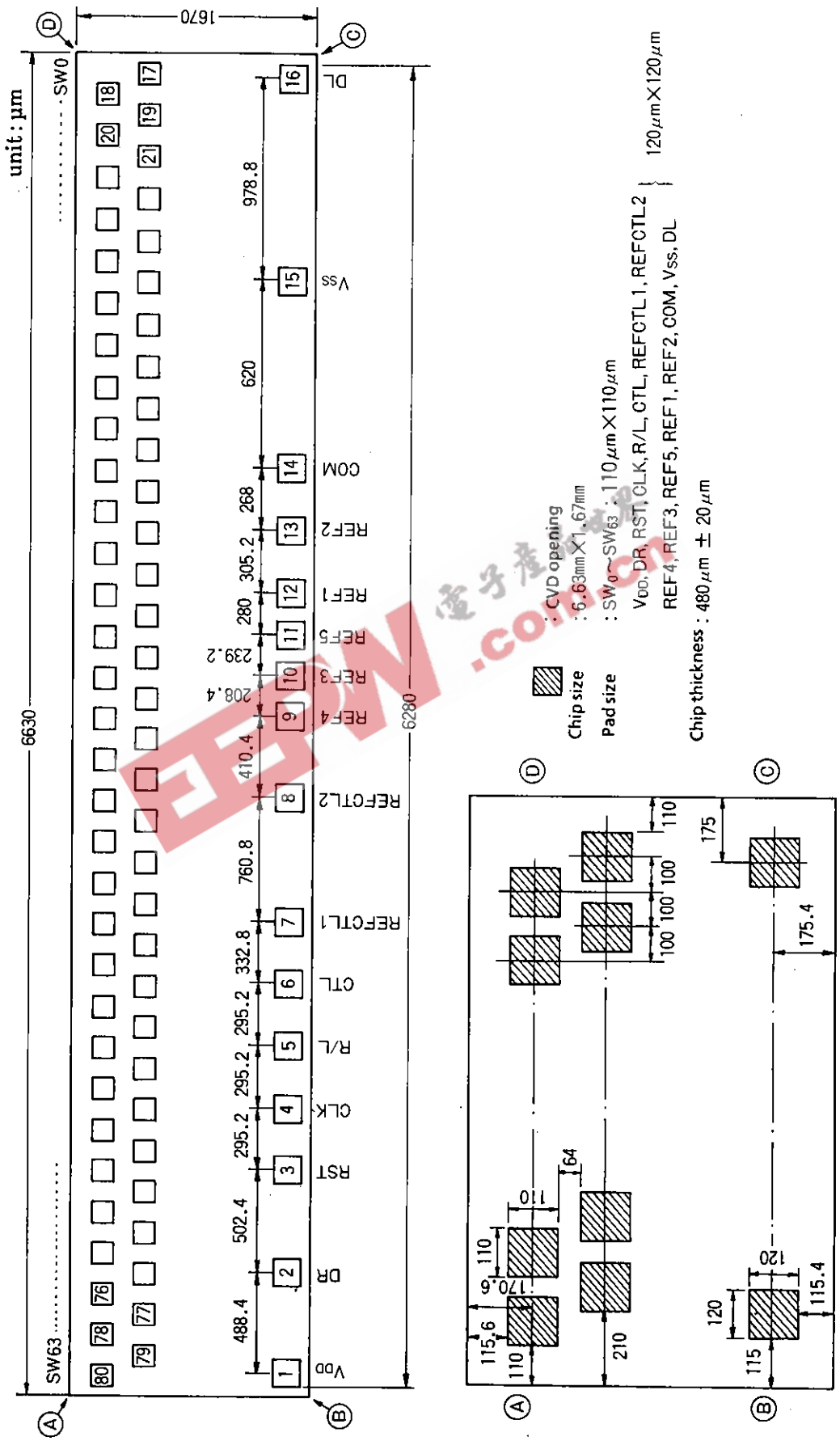
Input Data Timing Chart



Switching Waveforms



Pad Layout


unit : µm
6630
6280
1670
SW0
SW63
DL
Vss
COM
REF2
REF1
REF5
REF3
REF4
REFGTL2
REFGTL1
GTL
R/L
CLK
RST
DR
Vdd
488.4
502.4
295.2
295.2
295.2
332.2
760.8
410.4
208.4
239.2
280
305.2
268
620
978.8
Chip size : 6.63mm×1.67mm
Pad size : SW0~SW63 : 110µm×110µm
VDD, DR, RST, CLK, R/L, GTL, REFGTL1, REFGTL2
REF4, REF3, REF5, REF1, REF2, COM, Vss, DL
120µm×120µm
Chip thickness : 480µm ± 20µm

LC7938C Pad Coordinates

Pad No.	Signal Name	X Coordinate μm	Y Coordinate μm	Pad No.	Signal Name	X Coordinate μm	Y Coordinate μm
1	V_{DD}	−659.6	3140	41	SW39	490.4	−750
2	DR	−659.6	2651.6	42	38	664.4	−650
3	RST	−659.6	2149.2	43	37	490.4	−550
4	CLK	−659.6	1854	44	36	664.4	−450
5	R/L	−659.6	1558.8	45	35	490.4	−350
6	CTL	−659.6	1263.6	46	34	664.4	−250
7	REFCTL1	−659.6	930.8	47	33	490.4	−150
8	REFCTL2	−659.6	170	48	32	664.4	−50
9	REF4	−659.6	−240.4	49	31	490.4	50
10	REF3	−659.6	−448.8	50	30	664.4	150
11	REF5	−659.6	−688	51	29	490.4	250
12	REF1	−659.6	−968	52	28	664.4	350
13	REF2	−659.6	−1273.2	53	27	490.4	450
14	COM	−659.6	−1541.2	54	26	664.4	550
15	V_{SS}	−659.6	−2161.2	55	25	490.4	650
16	DL	−659.6	−3140	56	24	664.4	750
17	SW63	490.4	−3150	57	23	490.4	850
18	62	664.4	−3050	58	22	664.4	950
19	61	490.4	−2950	59	21	490.4	1050
20	60	664.4	−2850	60	20	664.4	1150
21	59	490.4	−2750	61	19	490.4	1250
22	58	664.4	−2650	62	18	664.4	1350
23	57	490.4	−2550	63	17	490.4	1450
24	56	664.4	−2450	64	16	664.4	1550
25	55	490.4	−2350	65	15	490.4	1650
26	54	664.4	−2250	66	14	664.4	1750
27	53	490.4	−2150	67	13	490.4	1850
28	52	664.4	−2050	68	12	664.4	1950
29	51	490.4	−1950	69	11	490.4	2050
30	50	664.4	−1850	70	10	664.4	2150
31	49	490.4	−1750	71	9	490.4	2250
32	48	664.4	−1650	72	8	664.4	2350
33	47	490.4	−1550	73	7	490.4	2450
34	46	664.4	−1450	74	6	664.4	2550
35	45	490.4	−1350	75	5	490.4	2650
36	44	664.4	−1250	76	4	664.4	2750
37	43	490.4	−1150	77	3	490.4	2850
38	42	664.4	−1050	78	2	664.4	2950
39	41	490.4	−950	79	1	490.4	3050
40	40	664.4	−850	80	0	664.4	3150

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