

OVERVIEW

The SM6103 is an 8-bit A/D converter fabricated in Molybdenum-gate CMOS. It features fast conversion times using a half-flash conversion method. It does not require an external sample-and-hold circuit, and can operate with or without an external microprocessor.

The SM6103 is AD7820- and ADC0820-equivalent and pin compatible. It is available in 20-pin plastic DIPs and 20-pin SOPs.

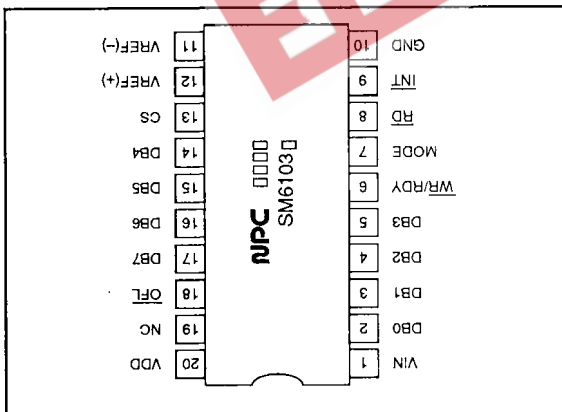
FEATURES

- 8-bit resolution
- 1.25 μ s (max) conversion time in RD mode and 0.65 μ s (max) in WR-RD mode
- AD7820- and ADC0820-equivalent and pin compatible
- External sample-and-hold circuit not required for input signals with less than 200 mV/s slew rate
- 8.5 mA (typ) current consumption (excluding VREF current)
- ± 0.5 LSB non-linearity
- ± 0.5 LSB differential non-linearity
- No external clock required
- Direct microprocessor interface
- TTL- and CMOS-compatible input/outputs
- Single 5 V supply
- 20-pin plastic DIP and 20-pin SOP
- Molybdenum-gate CMOS process

APPLICATIONS

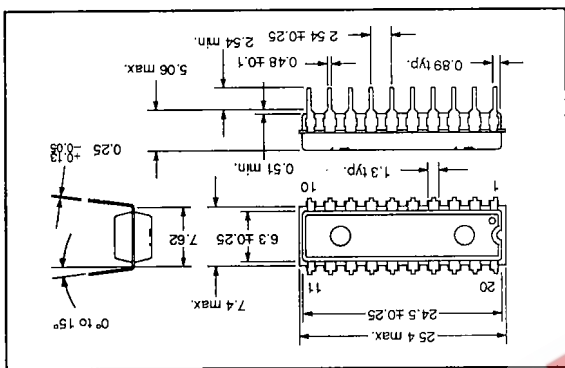
- Data acquisition systems
- Measuring instruments
- Process control

PINOUT

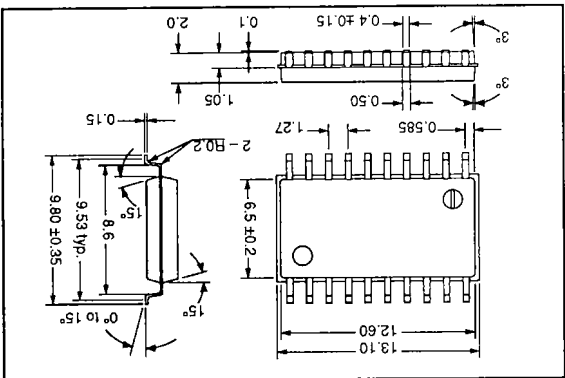


PACKAGE DIMENSIONS

Unit: mm



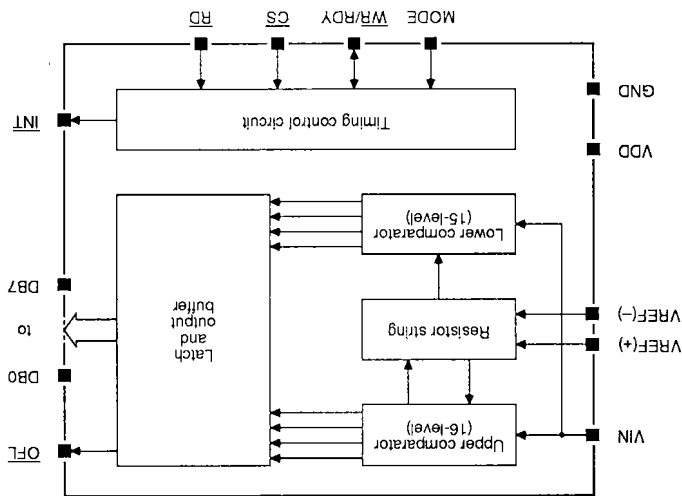
20-pin DIP (SM6103P)



20-pin SOP (SM6103S)

Number	Name	Description
1	VIN	Analog input. ($V_{REF-} \leq V_{IN} \leq V_{REF+}$)
2	DB0	Converter data output bit 0 (LSB)
3	DB1	Converter data output bit 1
4	DB2	Converter data output bit 2
5	DB3	Converter data output bit 3
6	WR/RDY	WR-RD mode (WR input): Conversion is started on the falling edge of WR. If RD is HIGH, the conversion is completed approx. 400 ns after the rising edge of WR. INT then goes LOW and RD mode (RDY output): This is an N-channel open-drain output. RDY goes LOW on the falling edge of CS. It enters a high-impedance state when conversion is completed. the data is latched.
7	MODE	Mode select input with internal pull-down resistance. RD mode when LOW or open and WR-RD mode when HIGH
8	RD	WR-RD mode: The results of the last conversion are output on DB0 to DB7 when CS and INT are LOW and RD is pulled LOW. If RD is pulled LOW before the internal conversion time has elapsed (approx. 400 ns), the conversion results are latched and output. RD mode: Conversion begins when CS is LOW and RD is pulled LOW. When conversion is completed, RDY goes high impedance and INT goes LOW.
9	INT	INT goes LOW when conversion is completed and the data is latched. INT returns HIGH on the rising edge of RD or CS
10	GND	Ground
11	VREF-	Reference voltage input (low end)
12	VREF+	Reference voltage input (high end)
13	CS	Chip select input. RD and WR propagate through the internal circuits only when CS is LOW.
14	DB4	Converter data output bit 4
15	DB5	Converter data output bit 5
16	DB6	Converter data output bit 6
17	DB7	Converter data output bit 7 (MSB)

PIN DESCRIPTION



BLOCK DIAGRAM

Number	Name	Description
18	OFL	Overflow output. When the analog input voltage is ($V_{REF+} - 0.5 \text{ LSB}$) or greater, OFL goes LOW. OFL can be used in cascade connection of 2 or more devices.
19	NC	No connection
20	VDD	Supply voltage

SPECIFICATIONS

Absolute Maximum Ratings

$V_{SS} = 0 \text{ V}$

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	-0.3 to 7.0	V
Input voltage range	V_{IN}	-0.3 to $V_{DD} + 0.3$	V
Output voltage range	V_{OUT}	-0.3 to $V_{DD} + 0.3$	V
Power dissipation	P_D	250	mW
Storage temperature range	T_{sig}	-40 to 125	deg. C
Soldering temperature	T_{sld}	260	deg. C
Soldering time	t_{sld}	10	s

Recommended Operating Conditions

Parameter	Symbol	Rating		Unit	
		min	typ		max
Supply voltage	V_{DD}	4.75	5.0	5.25	V
Operating temperature	T_{op}	0	-	70	deg. C

DC Electrical Characteristics

$V_{DD} = 5 \text{ V} \pm 5\%$, $T_a = -20$ to 70 deg. C, $V_{REF+} = 5 \text{ V} \pm 5\%$, $V_{REF-} = 0 \text{ V}$ unless otherwise noted

Parameter	Symbol	Condition	Rating		Unit	
			min	typ		max
V_{REF+} to V_{REF-} reference resistance	R_{REF}		0.5	0.85	1.3	k Ω
V_{REF+} input voltage	V_{REF+}		V_{REF-}	-	$V_{DD} + 0.3$	V
V_{REF-} input voltage	V_{REF-}		0	-	V_{REF+}	V
Analog input voltage	V_{IN}		-0.1	-	$V_{DD} + 0.1$	V
Analog input leakage current	LEAK1	$V_{IN} = 0 \text{ V to } V_{DD}$ $V_{OS} = V_{DD}$	-	± 0.1	± 3	μA
CS, WR and RD HIGH-level input voltage	V_{IH1}		2.4	-	-	V
MODE HIGH-level input voltage	V_{IH2}		3.5	-	-	V
CS, WR and RD LOW-level input voltage	V_{IL1}		-	-	0.8	V
MODE LOW-level input voltage	V_{IL2}		-	-	1.5	V

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
CS and RD HIGH-level input current	I _{HI}	V _{IH} = V _{DD}	-	-	1	µA
WR HIGH-level input current	I _{H2}	V _{IH} = V _{DD}	-	-	3	µA
MODE HIGH-level input current	I _{H3}	V _{IH} = V _{DD}	-	-	60	µA
CS, WR, RD and MODE LOW-level input current	I _L	V _{IL} = 0 V	-1	-	-	µA
DB0 to DB7, OFL and INT HIGH-level output voltage	V _{OH}	I _{source} = 360 µA	4	-	-	V
DB0 to DB7, OFL, INT and RDY LOW-level output voltage	V _{OL}	I _{sink} = 1.6 mA	-	-	0.4	V
DB0 to DB7 high-impedance leakage current	I _{LEAK2}	V _{OUT} = V _{DD} V _{OUT} = 0 V	-	-	3	µA
Current consumption	I _{DD}		-	8.5	16	mA
Analog input pin capacitance	C _{VIN}		-	25	-	pf
Logic output pin capacitance	C _{OUT}		-	5	-	pf
Logic input pin capacitance	C _{IN}		-	5	-	pf

AC Electrical Characteristics

V_{DD} = 5 V ±5%, V_{REF+} = 5 V ±5%, V_{REF-} = 0 V, t_r = t_f = 20 ns, T_a = -20 to 70 deg. C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
RD mode conversion time	t _{CRD}		-	0.8	1.25	µs
WR-RD mode conversion time	t _{WR + t_{RD} + t_{ACC1}}	t _{WR} = 220 ns, t _{RD} = 300 ns	-	-	0.65	µs
Input signal slew rate	SR		-	-	0.2	V/µs
CS to RDY delay time	t _{RDY}	RD mode	-	30	60	ns
Data access time	t _{ACC}	RD mode. See note 2.	-	t _{CRD} + 20	t _{CRD} + 40	ns
RD to INT delay time	t _{INTH}		-	50	100	ns
Data hold time	t _{DH}	See note 3.	-	50	100	ns
WR pulsewidth	t _{WR}	WR-RD mode	0.22	-	50	µs
WR to RD setup time	t _{RD}	WR-RD mode	300	-	-	ns
Data access time	t _{ACC1}	WR-RD mode. See note 2.	-	65	130	ns
WR to INT delay time	t _{INTL}	WR-RD mode	t _{RD} > t _f	-	t _f	ns
			t _{RD} > t _r	t _{RD} + 50	t _{RD} + 100	ns
Internal comparator time	t _f	WR-RD mode	-	400	650	ns
Data access time	t _{ACC2}	WR-RD mode. See note 2.	-	50	100	ns
RD pulsewidth	t _{RDPM}	WR-RD mode	150	-	-	ns
INT to data delay time	t _{IP}	WR-RD mode (stand-alone operation) See note 2.	-	20	40	ns

The SM6103 has two basic modes of operation, set by the level on MODE. If MODE is LOW or open, WR-RD mode is selected, and if MODE is HIGH, RD mode is selected. The WR-RD mode also has sub-modes of operation, according to the timing of CS, RD and WR.

If the input analog signal rises above ($V_{REF+} - 0.5$ LSB), then OFL goes LOW immediately after conversion is completed to indicate the overflow condition.

The SM6103 comprises two parallel A/D converters, one each for the upper and lower four bits of the 8-bit output.

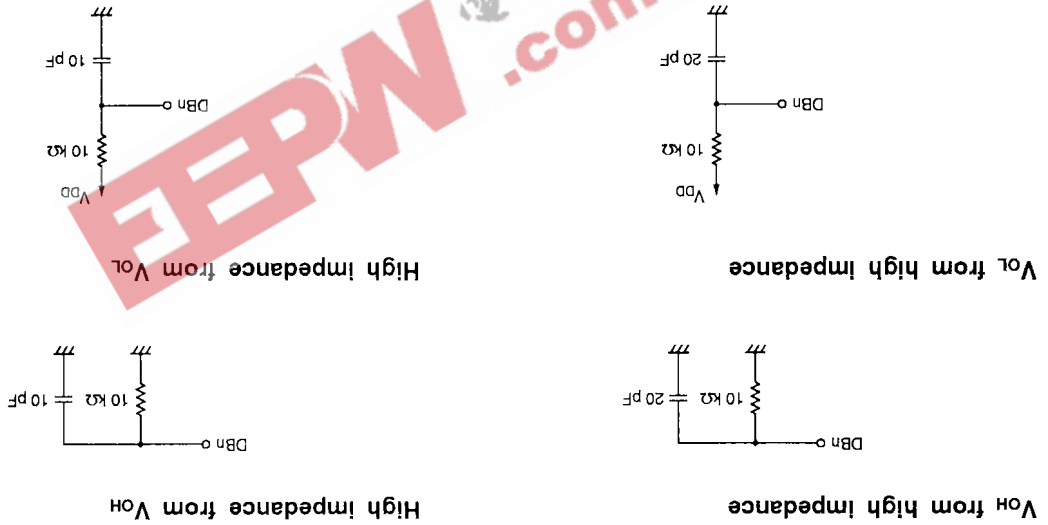
When conversion begins, the fifteen comparators (sixteen including the overflow comparator) in the upper converter (upper four bits) set the threshold levels for the fifteen comparators in the lower converter (lower four bits). The data is then latched and buffered for output.

FUNCTIONAL DESCRIPTION

Parameter	Rating			Unit
	min	typ	max	
Resolution	-	-	8	bit
Non-linearity	-	-	±0.5	LSB
Differential non-linearity	-	-	±0.5	LSB
Offset error	-	-	±0.5	LSB
Gain error	-	-	±0.5	LSB

$V_{DD} = 5 \text{ V} \pm 5\%$, $V_{REF+} = 5 \pm 0.5 \text{ V}$, $V_{REF-} = 0 \text{ V}$, $T_a = -20$ to 70 deg. C

Converter Characteristics



- All timing is measured at a signal control level of 1.6 V.
- Measured using the data access test circuits at output levels of 1.6 V.
- Measured using the data hold test circuits at output levels of 1.6 V.

Notes

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
Succeeding conversion wait time	t_p	WR-RD mode (stand-alone operation)	250	-	-	ns
		Other modes	100	-	-	

RD Mode (MODE = LOW or open)

When \overline{CS} is LOW, the CPU can strobe \overline{RD} LOW. Conversion begins on the falling edge of \overline{RD} . \overline{INT} goes LOW to signal the CPU that the conversion has completed approximately 0.8 μ s later and the data is output. If \overline{RDY} is connected to a pull-up resistor, \overline{RDY} goes HIGH on the falling edge of \overline{RD} . \overline{INT} , thus acting as the bus wait signal for the CPU. \overline{INT} returns HIGH and the outputs go high impedance on the rising edge of \overline{RD} or \overline{CS} .

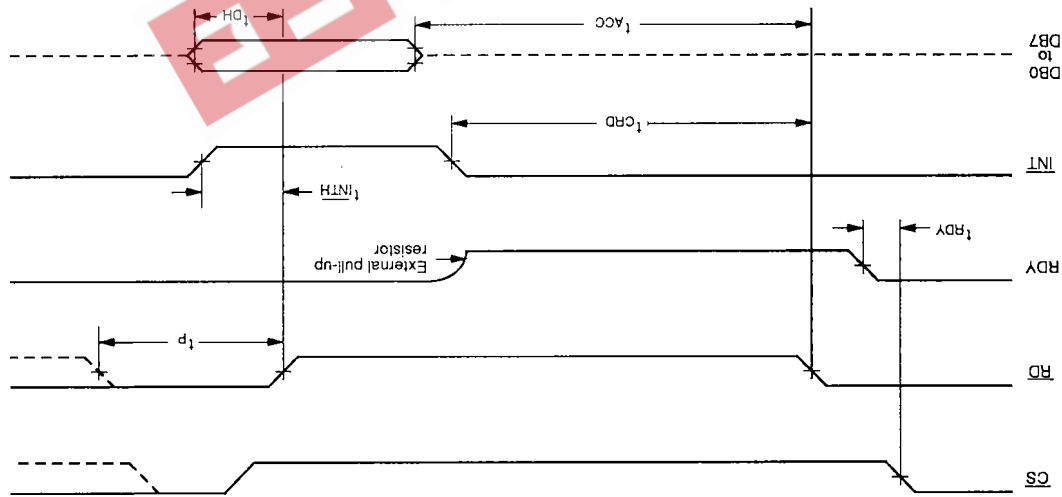


Figure 1. RD mode timing

WR-RD Mode (MODE = HIGH)

Mode A

When \overline{CS} is LOW, either \overline{RD} or \overline{WR} can be pulled LOW. Conversion of the analog input begins on the falling edge of \overline{WR} . Conversion is completed and \overline{INT} goes LOW approximately 400 ns after the rising edge of \overline{WR} , to inform the CPU that conversion is complete, and the output data is latched. When \overline{RD} goes LOW, the output data is output on $\overline{DB0}$ to $\overline{DB7}$ to be read by the CPU. In this mode, the CPU is effectively performing interrupt processing.

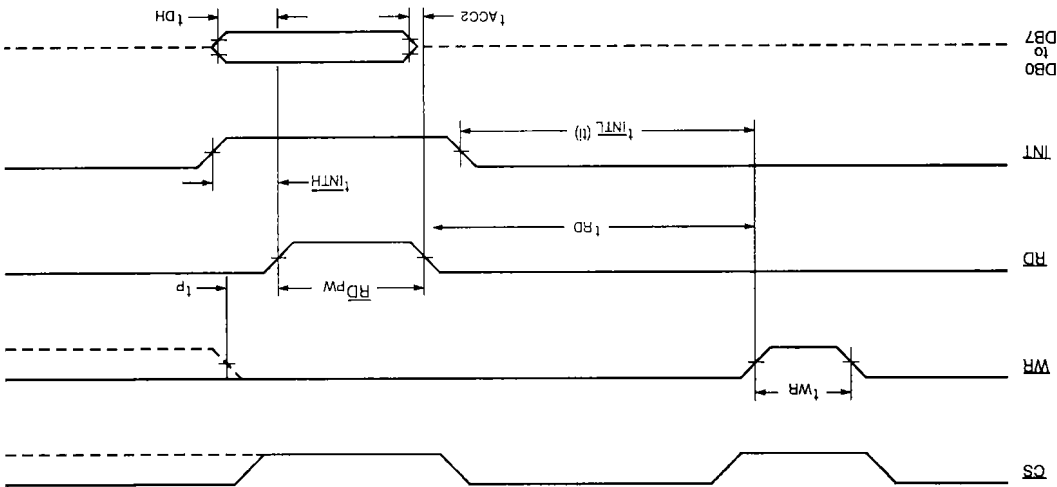


Figure 2. WR-RD mode (A) timing ($t_{RD} > t_i$)

Mode B

In mode B, \overline{RD} is pulled LOW earlier to shorten the conversion cycle. Provided that the WR-RD setup time (t_{RD}) is satisfied, approximately 300 ns, \overline{RD} can be pulled LOW to complete the conversion. In mode, the CPU is effectively polling the A/D converter.

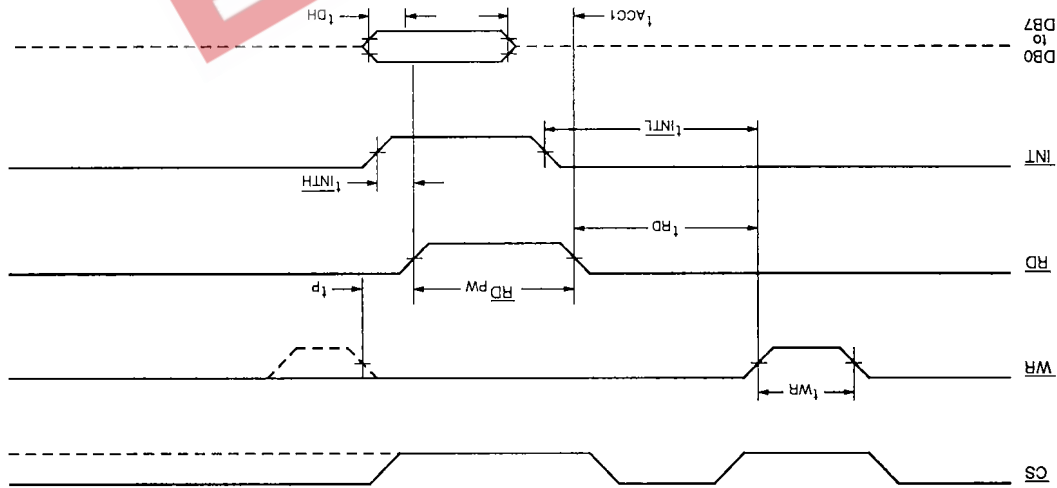


Figure 3. WR-RD mode (B) timing ($t_{RD} > t_i$)

Mode C

In mode C, \overline{CS} and \overline{RD} are both tied LOW to allow stand-alone operation (without an external microprocessor). Conversion begins on the falling edge of \overline{WR} , \overline{INT} then goes HIGH on the rising edge of \overline{WR} , \overline{INT} then goes LOW again approximately 400 ns after the rising edge of \overline{WR} , and the output data is output on $\overline{DB0}$ to $\overline{DB7}$.

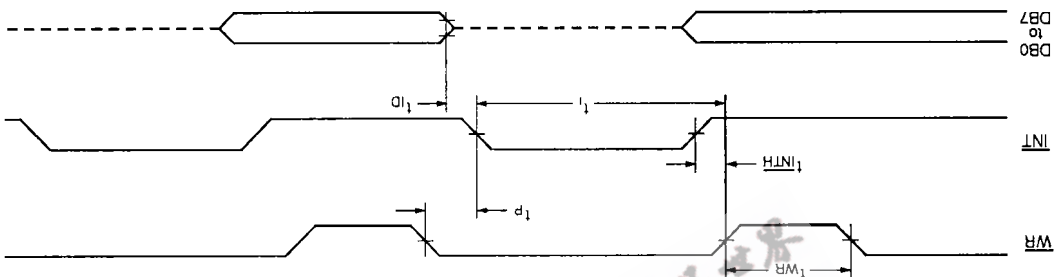
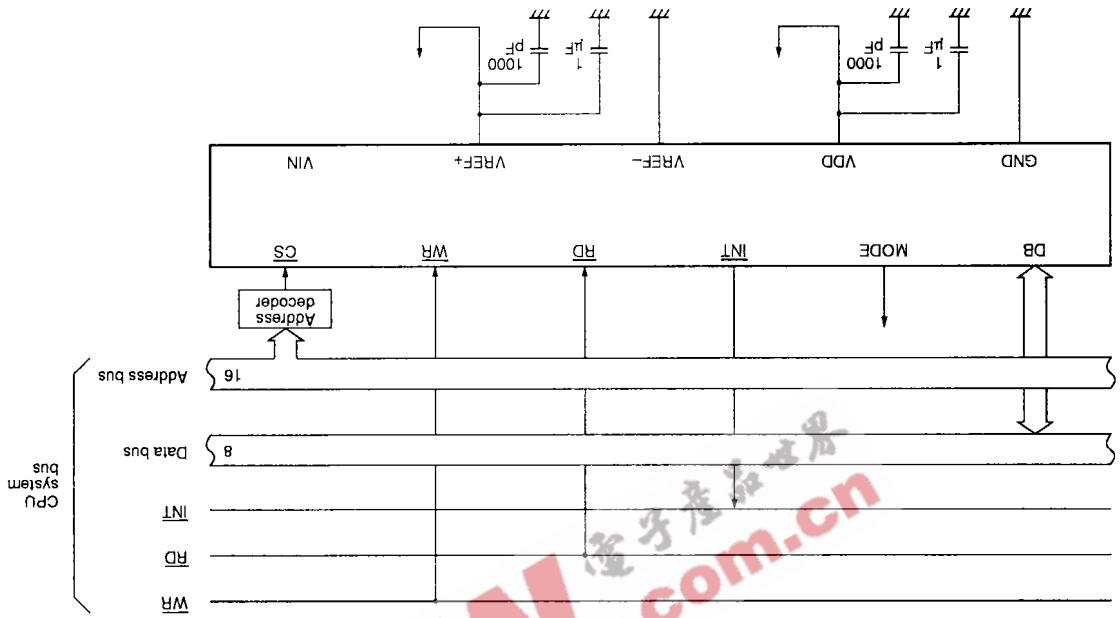
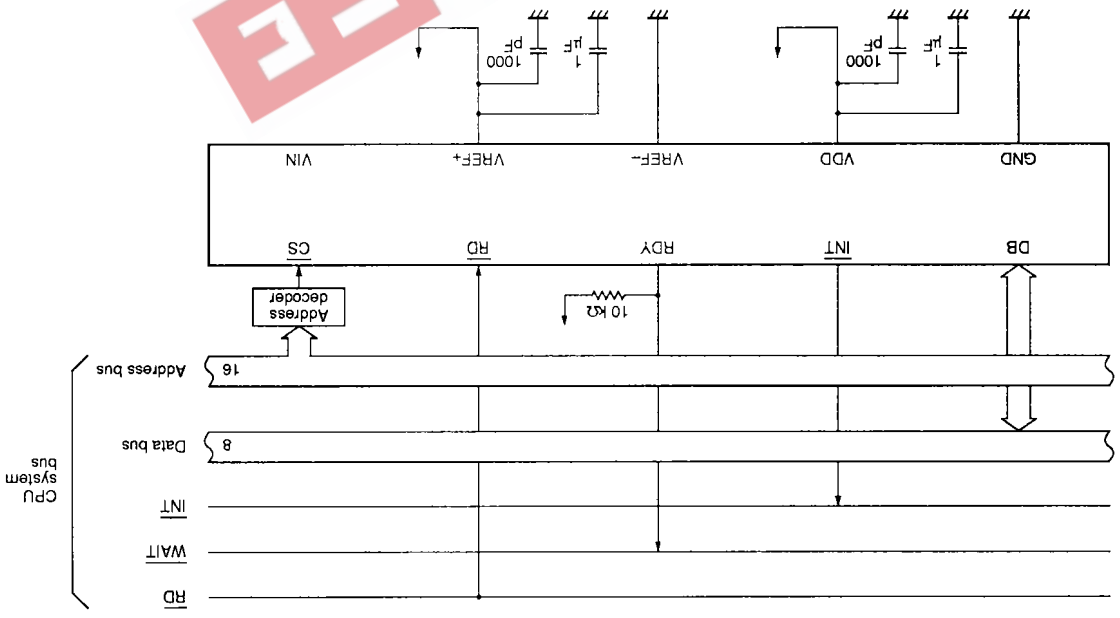


Figure 4. WR-RD mode (C) timing (stand-alone operation, $\overline{CS} = \overline{RD} = \text{LOW}$)



WR-RD mode



RD mode

Standard Configuration

