



ST230CPbF Series

Vishay High Power Products

Phase Control Thyristors (Hockey PUK Version), 410 A



TO-200AB (A-PUK)

FEATURES

- Center amplifying gate
- Metal case with ceramic insulator
- International standard case TO-200AB (A-PUK)
- Lead (Pb)-free
- Designed and qualified for industrial level



RoHS
COMPLIANT

PRODUCT SUMMARY

$I_{T(AV)}$	410 A
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TYPICAL APPLICATIONS

- DC motor controls
- Controlled DC power supplies
- AC controllers

MAJOR RATINGS AND CHARACTERISTICS

PARAMETER	TEST CONDITIONS	VALUES	UNITS
$I_{T(AV)}$		410	A
	T_{hs}	55	°C
$I_{T(RMS)}$		780	A
	T_{hs}	25	°C
I_{TSM}	50 Hz	5700	A
	60 Hz	5970	
I^2t	50 Hz	163	kA ² s
	60 Hz	149	
V_{DRM}/V_{RRM}		400 to 2000	V
t_q	Typical	100	µs
T_J		- 40 to 125	°C

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS

TYPE NUMBER	VOLTAGE CODE	V_{DRM}/V_{RRM} , MAXIMUM REPETITIVE PEAK AND OFF-STATE VOLTAGE V	V_{RSM} , MAXIMUM NON-REPETITIVE PEAK VOLTAGE V	I_{DRM}/I_{RRM} MAXIMUM AT $T_J = T_J$ MAXIMUM mA
ST230C..C	04	400	500	30
	08	800	900	
	12	1200	1300	
	14	1400	1500	
	16	1600	1700	
	18	1800	1900	
	20	2000	2100	

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ABSOLUTE MAXIMUM RATINGS						
PARAMETER	SYMBOL	TEST CONDITIONS			VALUES	UNITS
Maximum average on-state current at heatsink temperature	$I_{T(AV)}$	180° conduction, half sine wave double side (single side) cooled			410 (165)	A
					55 (85)	°C
Maximum RMS on-state current	$I_{T(RMS)}$	DC at 25 °C heatsink temperature double side cooled			780	
Maximum peak, one-cycle non-repetitive surge current	I_{TSM}	t = 10 ms	No voltage reapplied	Sinusoidal half wave, initial $T_J = T_J$ maximum	5700	A
		t = 8.3 ms			5970	
		t = 10 ms	100 % V_{RRM} reapplied		4800	
		t = 8.3 ms			5000	
Maximum I^2t for fusing	I^2t	t = 10 ms	No voltage reapplied		163	kA ² s
		t = 8.3 ms			148	
		t = 10 ms	100 % V_{RRM} reapplied		115	
		t = 8.3 ms			105	
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	t = 0.1 to 10 ms, no voltage reapplied			1630	kA ² √s
Low level value of threshold voltage	$V_{T(TO)1}$	$(16.7 \% \times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)})$, $T_J = T_J$ maximum			0.92	V
High level value of threshold voltage	$V_{T(TO)2}$	$(I > \pi \times I_{T(AV)})$, $T_J = T_J$ maximum			0.98	
Low level value of on-state slope resistance	r_{t1}	$(16.7 \% \times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)})$, $T_J = T_J$ maximum			0.88	mΩ
High level value of on-state slope resistance	r_{t2}	$(I > \pi \times I_{T(AV)})$, $T_J = T_J$ maximum			0.81	
Maximum on-state voltage	V_{TM}	$I_{pk} = 880$ A, $T_J = T_J$ maximum, $t_p = 10$ ms sine pulse			1.69	V
Maximum holding current	I_H	$T_J = 25$ °C, anode supply 12 V resistive load			600	mA
Maximum (typical) latching current	I_L				1000 (300)	

SWITCHING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum non-repetitive rate of rise of turned-on current	dI/dt	Gate drive 20 V, 20 Ω, t _r ≤ 1 μs T _J = T _J maximum, anode voltage ≤ 80 % V _{DRM}	1000	A/μs
Typical delay time	t _d	Gate current 1 A, dI _g /dt = 1 A/μs V _d = 0.67 % V _{DRM} ; T _J = 25 °C	1.0	μs
Typical turn-off time	t _q	I _{TM} = 300 A, T _J = T _J maximum, dI/dt = 20 A/μs, V _R = 50 V, dV/dt = 20 V/μs, gate 0 V 100 Ω, t _p = 500 μs	100	

BLOCKING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum critical rate of rise of off-state voltage	dV/dt	T _J = T _J maximum linear to 80 % rated V _{DRM}	500	V/μs
Maximum peak reverse and off-state leakage current	I _{RRM} , I _{DRM}	T _J = T _J maximum, rated V _{DRM} /V _{RRM} applied	30	mA



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TRIGGERING						
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES		UNITS
				TYP.	MAX.	
Maximum peak gate power	P _{GM}	T _J = T _J maximum, t _p ≤ 5 ms		10.0		W
Maximum average gate power	P _{G(AV)}	T _J = T _J maximum, f = 50 Hz, d% = 50		2.0		
Maximum peak positive gate current	I _{GM}	T _J = T _J maximum, t _p ≤ 5 ms		3.0		A
Maximum peak positive gate voltage	+ V _{GM}	T _J = T _J maximum, t _p ≤ 5 ms		20		V
Maximum peak negative gate voltage	- V _{GM}			5.0		
DC gate current required to trigger	I _{GT}	T _J = - 40 °C	Maximum required gate trigger/ current/voltage are the lowest value which will trigger all units 12 V anode to cathode applied	180	-	
		T _J = 25 °C		90	150	mA
		T _J = 125 °C		40	-	
DC gate voltage required to trigger	V _{GT}	T _J = - 40 °C		2.9	-	V
		T _J = 25 °C		1.8	3.0	
		T _J = 125 °C		1.2	-	
DC gate current not to trigger	I _{GD}	T _J = T _J maximum	Maximum gate current/voltage not to trigger is the maximum value which will not trigger any unit with rated V _{DRM} anode to cathode applied	10		mA
DC gate voltage not to trigger	V _{GD}			0.25		V

THERMAL AND MECHANICAL SPECIFICATIONS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum operating temperature range	T_J		- 40 to 125	°C
Maximum storage temperature range	T_{Stg}		- 40 to 150	
Maximum thermal resistance, junction to heatsink	R_{thJ-hs}	DC operation single side cooled	0.17	K/W
		DC operation double side cooled	0.08	
Maximum thermal resistance, case to heatsink	R_{thC-hs}	DC operation single side cooled	0.033	
		DC operation double side cooled	0.017	
Mounting force, ± 10 %			4900 (500)	N (kg)
Approximate weight			50	g
Case style		See dimensions - link at the end of datasheet	TO-200AB (A-PUK)	

ΔR_{thJC} CONDUCTION						
CONDUCTION ANGLE	SINUSOIDAL CONDUCTION		RECTANGULAR CONDUCTION		TEST CONDITIONS	UNITS
	SINGLE SIDE	DOUBLE SIDE	SINGLE SIDE	DOUBLE SIDE		
180°	0.015	0.017	0.011	0.011	T _J = T _J maximum	K/W
120°	0.018	0.019	0.019	0.019		
90°	0.024	0.024	0.026	0.026		
60°	0.035	0.035	0.036	0.036		
30°	0.060	0.060	0.060	0.061		

Note

- The table above shows the increment of thermal resistance R_{thJC} when devices operate at different conduction angles than DC

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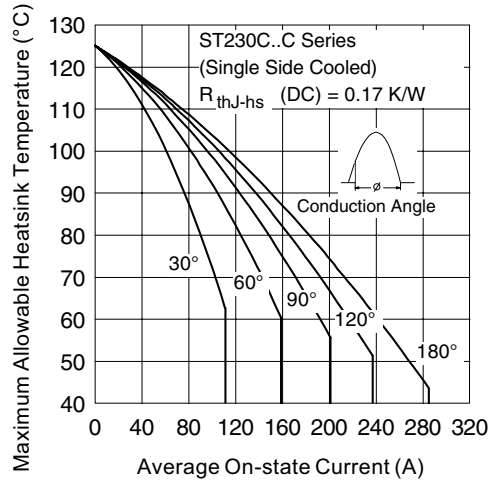


Fig. 1 - Current Ratings Characteristics

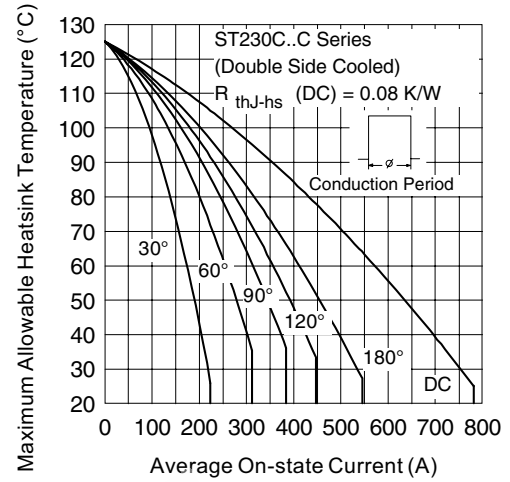


Fig. 4 - Current Ratings Characteristics

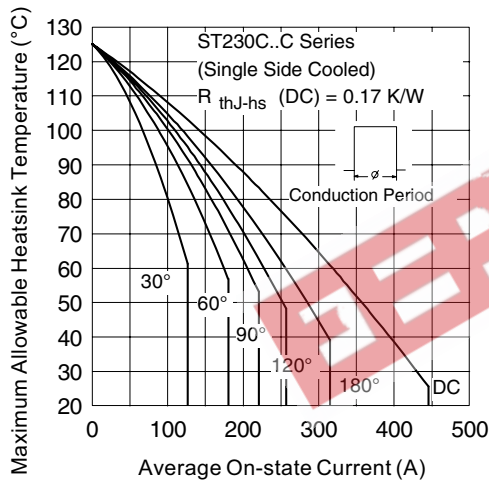


Fig. 2 - Current Ratings Characteristics

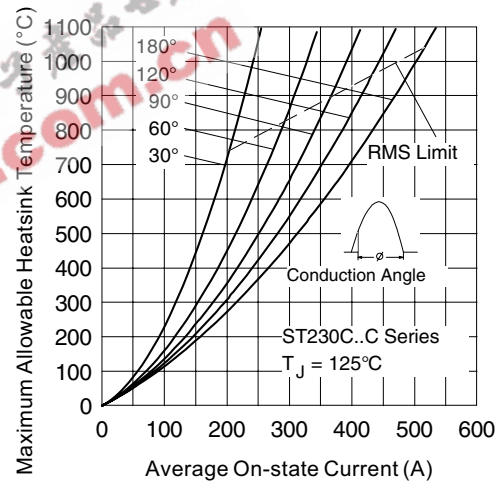


Fig. 5 - On-State Power Loss Characteristics

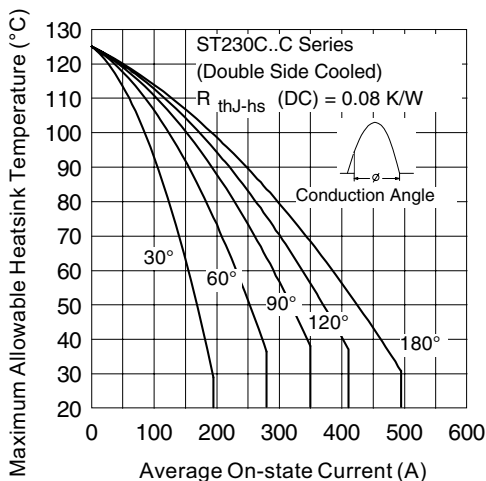


Fig. 3 - Current Ratings Characteristics

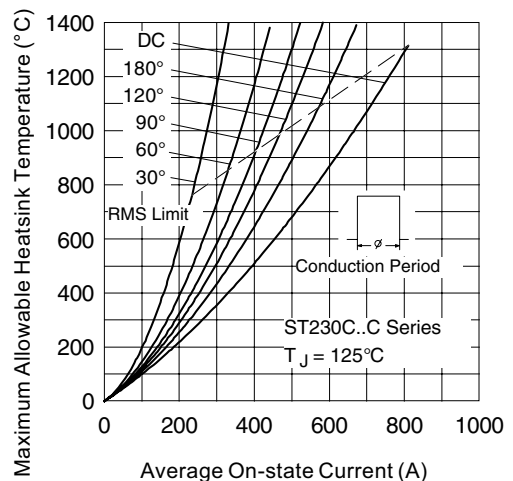


Fig. 6 - On-State Power Loss Characteristics



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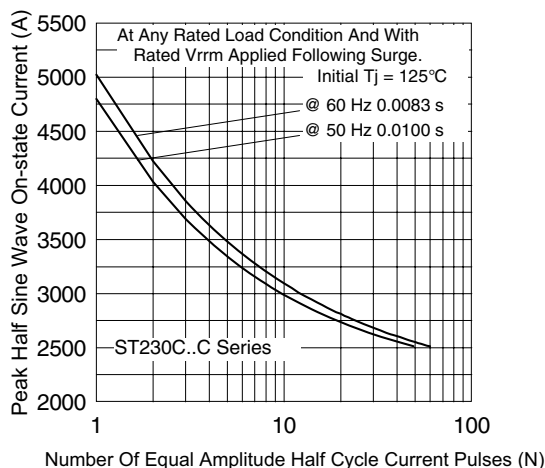


Fig. 7 - Maximum Non-Repetitive Surge Current Single and Double Side Cooled

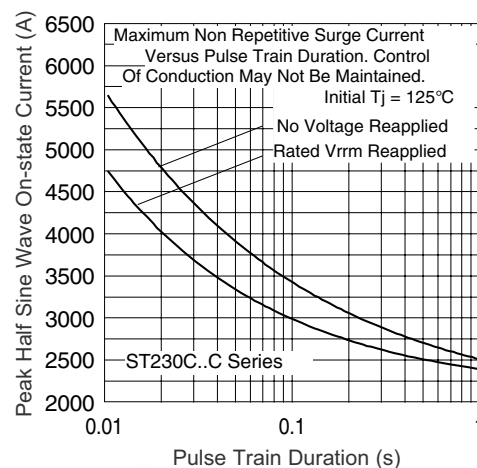


Fig. 8 - Maximum Non-Repetitive Surge Current Single and Double Side Cooled

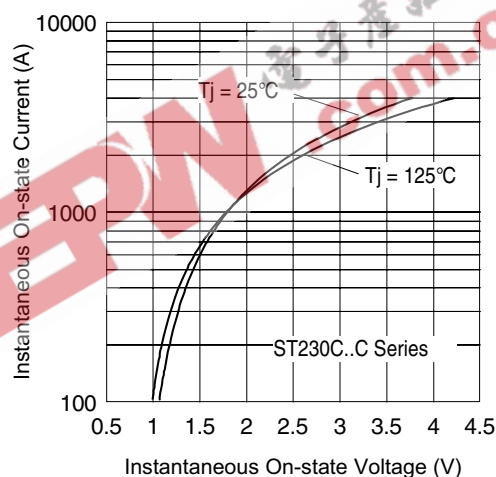


Fig. 9 - On-State Voltage Drop Characteristics

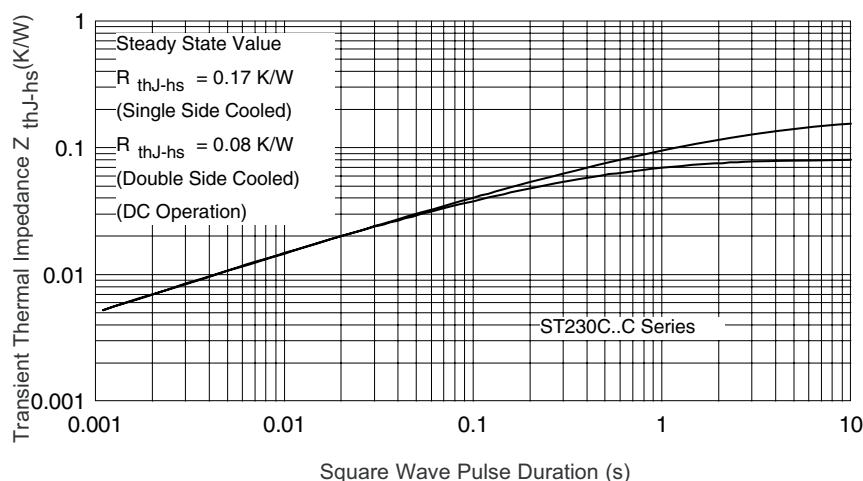


Fig. 10 - Thermal Impedance Z_{thJ-hs} Characteristics

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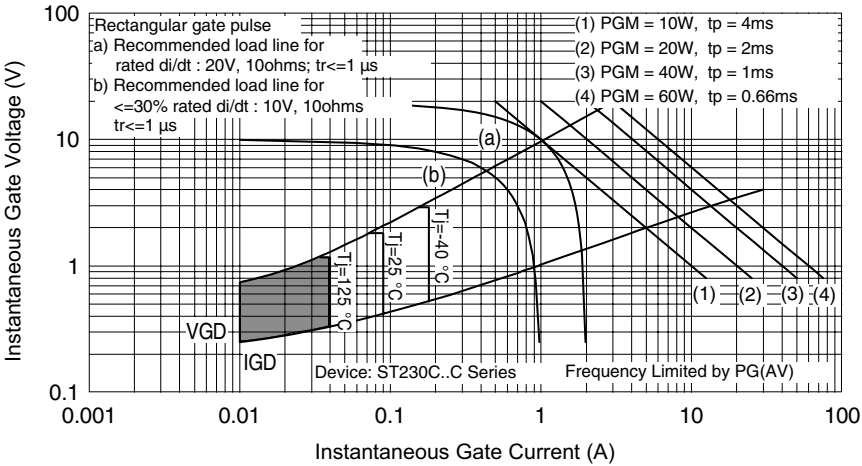


Fig. 11 - Gate Characteristics

ORDERING INFORMATION TABLE

Device code	ST	23	0	C	20	C	1	PbF
	①	②	③	④	⑤	⑥	⑦	⑧

- | | | |
|---|---|--|
| ① | - | Thyristor |
| ② | - | Essential part number |
| ③ | - | 0 = Converter grade |
| ④ | - | C = Ceramic PUK |
| ⑤ | - | Voltage code x 100 = V_{RRM} (see Voltage Ratings table) |
| ⑥ | - | C = PUK case TO-200AB (A-PUK) |
| ⑦ | - | 0 = Eyelet terminals (gate and auxiliary cathode unsoldered leads)
1 = Fast-on terminals (gate and auxiliary cathode unsoldered leads)
2 = Eyelet terminals (gate and auxiliary cathode soldered leads)
3 = Fast-on terminals (gate and auxiliary cathode soldered leads) |
| ⑧ | - | Critical dV/dt: • None = 500 V/µs (Standard selection)
• L = 1000 V/µs (Special selection) |
| ⑨ | - | Lead (Pb)-free |

LINKS TO RELATED DOCUMENTS	
Dimensions	http://www.vishay.com/doc?95074



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