



# BTA/BTB12 and T12 Series

SNUBBERLESS™, LOGIC LEVEL & STANDARD

12A TRIACS

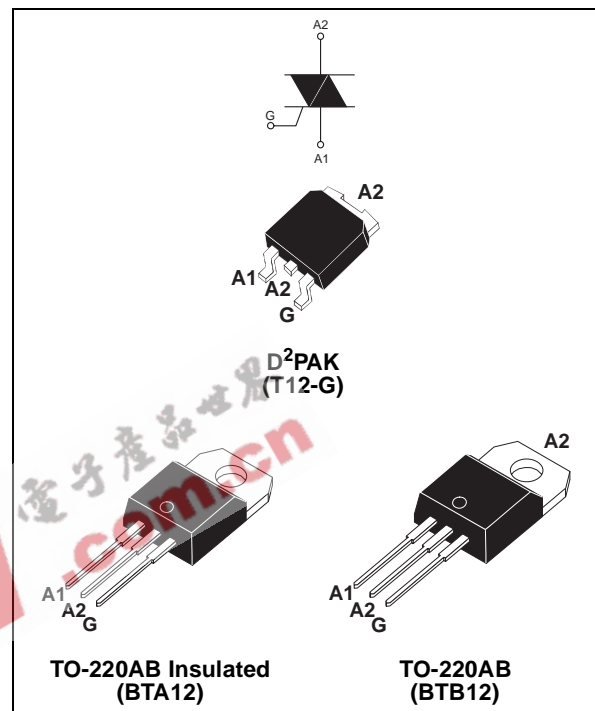
## MAIN FEATURES:

Symbol	Value	Unit
$I_{T(RMS)}$	12	A
$V_{DRM}/V_{RRM}$	600 and 800	V
$I_{GT}(Q_1)$	5 to 50	mA

## DESCRIPTION

Available either in through-hole or surface-mount packages, the BTA/BTB12 and T12 triac series is suitable for general purpose AC switching. They can be used as an ON/OFF function in applications such as static relays, heating regulation, induction motor starting circuits... or for phase control operation in light dimmers, motor speed controllers,...

The snubberless versions (BTA/BTB...W and T12 series) are specially recommended for use on inductive loads, thanks to their high commutation performances. Logic level versions are designed to interface directly with low power drivers such as microcontrollers. By using an internal ceramic pad, the BTA series provides voltage insulated tab (rated at 2500V RMS) complying with UL standards (File ref.: E81734)



## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter			Value	Unit	
$I_{T(RMS)}$	RMS on-state current (full sine wave)	D²PAK/TO-220AB	$T_c = 105^\circ\text{C}$	12	A	
		TO-220AB Ins.	$T_c = 90^\circ\text{C}$			
$I_{TSM}$	Non repetitive surge peak on-state current (full cycle, $T_j$ initial = $25^\circ\text{C}$ )	F = 50 Hz	t = 20 ms	120	A	
		F = 60 Hz	t = 16.7 ms	126		
$I^2t$	$I^2t$ Value for fusing	tp = 10 ms		78	$\text{A}^2\text{s}$	
dl/dt	Critical rate of rise of on-state current $I_G = 2 \times I_{GT}$ , tr ≤ 100 ns	F = 120 Hz	$T_j = 125^\circ\text{C}$	50	A/μs	
$V_{DSM}/V_{RSM}$	Non repetitive surge peak off-state voltage	tp = 10 ms	$T_j = 25^\circ\text{C}$	$V_{DRM}/V_{RRM} + 100$	V	
$I_{GM}$	Peak gate current	tp = 20 μs	$T_j = 125^\circ\text{C}$	4	A	
$P_{G(AV)}$	Average gate power dissipation	$T_j = 125^\circ\text{C}$		1	W	
$T_{stg}$ $T_j$	Storage junction temperature range Operating junction temperature range				- 40 to + 150 - 40 to + 125	$^\circ\text{C}$

## BTA/BTB12 and T12 Series

### ELECTRICAL CHARACTERISTICS (T<sub>j</sub> = 25°C, unless otherwise specified)

#### ■ SNUBBERLESS™ and LOGIC LEVEL (3 Quadrants)

Symbol	Test Conditions	Quadrant		BTA/BTB12					Unit
				T12	TW	SW	CW	BW	
I <sub>GT</sub> (1)	V <sub>D</sub> = 12 V R <sub>L</sub> = 30 Ω	I - II - III	MAX.	35	5	10	35	50	mA
V <sub>GT</sub>			MAX.	1.3					V
V <sub>GD</sub>	V <sub>D</sub> = V <sub>DRM</sub> R <sub>L</sub> = 3.3 kΩ T <sub>j</sub> = 125°C	I - II - III	MIN.	0.2					V
I <sub>H</sub> (2)	I <sub>T</sub> = 100 mA		MAX.	35	10	15	35	50	mA
I <sub>L</sub>	I <sub>G</sub> = 1.2 I <sub>GT</sub>	I - III	MAX.	50	10	25	50	70	mA
		II		60	15	30	60	80	
dV/dt (2)	V <sub>D</sub> = 67 %V <sub>DRM</sub> gate open T <sub>j</sub> = 125°C		MIN.	500	20	40	500	1000	V/μs
(di/dt) <sub>c</sub> (2)	(dV/dt) <sub>c</sub> = 0.1 V/μs T <sub>j</sub> = 125°C		MIN.	-	3.5	6.5	-	-	A/ms
	(dV/dt) <sub>c</sub> = 10 V/μs T <sub>j</sub> = 125°C			-	1	2.9	-	-	
	Without snubber T <sub>j</sub> = 125°C			6.5	-	-	6.5	12	

#### ■ STANDARD (4 Quadrants)

Symbol	Test Conditions	Quadrant		BTA/BTB12		Unit
				C	B	
I <sub>GT</sub> (1)	V <sub>D</sub> = 12 V R <sub>L</sub> = 30 Ω	I - II - III IV	MAX.	25 50	50 100	mA
V <sub>GT</sub>			MAX.	1.3		V
V <sub>GD</sub>	V <sub>D</sub> = V <sub>DRM</sub> R <sub>L</sub> = 3.3 kΩ T <sub>j</sub> = 125°C	ALL	MIN.	0.2		V
I <sub>H</sub> (2)	I <sub>T</sub> = 500 mA		MAX.	25	50	mA
I <sub>L</sub>	I <sub>G</sub> = 1.2 I <sub>GT</sub>	I - III - IV	MAX.	40	50	mA
		II		80	100	
dV/dt (2)	V <sub>D</sub> = 67 %V <sub>DRM</sub> gate open T <sub>j</sub> = 125°C		MIN.	200	400	V/μs
(dV/dt) <sub>c</sub> (2)	(di/dt) <sub>c</sub> = 5.3 A/ms T <sub>j</sub> = 125°C		MIN.	5	10	V/μs

### STATIC CHARACTERISTICS

Symbol	Test Conditions	Value	Unit
V <sub>T</sub> (2)	I <sub>TM</sub> = 17 A tp = 380 μs	T <sub>j</sub> = 25°C MAX.	1.55 V
V <sub>to</sub> (2)	Threshold voltage	T <sub>j</sub> = 125°C MAX.	0.85 V
R <sub>d</sub> (2)	Dynamic resistance	T <sub>j</sub> = 125°C MAX.	35 mΩ
I <sub>DRM</sub> I <sub>RDM</sub>	V <sub>DRM</sub> = V <sub>RDM</sub>	T <sub>j</sub> = 25°C	5 μA
		T <sub>j</sub> = 125°C	1 mA

**Note 1:** minimum I<sub>GT</sub> is guaranteed at 5% of I<sub>GT</sub> max.

**Note 2:** for both polarities of A2 referenced to A1

**THERMAL RESISTANCES**

Symbol	Parameter		Value	Unit	
$R_{th(j-c)}$	Junction to case (AC)		D <sup>2</sup> PAK/TO-220AB	1.4	°C/W
			TO-220AB Insulated	2.3	
$R_{th(j-a)}$	Junction to ambient	S = 1 cm <sup>2</sup>	D <sup>2</sup> PAK	45	°C/W
			TO-220AB TO-220AB Insulated	60	

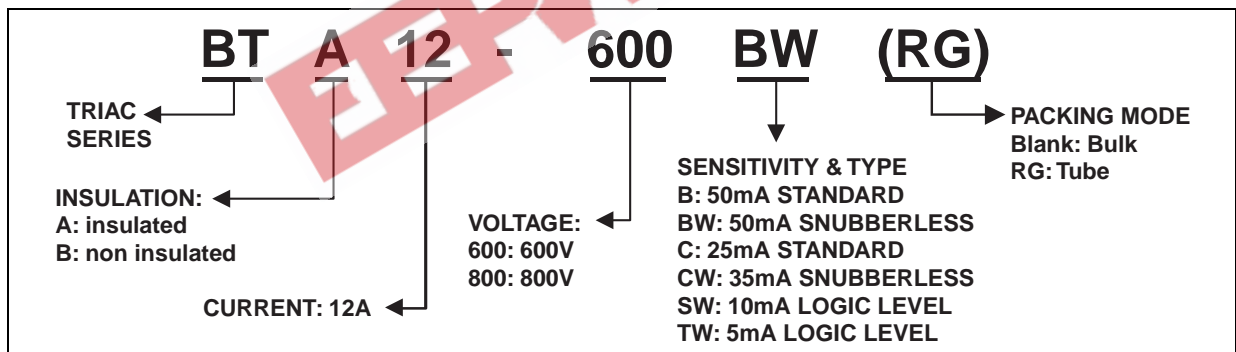
S = Copper surface under tab

**PRODUCT SELECTOR**

Part Number	Voltage (xxx)		Sensitivity	Type	Package
	600 V	800 V			
BTA/BTB12-xxxB	X	X	50 mA	Standard	TO-220AB
BTA/BTB12-xxxBW	X	X	50 mA	Snubberless	TO-220AB
BTA/BTB12-xxxC	X	X	25 mA	Standard	TO-220AB
BTA/BTB12-xxxCW	X	X	35 mA	Snubberless	TO-220AB
BTA/BTB12-xxxSW	X	X	10 mA	Logic level	TO-220AB
BTA/BTB12-xxxTW	X	X	5 mA	Logic Level	TO-220AB
T1235-xxxG	X	X	35 mA	Snubberless	D <sup>2</sup> PAK

BTB: non insulated TO-220AB package

**ORDERING INFORMATION**



# BTA/BTB12 and T12 Series

## OTHER INFORMATION

Part Number	Marking	Weight	Base quantity	Packing mode
BTA/BTB12-xxxxyz	BTA/BTB12-xxxxyz	2.3 g	250	Bulk
BTA/BTB12-xxxxyzRG	BTA/BTB12-xxxxyz	2.3 g	50	Tube
T1235-xxxG	T1235xxxG	1.5 g	50	Tube
T1235-xxxG-TR	T1235xxxG	1.5 g	1000	Tape & reel

Note: xxx = voltage, yy = sensitivity, z = type

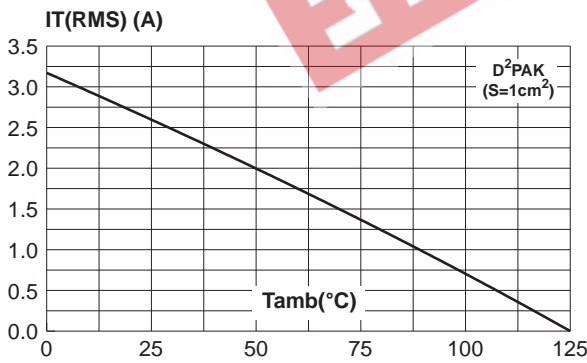
**Fig. 1:** Maximum power dissipation versus RMS on-state current (full cycle).



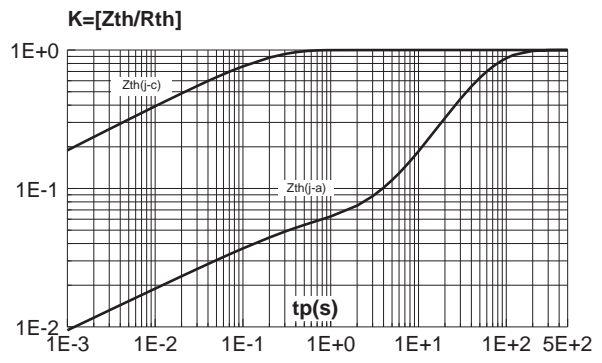
**Fig. 2-1:** RMS on-state current versus case temperature (full cycle).



**Fig. 2-2:** RMS on-state current versus ambient temperature (printed circuit board FR4, copper thickness: 35µm), full cycle.



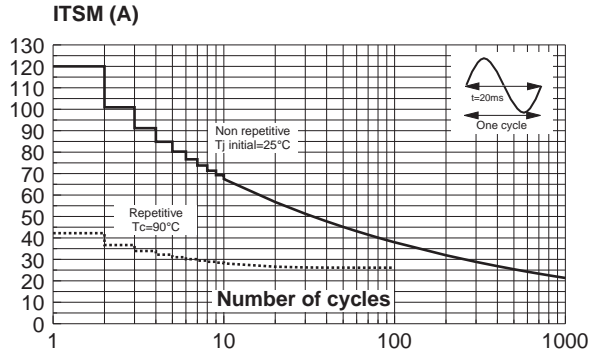
**Fig. 3:** Relative variation of thermal impedance versus pulse duration.



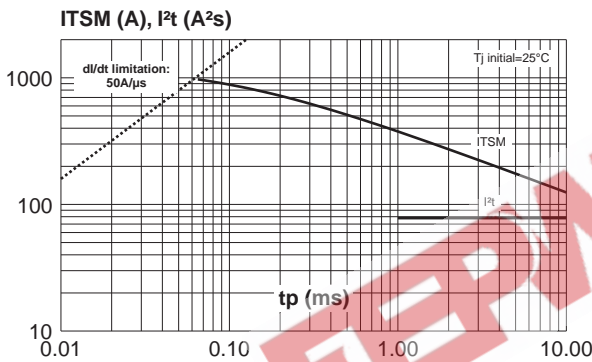
**Fig. 4:** On-state characteristics (maximum values).



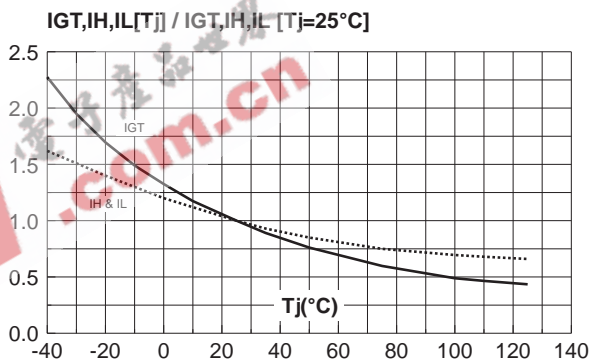
**Fig. 5:** Surge peak on-state current versus number of cycles.



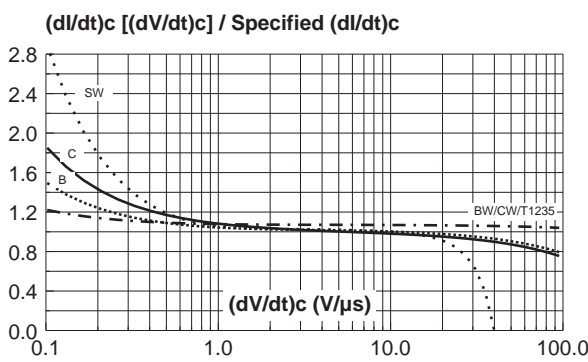
**Fig. 6:** Non-repetitive surge peak on-state current for a sinusoidal pulse with width  $t_p < 10\text{ms}$ , and corresponding value of  $I^2t$ .



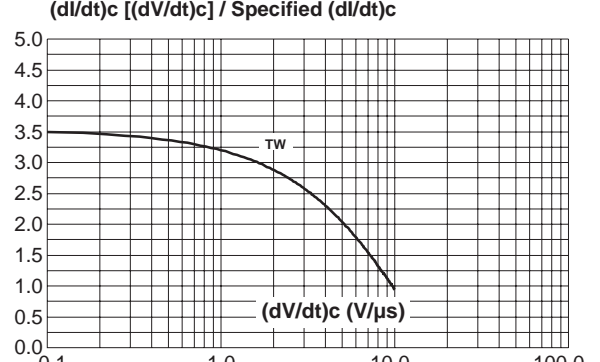
**Fig. 7:** Relative variation of gate trigger current, holding current and latching current versus junction temperature (typical values).



**Fig. 8-1:** Relative variation of critical rate of decrease of main current versus  $(dV/dt)_c$  (typical values) (BW/CW/T1235).



**Fig. 8-2:** Relative variation of critical rate of decrease of main current versus  $(dV/dt)_c$  (typical values) (TW).



## BTA/BTB12 and T12 Series

**Fig. 9:** Relative variation of critical rate of decrease of main current versus junction temperature.

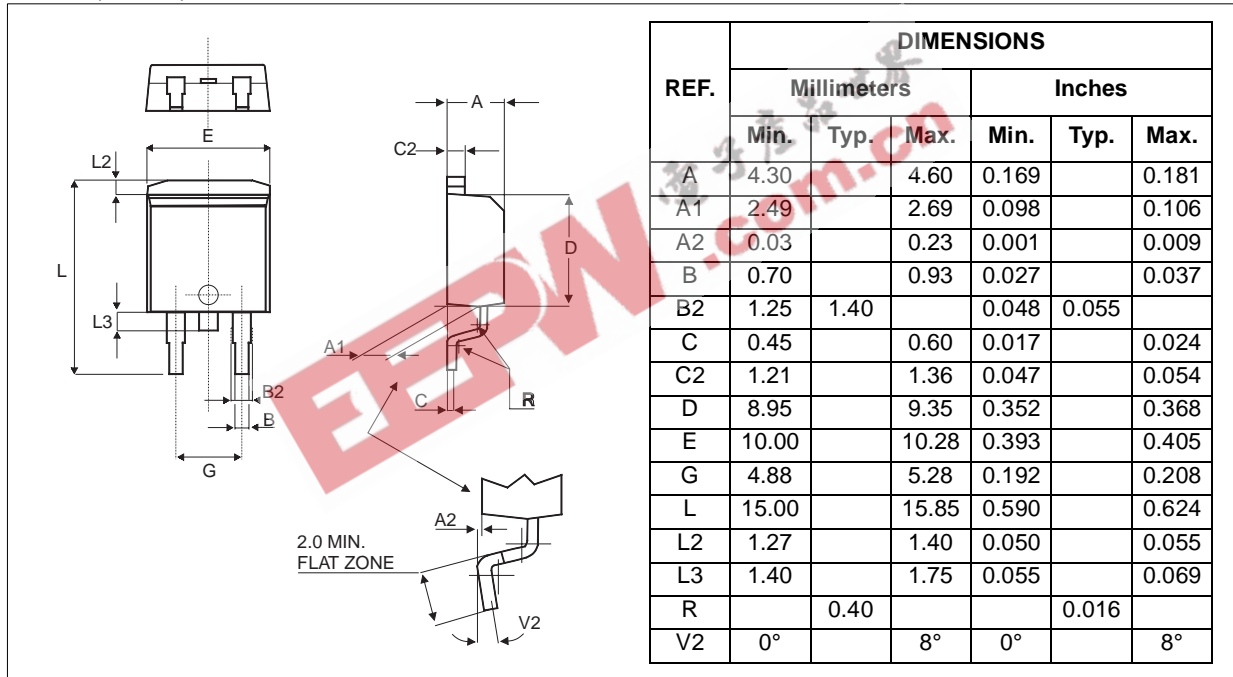


**Fig. 10:** D<sup>2</sup>PAK Thermal resistance junction to ambient versus copper surface under tab (printed circuit board FR4, copper thickness: 35 μm).



### PACKAGE MECHANICAL DATA

D<sup>2</sup>PAK (Plastic)



### FOOTPRINT DIMENSIONS (in millimeters)

D<sup>2</sup>PAK (Plastic)



PACKAGE MECHANICAL DATA

TO-220AB / TO-220AB Ins.



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2002 STMicroelectronics - Printed in Italy - All Rights Reserved

STMicroelectronics GROUP OF COMPANIES  
 Australia - Brazil - Canada - China - Finland - France - Germany  
 Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore  
 Spain - Sweden - Switzerland - United Kingdom - United States.

<http://www.st.com>

