FAIRCHILD SEMICONDUCTOR™

October 1987
Revised July 1999

CD40174BC • CD40175BC
Hex D-Type Flip-Flop • Quad D-Type Flip-Flop

General Description

The CD40174BC consists of six positive-edge triggered D-type flip-flops; the true outputs from each flip-flop are externally available. The CD40175BC consists of four positive-edge triggered D-type flip-flops; both the true and complement outputs from each flip-flop are externally available.

All flip-flops are controlled by a common clock and a common clear. Information at the D inputs meeting the set-up time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. The clearing operation, enabled by a negative pulse at Clear input, clears all Q outputs to logical "0" and $\overline{Q}$ s (CD40175BC only) to logical "1".

All inputs are protected from static discharge by diode clamps to V_{DD} and V_{SS}.

Features

- Wide supply voltage range: 3V to 15V
- High noise immunity: 0.45 V_{DD} (typ.)
- Low power TTL compatibility:
  fan out of 2 driving 74L or 1 driving 74 LS
- Equivalent to MC14174B, MC14175B
- Equivalent to MM74C174, MM74C175

Ordering Code:

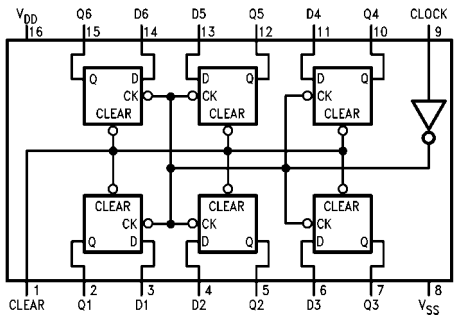
Order Number	Package Number	Package Description
CD40174BCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body
CD40174BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
CD40175BCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body
CD40175BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagrams

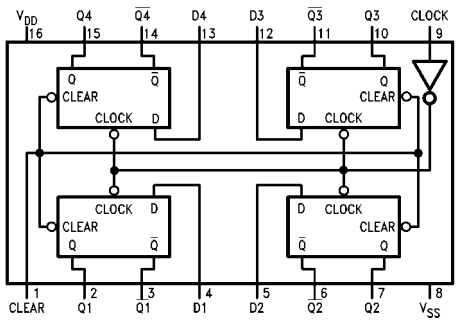
Pin Assignments for DIP and SOIC

CD40174B



Top View

CD40175B



Top View

© 1999 Fairchild Semiconductor Corporation

Truth Table

Inputs			Outputs	
Clear	**Clock**	**D**	**Q**	**$\overline{Q}$ (Note 1)**
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	H	X	NC	NC
H	L	X	NC	NC

H = HIGH Level
L = LOW Level
X = Irrelevant
↑ = Transition from LOW-to-HIGH level
NC = No change

Note 1: $\overline{Q}$ for CD40175B only

EEPW 电子产品世界 .com.cn

Absolute Maximum Ratings (Note 2)

(Note 3)

DC Supply Voltage (V_{DD})	−0.5V to +18V
Input Voltage (V_{IN})	−0.5V to V_{DD} +0.5V_{DC}
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 3)

DC Supply Voltage (V_{DD})	3V to 15 V_{DC}
Input Voltage (V_{IN})	0V to V_{DD} V_{DC}
Operating Temperature Range (T_A)	−40°C to +85°C

Note 2: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 3: V_{SS} = 0V unless otherwise specified.

DC Electrical Characteristics (Note 3)

CD40174BC/CD40175BC

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		4			4		30	µA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		8			8		60	µA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		16			16		120	µA
V_{OL}	LOW Level Output Voltage	V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	HIGH Level Output Voltage	V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	LOW Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	HIGH Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	LOW Level Output Current (Note 4)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	HIGH Level Output Current (Note 4)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.30		-10^{-5}	−0.30		−1.0	µA
		V_{DD} = 15V, V_{IN} = 15V		0.30		10^{-5}	0.30		1.0	µA

Note 4: I_{OH} and I_{OL} are tested one output at a time.

EEPW .com.cn

AC Electrical Characteristics (Note 5)

$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$k and $t_r = t_f = 20$ ns, unless otherwise specified

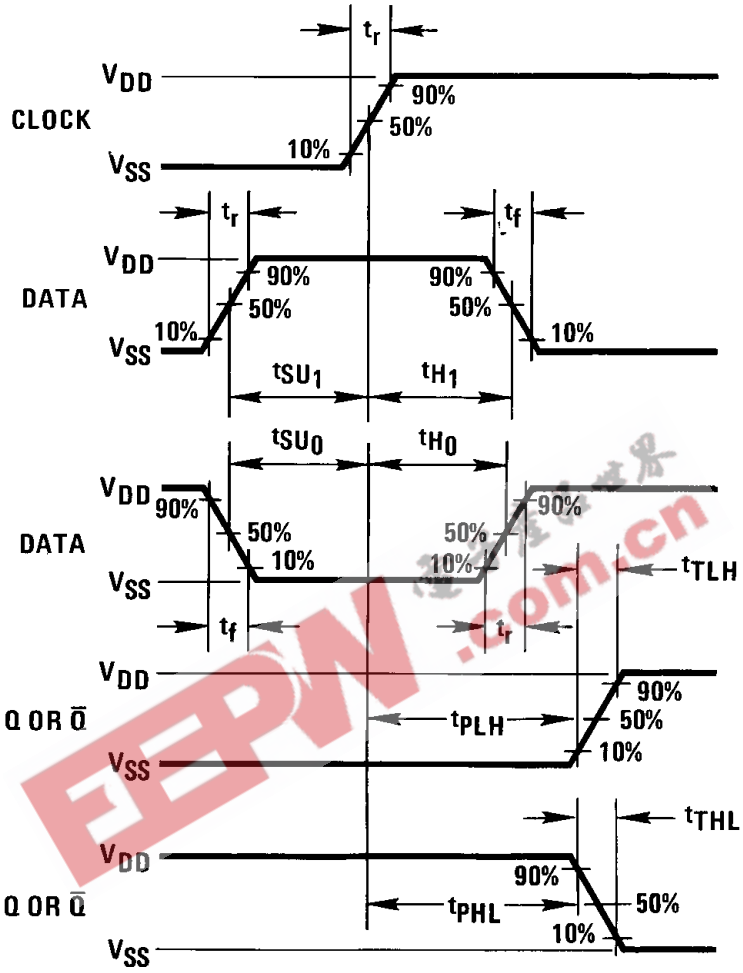
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}, t_{PLH}	Propagation Delay Time to a	$V_{DD} = 5V$		190	300	ns
	Logical "0" or Logical "1" from	$V_{DD} = 10V$		75	110	ns
	Clock to Q or $\overline{Q}$ (CD40175 Only)	$V_{DD} = 15V$		60	90	ns
t_{PHL}	Propagation Delay Time to a	$V_{DD} = 5V$		180	300	ns
	Logical "0" from Clear to Q	$V_{DD} = 10V$		70	110	ns
		$V_{DD} = 15V$		60	90	ns
t_{PLH}	Propagation Delay Time to a Logical	$V_{DD} = 5V$		230	400	ns
	"1" from Clear to $\overline{Q}$ (CD40175 Only)	$V_{DD} = 10V$		90	150	ns
		$V_{DD} = 15V$		75	120	ns
t_{SU}	Time Prior to Clock Pulse that	$V_{DD} = 5V$		45	100	ns
	Data must be Present	$V_{DD} = 10V$		15	40	ns
		$V_{DD} = 15V$		13	35	ns
t_H	Time after Clock Pulse that	$V_{DD} = 5V$		−11	0	ns
	Data Must be Held	$V_{DD} = 10V$		−4	0	ns
		$V_{DD} = 15V$		−3	0	ns
t_{THL}, t_{TLH}	Transition Time	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
t_{WH}, t_{WL}	Minimum Clock Pulse Width	$V_{DD} = 5V$		130	250	ns
		$V_{DD} = 10V$		45	100	ns
		$V_{DD} = 15V$		40	80	ns
t_{WL}	Minimum Clear Pulse Width	$V_{DD} = 5V$		120	250	ns
		$V_{DD} = 10V$		45	100	ns
		$V_{DD} = 15V$		40	80	ns
t_{RCL}	Maximum Clock Rise Time	$V_{DD} = 5V$	15			µs
		$V_{DD} = 10V$	5.0			µs
		$V_{DD} = 15V$	5.0			µs
t_{fCL}	Maximum Clock Fall Time	$V_{DD} = 5V$	15	50		µs
		$V_{DD} = 10V$	5.0	50		µs
		$V_{DD} = 15V$	5.0	50		µs
f_{CL}	Maximum Clock Frequency	$V_{DD} = 5V$	2.0	3.5		MHz
		$V_{DD} = 10V$	5.0	10		MHz
		$V_{DD} = 15V$	6.0	12		MHz
C_{IN}	Input Capacitance	Clear Input		10	15	pF
		Other Input		5.0	7.5	pF
C_{PD}	Power Dissipation	Per Package (Note 6)		130		pF

Note 5: AC Parameters are guaranteed by DC correlated testing.

Note 6: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see 74C Family Characteristics application note, AN-90.

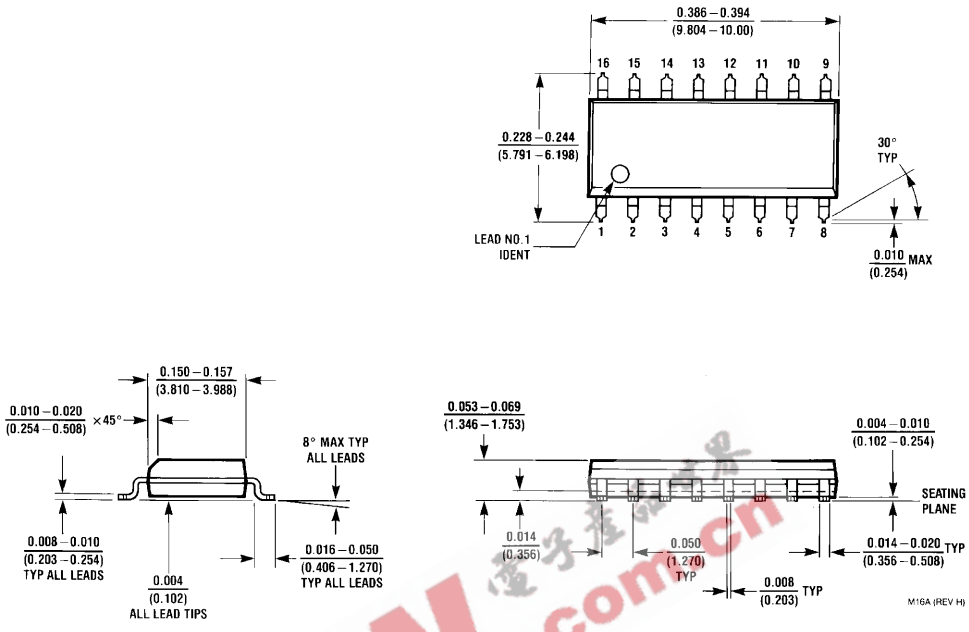
EEPW .com.cn

Switching Time Waveforms



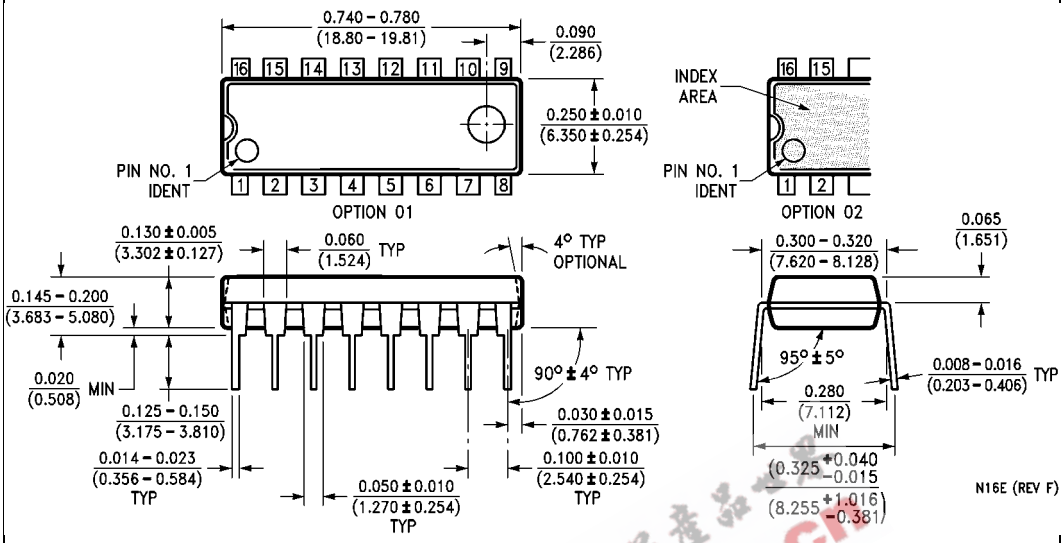
$t_r = t_f = 20$ ns

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body
Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16E

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com