

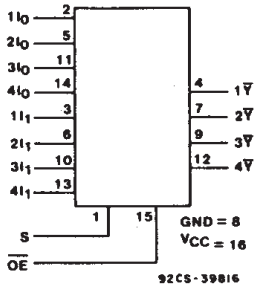
CD54/74HC258 CD54/74HCT258

File Number 1775



Data sheet acquired from Harris Semiconductor
SCHS276

High-Speed CMOS Logic



Quad 2-Input Multiplexer with 3-State Inverting Outputs

Type Features:

- Buffered inputs
- Typical CD54/74HC258 propagation delay = 7 ns @ $V_{CC} = 5\text{ V}$, $C_L = 15\text{ pF}$, $T_A = 25^\circ\text{C}$

FUNCTIONAL DIAGRAM

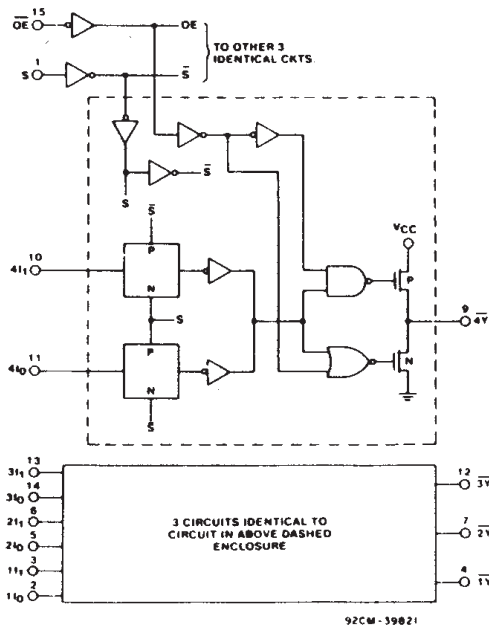
The RCA-CD54/74HC258 and CD54/74HCT258 are quad 2-input multiplexers which select four bits of data from two sources under the control of a common Select input (S). The Output Enable input (\overline{OE}) is active LOW. When \overline{OE} is HIGH, all of the outputs (1Y-4Y) are in the high impedance state regardless of all other input conditions.

Moving data from two groups of registers to four common output busses is a common use of the 258. The state of the Select input determines the particular register from which the data comes. It can also be used as a function generator.

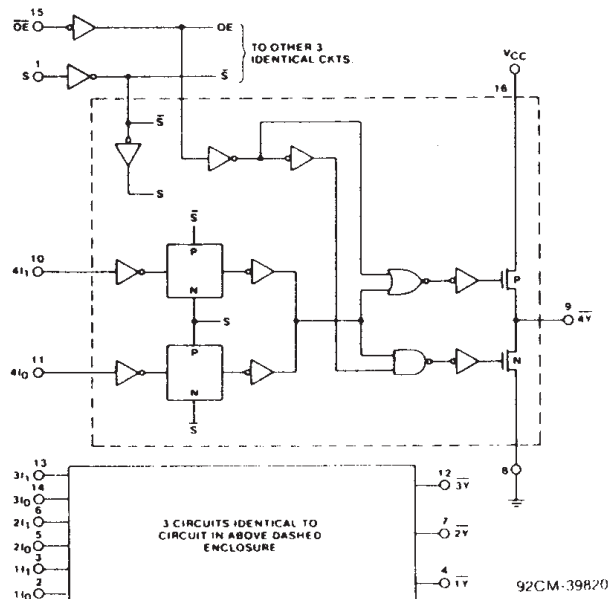
The CD54HC/HCT258 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC/HCT258 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- Fanout (Over Temperature Range):
 - Standard Outputs - 10 LSTTL Loads
 - Bus Driver Outputs - 15 LSTTL Loads
- Wide Operating Temperature Range:
 - CD74HC/HCT/HCU: -40 to +85°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- Alternate Source is Philips/Sigmetics
- CD54HC/CD74HC Types:
 - 2 to 6 V Operation
 - High Noise Immunity:
 - $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} ; @ $V_{CC} = 5\text{ V}$
- CD54HCT/CD74HCT Types:
 - 4.5 to 5.5 V Operation
 - Direct LSTTL Input Logic Compatibility
 - $V_{IL} = 0.8\text{ V Max.}$, $V_{IH} = 2\text{ V Min.}$
 - CMOS Input Compatibility
 - $I_1 \leq 1\text{ }\mu\text{A}$ @ V_{OL} , V_{OH}



CD54/74HC258 Logic Diagram



CD54/74HCT258 Logic Diagram

CD54/74HC258 CD54/74HCT258

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) -0.5 to +7 V

DC INPUT DIODE CURRENT, I_{IK} (FOR $V_i < -0.5$ V OR $V_i > V_{CC} + 0.5$ V) ± 20 mA

DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC} + 0.5$ V) ± 20 mA

DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR -0.5 V $< V_o < V_{CC} + 0.5$ V) ± 35 mA

DC V_{CC} OR GROUND CURRENT (I_{CC}) ± 70 mA

POWER DISSIPATION PER PACKAGE (P_o):
For $T_A = -40$ to $+60^\circ$ C (PACKAGE TYPE E) 500 mW
For $T_A = +60$ to $+85^\circ$ C (PACKAGE TYPE E) Derate Linearly at 8 mW/ $^\circ$ C to 300 mW
For $T_A = -55$ to $+100^\circ$ C (PACKAGE TYPE F, H) 500 mW
For $T_A = +100$ to $+125^\circ$ C (PACKAGE TYPE F, H) Derate Linearly at 8 mW/ $^\circ$ C to 300 mW
For $T_A = -40$ to $+70^\circ$ C (PACKAGE TYPE M) 400 mW
For $T_A = +70$ to $+125^\circ$ C (PACKAGE TYPE M) Derate Linearly at 6 mW/ $^\circ$ C to 70 mW

OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H -55 to $+125^\circ$ C
PACKAGE TYPE E, M -40 to $+85^\circ$ C

STORAGE TEMPERATURE (T_{stg}) -65 to $+150^\circ$ C

LEAD TEMPERATURE (DURING SOLDERING):
At distance $1/16 \pm 1/32$ in. (1.59 ± 0.79 mm) from case for 10 s max. $+265^\circ$ C
Unit inserted into a PC Board (min. thickness $1/16$ in., 1.59 mm)
with solder contacting lead tips only $+300^\circ$ C

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

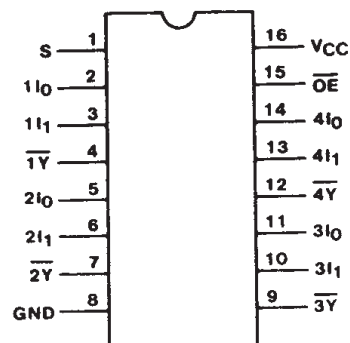
CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For $T_A =$ Full Package-Temperature Range) V_{CC} .* CD54/74HC Types CD54/74HCT Types	2 4.5	6 5.5	V
DC Input or Output Voltage V_i, V_o	0	V_{CC}	V
Operating Temperature T_A : CD74 Types CD54 Types	-40 -55	+85 +125	$^\circ$ C
Input Rise and Fall Times t_r, t_f at 2 V at 4.5 V at 6 V	0 0 0	1000 500 400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

FUNCTION TABLE

Output Enable	Select Input	Data Inputs		Output
\overline{OE}	S	I_0	I_1	\overline{Y}
H	X	X	X	Z
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = High level voltage
L = Low level voltage
X = Don't care.
Z = High impedance (off) state



92CS-39815

TERMINAL ASSIGNMENT

Technical Data

CD54/74HC258 CD54/74HCT258

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC258/CD54HC258										CD74HCT258/CD54HCT258										UNITS	
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPE		54HCT TYPE				
	V _I V	I _O mA	V _{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V _I V	V _{CC} V	+25°C			-40/ +85°C		-55/ +125°C				
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max			
High-Level Input Voltage V _{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5		2	—	—	2	—	2	—	V	
			4.5	3.15	—	—	3.15	—	3.15	—	—	to										
			6	4.2	—	—	4.2	—	4.2	—	—	5.5										
Low-Level Input Voltage V _{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5		—	—	0.8	—	0.8	—	0.8	V	
			4.5	—	—	1.35	—	1.35	—	1.35	—	to										
			6	—	—	1.8	—	1.8	—	1.8	—	5.5										
High-Level Output Voltage V _{OH} CMOS Loads	V _{IL}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V _{IL}	4.5	4.4	—	—	4.4	—	4.4	—	4.4	V	
	or		4.5	4.4	—	—	4.4	—	4.4	—	or		4.5	4.4	—	—	4.4	—	4.4	—	4.4	V
	V _{IH}		6	5.9	—	—	5.9	—	5.9	—	V _{IH}		6	5.9	—	—	5.9	—	5.9	—	5.9	V
TTL Loads (Bus Driver)	V _{IL}	-6	4.5	3.98	—	—	3.84	—	3.7	—	V _{IL}	4.5	3.98	—	—	3.84	—	3.7	—	3.7	V	
	or		4.5	3.98	—	—	3.84	—	3.7	—	or		4.5	3.98	—	—	3.84	—	3.7	—	3.7	V
	V _{IH}		-7.8	6	5.48	—	—	5.34	—	5.2	—		V _{IH}	-7.8	6	5.48	—	—	5.34	—	5.2	—
Low-Level Output Voltage V _{OL} CMOS Loads	V _{IL}	0.02	2	—	—	0.1	—	0.1	—	0.1	V _{IL}	4.5	—	—	0.1	—	0.1	—	0.1	—	0.1	V
	or		4.5	—	—	0.1	—	0.1	—	0.1	—		or	4.5	—	—	0.1	—	0.1	—	0.1	V
	V _{IH}		6	—	—	0.1	—	0.1	—	0.1	—		V _{IH}	6	—	—	0.1	—	0.1	—	0.1	—
TTL Loads (Bus Driver)	V _{IL}	6	4.5	—	—	0.26	—	0.33	—	0.4	V _{IL}	4.5	—	—	0.26	—	0.33	—	0.4	—	0.4	V
	or		4.5	—	—	0.26	—	0.33	—	0.4	—		or	4.5	—	—	0.26	—	0.33	—	0.4	V
	V _{IH}		7.8	6	—	—	0.26	—	0.33	—	0.4		V _{IH}	7.8	6	—	—	0.26	—	0.33	—	0.4
Input Leakage Current I _I	V _{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V _{CC} & Grid	5.5	—	—	±0.1	—	±1	—	±1	—	±1	μA
Quiescent Device Current I _{CC}	V _{CC} or Gnd	0	6	—	—	8	—	80	—	160	V _{CC} or Gnd	5.5	—	—	8	—	80	—	160	—	160	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI _{CC} *											V _{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	—	490	μA
3-State leakage current I _{OZ}	V _{IL} or V _{IH}	V _O = V _{CC} or Gnd	6	—	—	±0.5	—	±5	—	±10	V _{IL} or V _{IH}	5.5	—	—	±0.5	—	±5	—	±10	—	±10	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
Data	0.5
S	1.5
OE	1.5

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

CD54/74HC258 CD54/74HCT258

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC	CL (pF)	TYPICAL		UNITS
		HC	HCT	
nI _O , nI _I , to \bar{Y}	t _{PHL} t _{PLH}	15	7 11	ns
\overline{OE} to \bar{Y}	t _{PZL} t _{PZH}	15	11 11	ns
	t _{PLZ} t _{PHZ}	15	12 12	ns
S to \bar{Y}	t _{PHL} t _{PLH}	15	11 14	ns
Power Dissipation Capacitance*	C _{PD}	—	49 49	pF

*C_{PD} is used to determine the dynamic power consumption, per multiplexer.
 $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where: f_i = input frequency
 C_L = output load capacitance
 V_{CC} = supply voltage

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	V _{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
		HC		HCT		74HC		74HCT		54HC		54HCT		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay, nI _O , nI _I , to \bar{Y} (Fig. 2)	t _{PLH}	2	— 95	—	—	—	120	—	—	—	145	—	—	ns
	t _{PHL}	4.5	— 19	—	27	—	24	—	34	—	29	—	41	
		6	— 15	—	—	—	20	—	—	—	25	—	—	
Propagation Delay S to \bar{Y} (Fig. 3)	t _{PLH}	2	— 140	—	—	—	175	—	—	—	210	—	—	ns
	t _{PHL}	4.5	— 28	—	34	—	35	—	43	—	42	—	51	
		6	— 24	—	—	—	30	—	—	—	36	—	—	
Propagation Delay \overline{OE} to Y (Fig. 4)	t _{PZL}	2	— 140	—	—	—	175	—	—	—	210	—	—	ns
	t _{PZH}	4.5	— 28	—	28	—	35	—	35	—	42	—	42	
		6	— 24	—	—	—	30	—	—	—	36	—	—	
Propagation Delay \overline{OE} to Y (Fig. 4)	t _{PLZ}	2	— 150	—	—	—	190	—	—	—	225	—	—	ns
	t _{PHZ}	4.5	— 30	—	30	—	38	—	38	—	45	—	45	
		6	— 26	—	—	—	33	—	—	—	38	—	—	
Output Transition Time (Fig. 2)	t _{TLH}	2	— 60	—	—	—	75	—	—	—	90	—	—	ns
	t _{THL}	4.5	— 12	—	12	—	15	—	15	—	18	—	18	
		6	— 10	—	—	—	13	—	—	—	15	—	—	
Input Capacitance	C _I		— 10	—	10	—	10	—	10	—	10	—	10	pF
3-State Output Capacitance	C _O		— 20	—	20	—	20	—	20	—	20	—	20	pF

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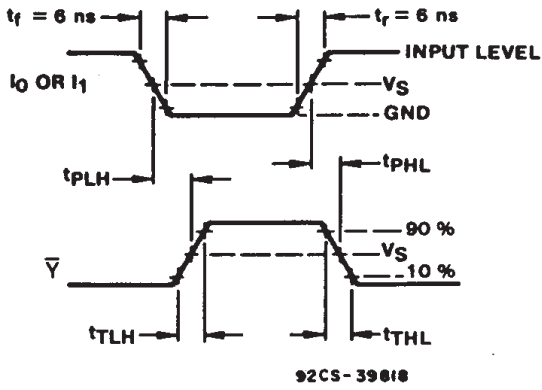


Fig. 2 - Select to output delays.

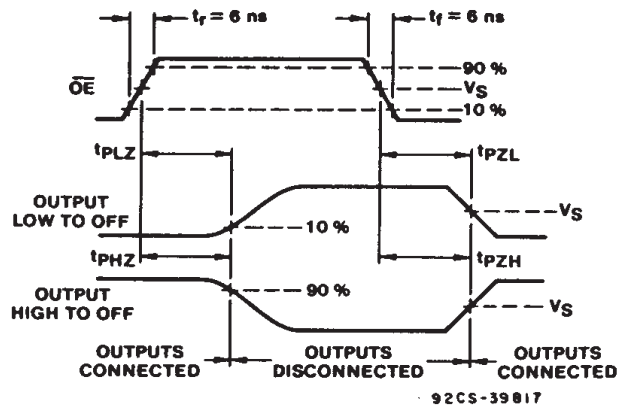


Fig. 4 - Output Enable to output propagation delays.

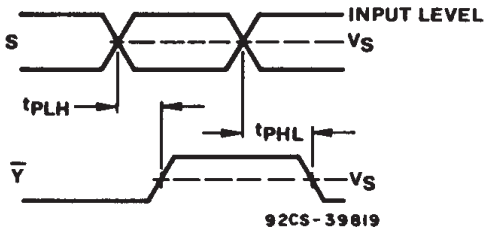


Fig. 3 - Select to output propagation delays.

	54/74HC	54/74HCT
Input Level	V_{CC}	3V
Switching Voltage, V_S	50% V_{CC}	1.3 V

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