Data sheet acquired from Harris Semiconductor
SCHS129

January 1998

CD74HC14, CD74HCT14

High Speed CMOS Logic Hex Inverting Schmitt Trigger

Features

- Unlimited Input Rise and Fall Times
- Exceptionally High Noise Immunity
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} at V_{CC} = 5V
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility, V_{IL} = 0.8V (Max), V_{IH} = 2V (Min)
  - CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}

Description

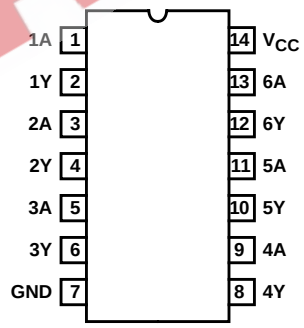
The Harris CD74HC14, CD74HCT14 each contain 6 inverting Schmitt Triggers in one package.

Ordering Information

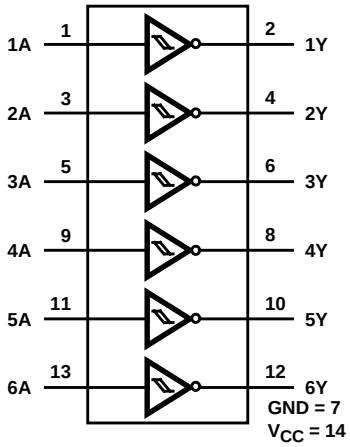
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD54HCT14F	-55 to 125	14 Ld CERDIP	F14.3

Pinout

CD54HC14, CD54HCT14, CD74HC14, CD74HCT14
(PDIP, CERDIP, SOIC)
TOP VIEW



Functional Diagram

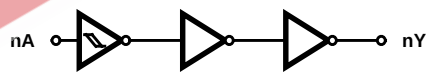


TRUTH TABLE

INPUT (A)	OUTPUT (Y)
L	H
H	L

NOTE:
H= High Level
L = Low Level

Logic Diagram



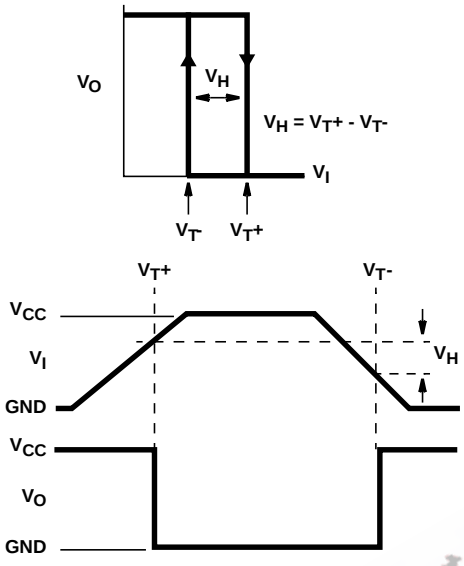


FIGURE 3. HYSTERESIS DEFINITION, CHARACTERISTIC, AND TEST SETUP

Absolute Maximum Ratings

DC Supply Voltage, V_{CC} . . . . . -0.5V to 7V
DC Input Diode Current, I_{IK}
For V_I < -0.5V or V_I > V_{CC} + 0.5V . . . . . ±20mA
DC Output Diode Current, I_{OK}
For V_O < -0.5V or V_O > V_{CC} + 0.5V . . . . . ±20mA
DC Drain Current, per Output, I_O
For -0.5V < V_O < V_{CC} +0.5V . . . . . ±25mA
DC Output Source or Sink Current per Output Pin, I_O
For V_O > -0.5V or V_O < V_{CC} + 0.5V . . . . . ±25mA
DC V_{CC} or Ground Current, I_{CC} . . . . . ±50mA

Operating Conditions

Temperature Range, T_A . . . . . -55^oC to 125^oC
Supply Voltage Range, V_{CC}
HC Types . . . . . 2V to 6V
HCT Types . . . . . 4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O . . . . . 0V to V_{CC}
Input Rise and Fall Time, t_r, t_f
2V . . . . . 100ms (Max)
4.5V. . . . . 100ms (Max)
6V . . . . . 100ms (Max)

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
PDIP Package	90	-
CERDIP Package	130	55
SOIC Package	120	-

Maximum Junction Temperature (Hermetic Package or Die) . . . 175^oC
Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS V_I (V)	TEST CONDITIONS I_O (mA)	TEST CONDITIONS V_{CC} (V)	25^oC MIN	25^oC MAX	-40^oC TO 85^oC MIN	-40^oC TO 85^oC MAX	-55^oC TO 125^oC MIN	-55^oC TO 125^oC MAX	UNITS
HC TYPES											
Input Switch Points	V_{T+}	-	-	2	0.7	1.5	0.7	1.5	0.7	1.5	V
				4.5	1.7	3.15	1.7	3.15	1.7	3.15	V
				6	2.1	4.2	2.1	4.2	2.1	4.2	V
	V_{T-}	-	-	2	0.3	1.0	0.3	1.0	0.3	1.0	V
				4.5	0.9	2.2	0.9	2.2	0.9	2.2	V
				6	1.2	3.0	1.2	3.0	1.2	3.0	V
	V_H	-	-	2	0.2	1.0	0.2	1.0	0.2	1.0	V
				4.5	0.4	1.4	0.4	1.4	0.4	1.4	V
				6	0.6	1.6	0.6	1.6	0.6	1.6	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{T-} or V_{T+}	-0.02	2	1.9	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	V
			-4	4.5	3.98	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	5.34	-	5.2	-	V

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25°C		-40°C TO 85°C		-55°C TO 125°C		UNITS
		V_I (V)	I_O (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	2	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			-	-	-	-	-	-	-	-	V
			4	4.5	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} or GND	-	6	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	6	-	2	-	20	-	40	µA
HCT TYPES											
Input Switch Points	V_T+	-	-	4.5	1.2	1.9	1.2	1.9	1.2	1.9	V
				5.5	1.4	2.1	1.4	2.1	1.4	2.1	V
	V_T-			4.5	0.5	1.2	0.5	1.2	0.5	1.2	V
				5.5	0.6	1.4	0.6	1.4	0.6	1.4	V
	V_H			4.5	0.4	1.4	0.4	1.4	0.4	1.4	V
				5.5	0.4	1.5	0.4	1.5	0.4	1.5	V
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	4.5	4.4	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	4.5	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} and GND	-	5.5	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	5.5	-	2	-	20	-	40	µA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI_{CC} (Note 4)	V_{CC} - 2.1	-	4.5 to 5.5	-	360	-	450	-	490	µA

NOTE:

4. For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
nA	0.6

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Specifications table, e.g., 360µA max at 25°C.

Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
Propagation Delay, A to Y	t_{PLH}, t_{PHL}	C_L = 50pF	2	-	-	135	-	170	-	205	ns
		C_L = 50pF	4.5	-	-	27	-	34	-	41	ns
		C_L = 15pF	5	-	11	-	-	-	-	-	ns
		C_L = 50pF	6	-	-	23	-	29	-	35	ns
Output Transition Times	t_{TLH}, t_{THL}	C_L = 50pF	2	-	-	75	-	95	18	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Input Capacitance	C_I	-	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 5, 6)	C_{PD}	-	5	-	20	-	-	-	-	-	pF
HCT TYPES											
Propagation Delay, A to Y	t_{PLH}, t_{PHL}	C_L = 50pF	4.5	-	-	38	-	48	-	57	ns
		C_L = 15pF	5	-	16	-	-	-	-	-	ns
Output Transition Times	t_{TLH}, t_{THL}	C_L = 50pF	4.5	-	-	15	-	19	-	22	ns
Input Capacitance	C_I	-	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 5, 6)	C_{PD}	-	5	-	20	-	-	-	-	-	pF

NOTES:

5. C_{PD} is used to determine the dynamic power consumption, per inverter.
6. $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = input frequency, C_L = output load capacitance, V_{CC} = supply voltage.

Test Circuits and Waveforms

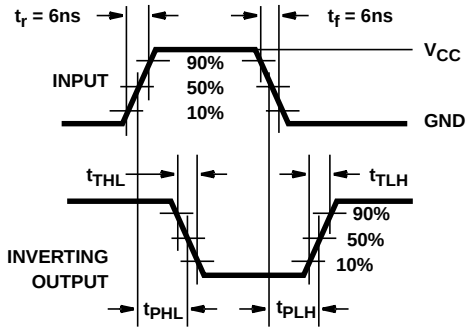


FIGURE 4. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

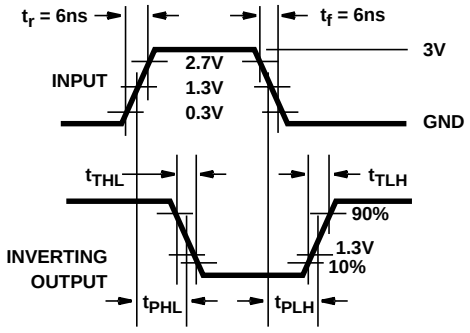


FIGURE 5. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

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